ANALOG DATA MANUAL 1981

SIGNETICS

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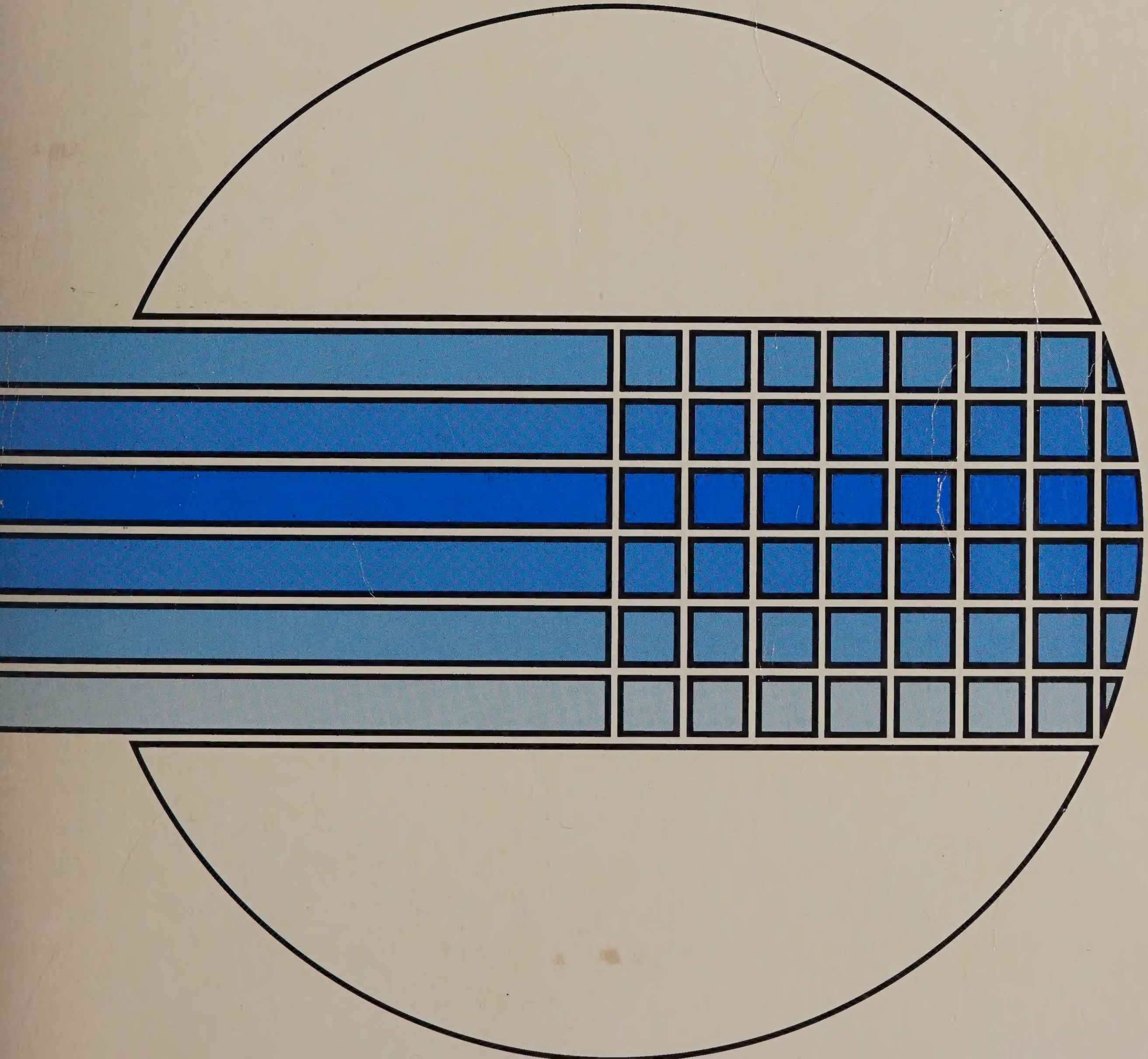

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LIMA TECHNICAL COLLEGE
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LIMA, OHIO 45804

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NOTE
[*] This data sheet may be obtained by writing Publication Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-2111.

INTRODUCTION

As one of the world's largest manufacturers of integrated circuits, Signetics designs, develops, manufactures, and sells over 1600 different types of integrated circuits. Signetics produces integrated circuits utilizing both bipolar and metal-oxide semiconductor (MOS) manufacturing processes for Memory, Microprocessor, Digital, and Analog applications.

The Analog division, one of eight divisions, is a major broad line supplier of Analog circuits consisting of Signetics' original designs, industry standard devices, and custom circuits for EDP, Automotive, Military, Communications, Industrial, and Consumer markets. The family of 555 Timers, the NE5534 High Performance Operational Amplifier, the NE5018 and NE5020 microprocessor compatible DAC's and the NE5560 Switched Mode Power Supply Regulator are a few examples of Signetics' original products. The breadth of the Analog product line offers the designer, the component engineer, and the purchasing agent a broad Analog circuit product line backed by Signetics' industry image as a quality manufacturer to whom the servicing of the customers' needs is paramount.

The 1981 Analog Data Manual is intended to serve as a single reference for Analog circuits by presenting information necessary to select Signetics' Analog products properly. The data manual is updated and rewritten to reflect data on new products issued in the past 2 years, as well as new package configurations such as the new microminiature packages which have recently been released for volume production. Designated the SO package (SO = Small Outline), this new package offers advantages to the hybrid as well as the P.C. board assembler in the purchasing of fully DC- and AC-tested circuits for substrate assembly. Complete details on this new package are available in the Packaging section at the end of this manual.

Additions and errata will be generated at periodic intervals as appropriate.

Your inputs to improve this or any of our publications would be greatly appreciated.

Lou Johnson
Marketing Manager, Analog Division

ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

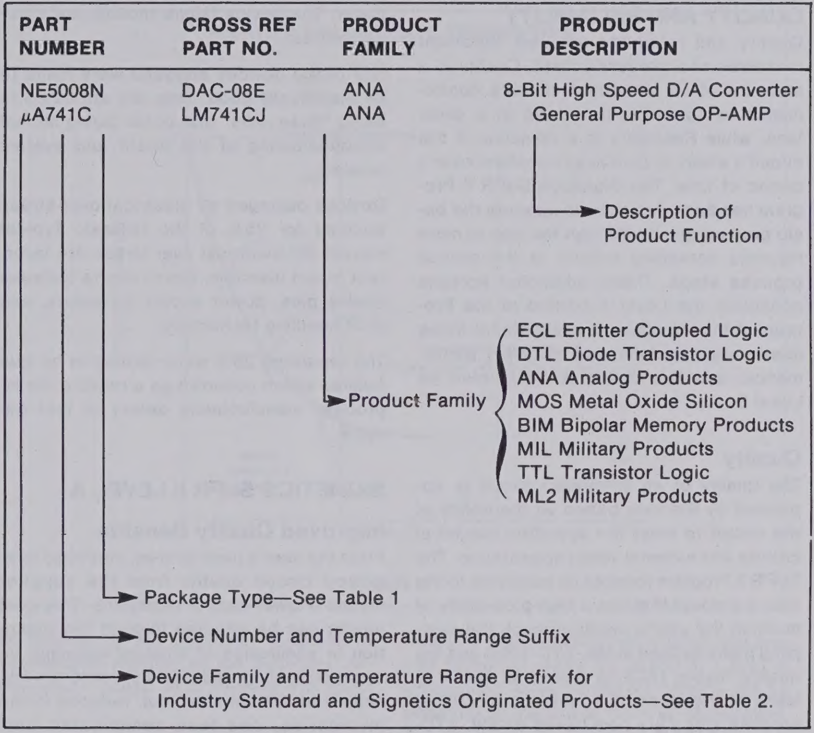
Commercial Product:
$1000 per order
$50 per line item per order

Military Product:
$250 per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix (-55°C to +125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.



PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5008N	DAC-08E	ANA	8-Bit High Speed D/A Converter
μA741C	LM741CJ	ANA	General Purpose OP-AMP

Description of Product Function
Product Family
ECL Emitter Coupled Logic
DTL Diode Transistor Logic
ANA Analog Products
MOS Metal Oxide Silicon
BIM Bipolar Memory Products
MIL Military Products
TTL Transistor Logic
ML2 Military Products
Package Type—See Table 1
Device Number and Temperature Range Suffix
Device Family and Temperature Range Prefix for Industry Standard and Signetics Originated Products—See Table 2.

Table 1 PART NUMBER DESCRIPTION

SUFFIX		PACKAGE DESCRIPTION[2]
Old	New	
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package
DB	HB	3-lead TO-39
DC	EC	4-lead TO-46
DE	EE	4-lead TO-72
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
SK	SK	Microprocessor kit
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
W,WJ	W	10, 14, 16 and 24-lead ceramic (Cerpac) flat
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 2 PACKAGE DESCRIPTIONS

PREFIX	DEVICE TEMPERATURE RANGE
N-	0° to +70°C
S-	-55° to +125°C
NE-	0° to +70°C
SE-	-55° to +125°C
SA	-40° to +85°C
SU	-25° to +85°C

Table 3 DEVICE TEMPERATURE

PREFIX	DEVICE FAMILY
CA	Linear Industry Standard
DS	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LH	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
SD	Linear DMOS
μA	Linear Industry Standard
ULN	Linear Industry Standard

Table 4 FAMILY PREFIX

QUALITY AND RELIABILITY

Quality and reliability are two important measures of a product's merit. Quality is a measure of an integrated circuit's conformance to agreed-upon criteria at a given time, while Reliability is a measure of the circuit's ability to continue to conform over a period of time. The Signetics SUPR II Program has been designed to upgrade the basic product quality through the use of more rigorous screening criteria at the critical process steps. These additional screens constitute the Level A portion of the Program. A burn-in option is available for those users requiring enhanced reliability performance, and this option is designated as Level B.

Quality

The quality of an integrated circuit is appraised by the user based on the ability of the circuit to meet the specified electrical criteria and external visual appearance. The SUPR II Program focuses on supplying to the user a product that has a high probability of meeting the user's needs through the sampling plans defined in MIL-STD-105D and the quality levels (AQL's) stated in Table II. Many of the inspection methods at critical process steps are now based on MIL-STD-883 criteria in order to build, rather than test, quality into the product.

Reliability

System performance over a period of time is the user's measure of an integrated circuit's reliability. The SUPR II Program improves system reliability by building quality into the product via additional manufacturing inspections and the offering of a burn-in screen. In addition to the SUPR II Program, Signetics performs periodic reliability testing via the SURE II/883A Program to assure continuing uniformity and long-term reliability of all product lines. This data base is available upon request as is the ten-year reliability summary, Signetics Product Reliability Report, R-363.

How Do Integrated Circuit Failures Occur?

Results from the Signetics Failure Analysis Lab over a three-year period on product returned from board checkout, system checkout, field usage and accelerated life testing are graphically presented in Figure 1. Under typical system operating conditions, random manufacturing defects, as outlined in Table 1, are the primary cause of true device failure. Also shown in Table 1 are the process controls that have been added via the SUPR II Program to minimize these defects prior to shipment to the customer. The device failure models are categorized as:

Half of the devices analyzed were found to be electrically good. They are attributed to being "false pulls" that occur during normal troubleshooting at the board and system levels.

Devices damaged by electrical over-stress account for 25% of the failures. Typical causes for electrical over-stress are incorrect board insertion, board shorts between device pins, power supply transients, and poor handling techniques.

The remaining 25% were verified to be true failures which occurred as a result of an in-process manufacturing defect or test escape.

SIGNETICS SUPR II LEVEL A

Improved Quality Benefits

From the user's point of view, improved integrated circuit quality from the supplier means a lower cost of ownership. This cost saving can be effected through the reduction or elimination of involved incoming inspection testing, reduced PC board rework, simplified system checkout, reduced in-line inventories, and less complicated part tracking by Purchasing Management.

The SUPR II Program is Corporate in scope and covers Logic (Standard TTL, Schottky TTL, Low Power Schottky TTL, ECL, 8T Interface), Analog (Industrial, Consumer, Interface), Bipolar Memories (RAM's, ROM's, PROM's), and MOS Memories (RAM's, ROM's, Shift Registers), All package options are also available.

The SUPR II flow is detailed in Figure 5, including the test methods and Quality acceptance levels (Table 2 provides the electrical/mechanical finished product AQL's). Highlights of the flow are visual inspections, thermal shock preconditioning, hermeticity, and burn-in, all based on MIL-STD-883 criteria.

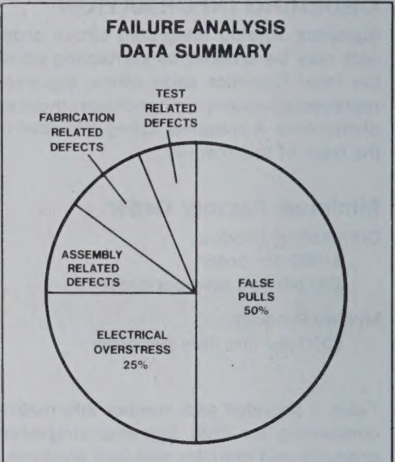


Figure 1

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 2. Here we are comparing the various levels of inspection (AQL's) available for device functionality and its impact on the number of PC boards which must be reworked during system manufacturing. Using the standard commercial AQL in functionality of 1.0%, at 120 integrated circuit packages per board, typically more than 90% of boards will require rework. At 0.15% AQL, rework is reduced to 25%, and at 0.1%, typically only 12% rework is required.

SIGNETICS SUPR II LEVEL B

Infant Mortality Failures

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. A system

FAILURE MECHANISMS	CAUSES	SUPR II CONTROL
Die Fabrication Related	Metalization Oxide Defects Mechanical Scratches Contamination	SEM Monitor Visual Stabilization Bake Burn-In
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Thermal Shock Stabilization Bake Hermeticity Hot-Rail Testing
Test Related	Test Escapes	Tightened AQL Guarantees High Temperature Testing

Table 1

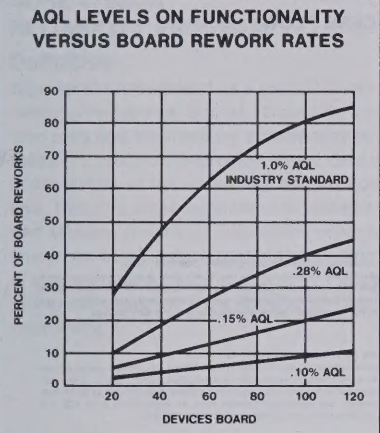


Figure 2

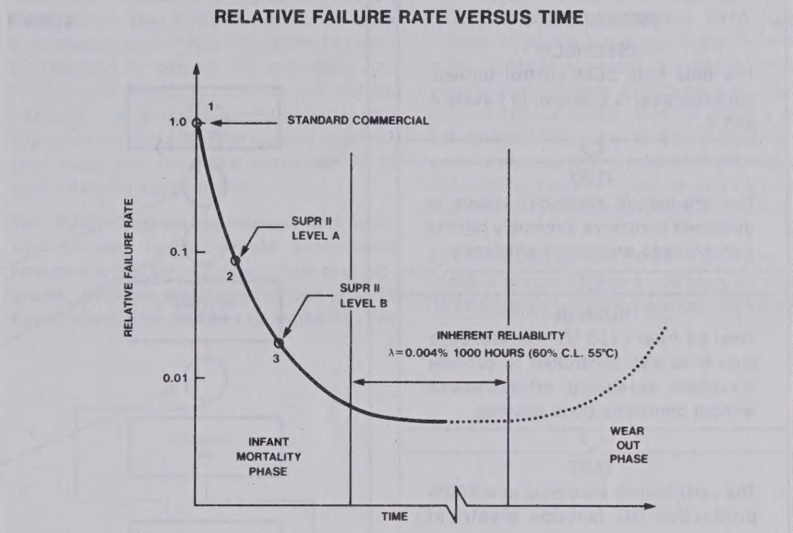


Figure 3

manufacturer has various options to solve problems arising from infant failures. He can ship his system to the end customer and repair field failures as they occur. He can operate the system in-house for this period and repair failures. Or he can purchase devices which have already been preconditioned to eliminate the early failures. Each customer must choose the most cost-effective method for his particular business. A considerable number of the reliabilty defects which cause early failures are eliminated by the manufacturing control and preconditioning steps of SUPR II Level A processing. More persistent defects can be removed by the use of "burn-in" techniques. The "burn-in" processing of SUPR II Level B effectively allows the system manufacturer to ship his equipment at Point 3 on the failure rate curve in Figure 3.

		ANALOG	
		Plastic	Ceramic Metal Can
HOT OPENS	100°C	.015%	-
FUNCTIONALITY (NOTE 1)	25°C	0.10	0.10
	HIGH	0.15	0.15
D.C. PARAMETRIC	25°C	0.15	0.15
TEMPERATURE	OVER	0.40	0.40
A.C. PARAMETRIC	25°C	0.65	0.65
MECHANICAL	MAJOR	0.25	0.25
	MINOR	1.0	1.0
SEAL TEST (CERAMIC METAL CAN ONLY)	FINE LEAK 1 x 10^{-7}cc/s	N/A	1.0
	GROSS LEAK 1 x 10^{-5}cc/s	N/A	0.65

NOTE

1. To insure AQL levels tighter than 0.65% on D.C. parameters usually requires continual correlation of test equipment between customer and vendor to avoid test interpretation problems. If the objective is to reduce system rework costs, functional operation of a device (does it switch or toggle in the system) is often more critical than the absolute value of a parameter. For this reason SUPR II focuses attention on tightened AQL's on functionality.
For analog devices, D.C. parameters, such as input current and offset voltages, tend to be more critical to system operation than for logic devices. A 0.25% AQL is therefore offered on analog D.C. parameters, with the realization that careful attention must be paid to establishing correlation at the customer's incoming inspection.

Table 2 SUPRA II AQL GUARANTEE

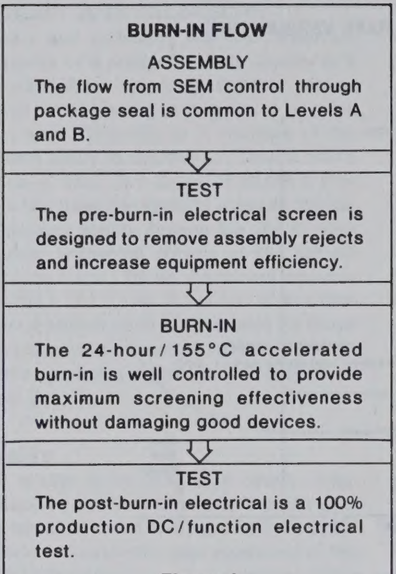
Burn-In Conditions

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is the accelerated burn-in method derived from MIL-STD-883A, utilizing a high temperature reversed bias condition. This bias scheme is preferred for infant mortality screening, while operating conditions are generally utilized for internal reliability programs oriented toward generating MTBF data for the system designer.

Integrated Burn-In Flow

Signetics SUPR II Level B burn-in is performed to provide reliability assurance equivalent to a 168-hour/125°C screen. This process has been integrated into the standard manufacturing flow to provide the customer with the most cost effective screen and significantly reduced delivery times.

BURN-IN FLOW



ASSEMBLY

The flow from SEM control through package seal is common to Levels A and B.

TEST

The pre-burn-in electrical screen is designed to remove assembly rejects and increase equipment efficiency.

BURN-IN

The 24-hour/155°C accelerated burn-in is well controlled to provide maximum screening effectiveness without damaging good devices.

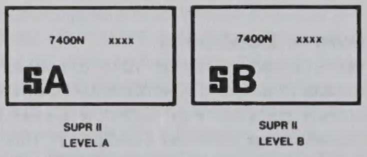
TEST

The post-burn-in electrical is a 100% production DC/function electrical test.

Figure 4

Marking Format

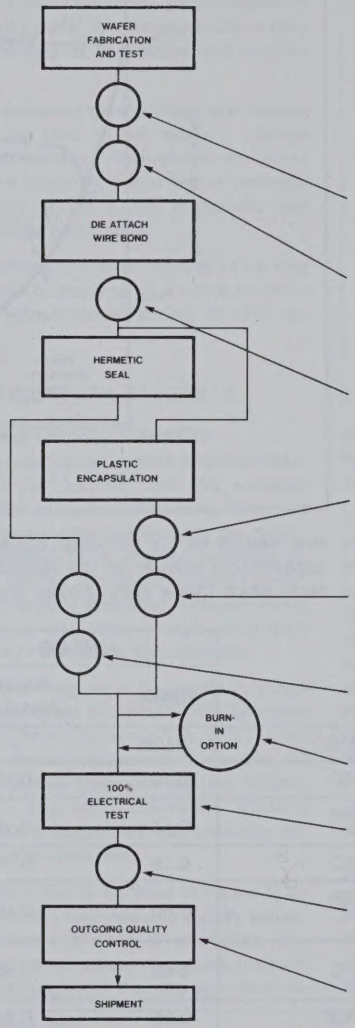
Product processed to the SUPR II manufacturing flow can be identified by an SA for Level A, and an SB for the Level B burn-in option.



NOTE
Marking for Level A in process of being implemented.

Figure 5 shows the generalized process flow for all Signetics integrated circuits purchased to the SUPR II program. Each product group (Analog, Bipolar Memory, Logic, and MOS) may follow slightly different procedures dictated by the specific device characteristics.

SUPR II PROCESS FLOW



SCANNING ELECTRON MICROSCOPE CONTROL (SEM)
Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Critical defects such as scratches, smears, and glassivated bonding pads are inspected to a 1% AQL. Lot acceptance for noncritical defects is to a 4% AQL.

PRE-SEAL VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect any damage incurred at the die attach and wire bonding stations. Critical defects such as scratches, contamination and smeared ball bonds are inspected to a 0.65% AQL. Lot acceptance is to 2.5% AQL.

STABILIZATION BAKE PRECONDITIONING
Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance.

THERMAL SHOCK PRECONDITIONING
MIL-STD-883, Method 1011, Condition A. Devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during high temperature "HOT-RAIL" testing. This preconditioning is especially effective in eliminating intermittent or "HOT-OPENS" problems in plastic devices.

SEAL TESTS
Package seal integrity is ensured by 100% gross leak testing per MIL-STD-883, Method 1014, Condition C and fine leak sampling per Condition A or B.

BURN-IN (LEVEL B OPTION)
Devices are burned in for the equivalent of 168 hours at 125°C in accordance with MIL-STD-883A, Method 1015, Condition F.

100% PRODUCTION ELECTRICAL TESTING
Every device is tested for functional and DC parameters at 25°C, room ambient.

HOT RAIL, HIGH TEMPERATURE TESTING
All plastic devices are subjected to testing at 100°C. In plastic devices this eliminates "HOT-OPENS" and shorts resulting from temperature sensitive intermittent bonds. In addition, logic circuits are tested 100% to a functional pattern that simulates usage in a system environment.

QA GUARANTEES
A final QA inspection step guarantees the mechanical and electrical AQL's of Table II. Every shipment is sealed and identified by QA personnel.

Figure 5

SURE II/883B RELIABILITY PROGRAM

Definition

Signetics is recognized as a manufacturer of reliable integrated circuts. Signetics realized long ago the need for a comprehensive reliability program to provide timely data representative of the entire Signetics product line. Thus the establishment of a Systematic and Uniform Reliability Evaluation program, known as SURE, which provides this data in a manner unique to the industry. Furthermore, this program is provided at no cost to customers.

The SURE Program is a Signetics in-house Qualification Test Program which has been in existence since 1963. The SURE Program is designed to monitor the continuing uniformity of all Signetics products and to demonstrate via periodic qualifications that Signetics products meet or exceed the stringent long-term reliability requirements of their intended applications.

The SURE Program is reviewed and modified annually to incorporate appropriate changes in military microelectronic test programs, products and demonstrated product capabilities, and market requirements. The 1978 SURE II/883B Reliability Program contains minor changes to the 1975 SURE II/883A Program, most significant of which is the inclusion of recent changes in military microelectronic test programs (i.e., inclusion of MIL-SD-883B, Method 5005.4 and MIL-M-3851OD). The SURE II/883B Program continues to incorporate additional environmental tests to fulfill the need for special reliability assurance of plastic products.

For more detailed information regarding the SURE II program, refer to Section 11 of the 1979 Signetics Analog Applications Manual.

ANALOG CROSS REFERENCE

Manufacturer	SIGNETICS	AMD	FAIRCHILD	INTEL	MOTOROLA	NATIONAL	T.I.

TEMPERATURE RANGE CROSS REFERENCE

Commercial	NE	C	C	—	14, 34, 86	3, 86, 88	72, 74, 75
Military	SE	M	M	M	15, 35, 96	1, 96, 78	52, 54, 55

PACKAGE CROSS REFERENCE

Hermetic DIP	F-FE	D	D	C, D	L	D	J
Molded DIP	N	P	P	P	P_2	N	N
Mini-molded DIP	N	T	T	—	P_1	N	P
Metal can	H	H	H	—	G, R	H	L

PART NUMBER CROSS REFERENCES

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
AD741CN	μA741CN	CA555F	SE555F	DS8880J	DS8880F
AD559JD	MC1408-8F	CA555T	SE555H	DS8880N	DS8880N
AD559K	MC1408-8F	CA723CE	μA723CN	LM111D	LM111F
AD559KD	MC1408-8F	CA723CT	μA723CH	LM111H	LM111H
AD559S	MC1508-8F	CA723E	μA723N	LM111J	LM111F
AD559SD	MC1508-8F	CA723T	μA723H	LM111L	LM111H
AM555DC	NE555F	CA741CE	μA741CN	LM119D	LM119F
AM555DM	SE555F	CA741CF	μA741CFE	LM119H	LM119H
AM555HC	NE555H	CA741F	μA741FE	LM119J	LM119F
AM555HM	SE555H	CA747CF	μA747CF	LM124D	LM124F
AM555TC	NE555N	CA747CT	μA747CH	LM124J	LM124F
AM723DC	μA723CF	CA747F	μA747F	LM139D	LM139F
AM723DM	μA723F	CA747T	μA747H	LM139J	LM139F
AM723HC	μA723CH	CA748CE	μA748CN	LM158H	LM158H
AM723HM	μA723H	CA748CF	μA748CF	LM158JG	LM158FE
AM741DC	μA741CFE	CA748F	μA748F	LM158L	LM158H
AM741DM	μA741FE	CA1458E	MC1458N	LM161D	SE529F
AM747DC	μA747CF	CA1458F	MC1458FE	LM161H	SE529H
AM747DM	μA747F	CA1458T	MC1458H	LM161J	SE529F
AM747HC	μA747CH	CA1558T	MC1558H	LM193L	LM193H
AM747HM	μA747H	CA3081E	CA3081N	1LM211D	LM211F
AM748DC	μA748CF	CA3082E	CA3082N	LM211H	LM211H
AM748DM	μA748F	CA3183E	CA3183N	LM211J	LM211F
AMLM111H	LM111H	DM7820AJ	DS7820AF	LM219D	LM219F
AMLM211D	LM211F	DM7820J	DS7820F	LM219H	LM219H
AMLM211H	LM211H	DM7830J	DS7830F	LM219J	LM219F
AMLM311D	LM311F	DM7880J	DS7880F	LM224D	LM224F
AMLM311H	LM311H	DM8820AJ	DS8820AF	LM224J	LM224F
CA111F	LM111F	DM8820AN	DS8820AN	LM224N	LM224N
CA111T	LM111H	DM8820J	DS8820F	LM239D	LM239F
CA124F	LM124F	DM8820N	DS8820N	LM239J	LM239F
CA139AF	LM139AF	DM8830J	DS8830F	LM239N	LM239N
CA139F	LM139F	DM8830N	DS8830N	LM258H	LM238H
CA211F	LM211F	DM8880J	DS8880F	LM258JG	LM258FE
CA211T	LM211H	DM8880N	DS8880N	LM258L	LM258H
CA224F	LM224F	DS1488J	MC1488F	LM258P	LM258N
CA239AF	LM239F	DS1489AJ	MC1489AF	LM293L	LM293H
CA239F	LM239F	DS1489J	MC1489F	LM293P	LM293N
CA301AF	LM301AFE	DS7820AJ	DS7820AF	LM301AJG	LM301AFE
CA311F	LM311F	DS7820J	DS7820F	LM311D	LM311F
CA311T	LM311H	DS7830J	DS7830F	LM311H	LM311H
CA324E	LM324N	DS7880J	DS7880F	LM311J	LM311F
CA324F	LM324F	DS8820J	DS8820F	LM311J-14	LM311F
CA339E	LM339N	DS8820AJ	DS8820AF	LM311JG	LM311FE
CA339F	LM339F	DS8820AN	DS8820AN	LM311L	LM311H
CA555CE	NE555N	DS8820N	DS8820N	LM311N	LM311N
CA555CF	NE555F	DS8830J	DS8830F	LM311P	LM311N
CA555CT	NE555H	DS8830N	DS8830N	LM319D	LM319F

PART NUMBER CROSS REFERENCES (Cont'd)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
LM319H	LM319H	LM748J	μA748F	MC1723G	μA723H
LM319J	LM319F	LM1458H	MC1458H	MC1723L	μA723F
LM319N	LM319N	LM1458J	MC1458FE	MC1733CG	μA733CH
LM324J	LM324F	LM1458N	MC1458N	MC1733CL	μA733CF
LM324N	LM324N	LM1496H	MC1496H	MC1733CP	μA733CN
LM339J	LM339F	LM1496J	MC1496F	MC1733G	μA733H
LM339N	LM339N	LM1496N	MC1496N	MC1733L	μA733F
LM358H	LM358H	LM1558H	MC1558H	MC1741CP1	μA741CN
LM358JG	LM358FE	LM1558J	MC1558FE	MC1741CU	μA741CFE
LM358L	LM358H	LM1596H	MC1596H	MC1741SCG	NE535H
LM358N	LM358N	LM1596J	MC1596F	MC1741SCP1	NE535N
LM358P	LM358N	LM2901J	LM2901F	MC1741SCU	NE535FE
LM361D	NE529F	LM2901N	LM2901N	MC1741SG	SE535H
LM361H	NE529H	LM2902J	LM2902F	MC1741SU	SE535FE
LM361J	NE529F	LM2902N	LM2902N	MC1741U	SE535FE
LM361N	NE529N	LM2903L	LM2903H	MC1747CG	μA747CH
LM381N	LM381N	LM2903N	LM2903N	MC1747CL	μA747CF
LM382N	LM382N	LM2903P	LM2903N	MC1747CP2	μA747CN
LM387N	LM387N	MC1408L6	MC1408-6F	MC1747G	μA747H
LM393H	LM393H	MC1408L7	MC1408-7F	MC1747L	μA747F
LM393L	LM393H	MC1408L8	MC1408-8F	MC1748CP1	μA748CN
LM393N	LM393N	MC1408P6	MC1408-6N	MC1748G	μA748H
LM393P	LM393N	MC1408P7	MC1408-7N	MC3302L	MC3302F
LM555CH	NE555H	MC1408P8	MC1408-8N	MC3302P	MC3302N
LM555CN	NE555N	MC1411P	ULN2001N	MC3456L	NE556F
LM555H	SE555H	MC1416P	ULN2004N	MC3456P	NE556N
LM556CD	NE556F	MC1455G	NE555H	MC3556L	SE556F
LM556CJ	NE556F	MC1455P1	NE555N	MC75107L	75S107F
LM556CN	NE556N	MC1455U	NE555FE	MC75107P	75S107N
LM556D	SE556F	MC1456CP1	MC1456N	MC75108L	75S108F
LM556J	SE556F	MC1456CU	MC1456FE	MC75108P	75S108N
LM565CH	NE565H	MC1456P1	MC1456N	MLM111G	LM111H
LM565CN	NE565N	MC1456U	MC1456FE	MLM111L	LM111F
LM565H	SE565H	MC1458CG	MC1458H	MLM111U	LM111FE
LM566CH	NE566H	MC1458CL	MC1458F	MLM124L	LM124F
LM566CN	NE566N	MC1458CP1	MC1458N	MLM139AL	LM139AF
LM566H	SE566H	MC1458CU	MC1458FE	MLM139L	LM139F
LM567H	SE567H	MC1458G	MC1458H	MLM158G	LM158H
LM567CN	NE567N	MC1458JG	MC1458FE	MLM158U	LM158FE
LM567H	SE567H	MC1458P	MC1458N	MLM211G	LM211H
LM723CD	μA723CF	MC1458P1	MC1458N	MLM211L	LM211F
LM723CH	μA723CH	MC1458SG	NE5535H	MLM211U	LM211FE
LM723CJ	μA723CF	MC1458SL	NE5535F	MLM224L	LM224F
LM723CN	μA723CN	MC1458SP1	NE5535N	MLM224P	LM224N
LM723D	μA723F	MC1458U	MC1458FE	MLM239AL	LM239AF
LM723H	μA723H	MC1488L	MC1488F	MLM239AP	LM239AN
LM723J	μA723F	MC1489AL	MC1489AF	MLM239L	LM239F
LM723N	μA723N	MC1489L	MC1489F	MLM239P	LM239N
LM733CD	μA733CF	MC1496G	MC1496H	MLM258G	LM258H
LM733CH	μA733CH	MC1496L	MC1496F	MLM258P1	LM258N
LM733CJ	μA733CF	MC1496P	MC1496N	MLM258U	LM258FE
LM733CN	μA733CN	MC1508L8	MC1508-8F	MLM301AP1	LM301AN
LM733D	μA733F	MC1555G	SE555H	MLM301AU	LM301AFE
LM733H	μA733H	MC1555U	SE555FE	MLM311G	LM311H
LM733T	μA733F	MC1556U	MC1556FE	MLM311L	LM311F
LM741CJ	μA741CFE	MC1558G	MC1558H	MLM311P1	LM311N
LM741CN	μA741CN	MC1558JG	MC1558FE	MLM311U	LM311FE
LM747CD	μA747CF	MC1558SG	SE5535H	MLM324L	LM324F
LM747CH	μA747CH	MC1558SL	SE5535F	MLM324P	LM324N
LM747CJ	μA747CF	MC1558U	MC1558FE	MLM339AL	LM339AF
LM747D	μA747F	MC1596G	MC1596H	MLM339AP	LM339AN
LM747H	μA747H	MC1596L	MC1596F	MLM339L	LM339F
LM747J	μA747F	MC1723CF	μA723CH	MLM339P	LM339N
LM748CJ	μA748CF	MC1723CL	μA723CF	MLM358G	LM358H
LM748CN	μA748CN	MC1723CP	μA723CN	MLM358P1	LM358N

PART NUMBER CROSS REFERENCES (Cont'd)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
MLM358U	LM358FE	μA0802DM-1	MC1508-8F	SN72747J	μA747CF
MLM565CP	NE565N	μA0802PC-1	MC1408-8N	SN72747L	μA747CH
MLM2901P	LM2901N	μA0802PC-2	MC1408-7N	SN72747N	μA747CN
MLM2902P	LM2902N	μA0802PC-3	MC1408-6N	SN72748J	μA748CF
μA111HM	LM111H	μA1458HC	MC1458H	SN72748P	μA748CN
μA124DM	LM124F	μA1458TC	MC1458N	SN72771N	MC1456N
μA224DM	LM224F	μA1558HM	MC1558H	SN75107AT	75S107F
μA301ANC	LM301AN	μA2901PC	LM2901N	SN75107AN	75S107N
μA311HC	LM311H	μA2902PC	LM2902N	SN75108AT	75S108F
μA311TC	LM311N	NE555JG	NE555FE	SN75108AN	75S108N
μA324DC	LM324F	NE555L	NE555H	SN75182J	DS8820F
μA324PC	LM324N	NE555P	NE555N	SN75182N	DS8820N
μA339ADC	LM339AF	NE592G	NE592H	SN75183J	DS8830F
μA339DC	LM339F	NE592L	NE592F	SN75183N	DS8830N
μA339PC	LM339N	RC723D	μA723CF	SN75188J	MC1488F
μA555HC	NE555H	RC723T	μA723CH	SN75188N	MC1488N
μA555HM	SE555H	RC733D	μA733CF	SN75189AT	MC1489AF
μA555TC	NE555N	RC733T	μA733CH	SN75189AN	MC1489AN
μA556DC	NE556F	RC741DN	μA741CN	SN75189J	MC1489F
μA556DM	SE556F	RC747D	μA747CF	SN75189N	MC1489N
μA556PC	NE556N	RC747T	μA747CH	SN75207J	75S207F
μA723CJ	μA723CF	RC1458DN	MC1458N	SN75207N	75S207N
μA723CL	μA723CH	RC1458T	MC1458H	SN75208J	75S208F
μA723CN	μA723CN	RC1488DC	MC1488F	SN75208N	75S208N
μA723DC	μA723CF	RC1489ADC	MC1489AF	TBB0747	μA747CH
μA723DM	μA723F	RC1489DC	MC1489F	TBB0748B	μA748CN
μA723HC	μA723CH	SE555JG	SE555FE	TBB1458	MC1458H
μA723HM	μA723H	SE555L	SE555H	TBB1458B	MC1458N
μA723MJ	μA723F	SE592G	SE592H	TBC0747	μA747H
μA723ML	μA723H	SE592L	SE592F	TBC1458	MC1558H
μA723PC	μA723CN	SFC2111M	LM111H	TDB0555	NE555H
μA733CJ	μA733CF	SFC2211	LM211H	TDB0555B	NE555N
μA733CL	μA733CH	SFC2301ADC	LM301AN	TDB0556A	NE556N
μA733CN	μA733CN	SFC2311	LM311H	TDB0723	μA723CH
μA733DC	μA733CF	SFC2741DC	μA741CN	TDB0723A	μA723CN
μA733DM	μA733F	SFC2741EC	μA741CN	TDC0555	SE555H
μA733HC	μA733CH	SFC2741EM	μA741N	TDC0723	μA723H
μA733HM	μA733H	SFC2748DC	μA748CN	ULN2001A	ULN2001N
μA733MJ	μA733F	SN52555L	SE555H	ULN2003A	ULN2003N
μA733ML	μA733H	SN52558L	MC1558H	ULN2004A	ULN2004N
μA740HC	μA740CH	SN52723J	μA723F	556CJ	NE556CN
μA741CJG	μA741CFE	SN52723L	μA723H	723BE	μA723H
μA741CP	μA741CN	SN52733J	μA733F	723CE	μA723CH
μA741MJG	μA741FE	SN52733L	μA733H	723CT	μA723CN
μA741TC	μA741CN	SN52747J	μA747F	723CL	μA723CF
μA747CJ	μA747CF	SN52747L	μA747H	733BE	μA733H
μA747CL	μA747CH	SN52748J	μA748F	733CE	μA733CH
μA747CN	μA747CN	SN55182J	DS7820F	733CJ	μA733CN
μA747DC	μA747CF	SN55182N	DS7820N	747BE	μA747H
μA747DM	μA747F	SN55183J	DS7830F	747BL	μA747F
μA747HC	μA747CH	SN55183N	DS7830N	747CE	μA747CH
μA747HM	μA747H	SN72301AP	LM301AN	747CJ	μA747CN
μA747MJ	μA747F	SN72311J	LM311F	747CL	μA747CF
μA747ML	μA747H	SN72311L	LM311H	748BL	μA748F
μA747PC	μA747CN	SN72311P	LM311N	748CL	μA748CF
μA748CJ	μA748CF	SN72555L	NE555H	1458CE	MC1458H
μA748CP	μA748CN	SN72555P	NE555N	1458CP	MC1458N
μA748DC	μA748CF	SN72558L	MC1458H	1458E	MC1458H
μA748DM	μA748F	SN72558P	MC1458N	1458P	MC1458N
μA748MJ	μA748F	SN72723L	μA723CH	1558E	MC1558H
μA748TC	μA748CN	SN72723N	μA723CN	2740CE	μA740CH
μA796HC	MC1496H	SN72733J	μA733CF	9665DC	ULN2001F
μA0802DC-1	MC1408-8F	SN72733L	μA733CH	0665PC	ULN2001N
μA0802DC-2	MC1408-7F	SN72733N	μA733CN	UA3089N	CA3089N
μA0802DC-3	MC1408-6F	SN72741P	μA741CN	UA3089	CA3089N

PART NUMBER CROSS REFERENCES (Cont'd)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
UA760HM	NE527H	UA758PC	UA758N	SN7512N	NA733N
UA760DC	NE527N	UA798HM	LM158H	SN76689N	CA3089N
UA798TC	NE532N	UA739PC	LM387N	ULN2210A	UA758N
UA740HM	NE536N	UA739PC	LM382N	ULN2244	µA758N
UA556PC	NE556N	UA796PC	MC1496N	UA740HC	µA740CH
UA0801	DAC-08N	UA760HC	NE529N		
UA0801A	DAC-08AN	SN7512L	NA733CH		

SECTION I
OPERATIONAL AMPLIFIERS

Section 1—OPERATIONAL AMPLIFIERS

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OPERATIONAL AMPLIFIERS DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Acquisition Time

The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time

The time elapsed from the hold command to the opening of the switch.

Aperture Jitter

Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperature delay.

Aperture Time

The delay required between "hold" command and an input analog transition, so that the transition does not affect the hold output.

Bandwidth

The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Effective Aperture Delay

The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure Of Merit

The ratio of the available charging current during sample mode to the leakage current during hold mode.

Hold-Mode Droop

The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold-Mode Feed Through

The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time

The time required for the output to settle within 1mV of final value after the "hold" logic command.

Sample-To-Hold Offset Error

The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate

The fastest rate at which the sample & hold output can change (specified in V/μs).

Hold Step

The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Dynamic Sampling Error

The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error

The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Threshold

Level shall be defined as that level which causes the switch control to change state.

Average Input Offset Current T^{O} coeff.

The change in input offset current divided by the change to ambient temperature producing it.

Average Input Offset Voltage T^{O} coeff.

The change in input offset voltage divided by the change in ambient temperature producing it.

Common Mode Input Resistance

The resistance looking into both inputs, with inputs tied together.

Common Mode Rejection Ratio (CMRR)

The ratio of the change of input offset voltage to the input common mode voltage change producing it.

Full Power Bandwidth

The maximum frequency at which the full sinewave output might be obtained.

Input Bias Current

The average of the two input currents at zero output voltage. In some cases, the input current is measured for either input independently.

OPERATIONAL AMPLIFIERS DEFINITIONS (Cont'd)

Input Capacitance

The capacitance looking into either input terminal with the other grounded.

Input Current

The current into an input terminal.

Input Noise Voltage

The square root of the mean square narrow-band noise voltage referred to the input.

Input Offset Current

The difference in the currents into the two input terminals with the output at zero volts.

Input Offset Voltage

That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

Input Resistance

The resistance looking into either input terminal with the other grounded.

Input Voltage Range

The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

Large-Signal Voltage Gain

The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

Output Resistance

The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

Output Short-Circuit Current

The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Output Voltage Swing

The peak output swing, referred to zero, that can be obtained.

Power Consumption

The dc power required to operate the amplifier with the output at zero and with the output at zero and with no load current.

Power Supply Rejection Ratio

The ratio of the change in input offset voltage to the change in supply voltages producing it.

Rise Time

The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate

The maximum rate of change of output voltage under large signal condition.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Temperature Stability of Voltage Gain

The maximum variation of the voltage gain over the specified temperature range.

NOTE

Refer to Section 3 of the 1979 Analog Applications Manual for an in depth explanation of Operational Amplifiers and their applications

OPERATIONAL AMPLIFIER SELECTION GUIDE

Device #	Complexity	Temp. Range	Max. Input Voltage		Max. Input Current		Min. A VOL V/mV	Typ. BW $A_V=1$ MHz	Typ. Slew Rate V/µs	Diff. Inp. Volt. V	Typical Common Mode Rej. Volt		Typ. PSRR dB	Supply Volt. Typ.		Outp. Curr. mA	Max Supply Curr. mA	Min. Outp. Volt. Swing V	Int. Compensation	Input Noise Volt. N$\sqrt{Hz}$	Packages
			Offset mV	Drift µV/°C	Offset nA	Bias nA					Ratio dB	Range V		Min. V	Max. V						
NE536	Sing.	Ind.	30●	30●	5pA■	0.1▲	25	1.0	6.0	±30	80	±11	80	±6	±20	5.0	8.0▲	±12	yes		H
SU536	Sing.	Ext.	30	20●	5pA■	3.0	50	1.0	6.0	±30	80	±11	86	±6	±18	5.0	5.5▲	±12	yes		H
NE530	Sing.	Ind.	6.0	6●	80	200	25	3.0	35	±30	90	±13	70	±15	±18	25▲	3.0	±12	yes		H,N,FE
SE530	Sing.	Ind.	3.0	15	20	100	25	3.0	35	±30	90	±13	70	±15	±18	25▲	3.0	±12	yes		H,N,FE
SE538	Sing.	Mil.	3.0	15	20	100	25	6.0	60	±30	90	±13	70	±15	±22	25▲	3.6	±12	yes		H,N,FE
NE538	Sing.	Ind.	6.0	6●	80	200	25	6.0	60	±30	90	±13	70	±15	±18	25▲	2.2●	±12	yes		H,N,FE
NE5534/A	Sing.	Ext.	4.0▲		300▲	1500▲	30▲	10.0	13	±5	100	±13	100	±3	±22	38■	6.5▲	±12	yes	4.5	H,N,FE
SE5534/A	Sing.	Mil.	3.0		500	1500	25	10.0	13	±5	100	±13	100	±3	±22	38■	9.0	±12	yes	4.5	H,N,FE
µA740C	Sing.	Ind.	30●		0.06●	10.0	500●	1.0	6.0	±30	80	±12	80	±5	±22	5.0	8.0▲	±12	yes		H
µA741	Sing.	Mil.	6.0		500	1500	25	1.0	0.5	±30	90	±13	100	±3	±22	5.0	2.5	±12	yes		N,FE
µA741C	Sing.	Ind.	7.5		300	800	15	1.0	0.5	±30	90	±13	100	±3	±18	5.0	2.8▲	±12	yes		N,FE
µA748	Sing.	Mil.	6.0		500	1500	25	1.0	0.5	±30	90	±13	90	±3	±22	5.0	2.8	±12	no		N,F
µA748C	Sing.	Ind.	7.5		300	800	25	1.0	0.5	±30	90	±13	90	±3	±18	5.0	2.8	±12	no		N,F
LM158	Dual	Mil.	7.0	7●	100	300	25	1.0		32	70	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		H
LM258	Dual	Ext.	9.0	7●	150	500	15	1.0		32	65	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		H,N,FE
LM358	Dual	Ind.	9.0	7●	150	500	15	1.0		32	65	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		H,N,FE
MC1458	Dual	Ind.	7.5		300	800	15	1.0	0.8	±30	90	±13	90	±3	±18	5.0	5.6▲	±12	yes		H,N,FE
MC1558	Dual	Mil.	6.0		500	1500	25	1.0	0.5	±30	90	±13	90	±3	±22	5.0	5.0▲	±12	yes		H,N,FE
SA1458	Dual	Ext.	7.5		500	1500	15	1.0	0.8	±30	90	±13	90	±3	±18	5.0	5.0▲	±12	yes		N
NE532	Dual	Ind.	7.5	7●	150	500	15	1.0		32	70	$V_S-1.5$	100	3	30	40	1.2	V_S-2	yes		H,N,FE
SA532	Dual	Ext.	7.5	7.5●	150	500	15	1.0		32	70	$V_S-1.5$	100	3	30	40	1.2	V_S-2	yes		N
SE532	Dual	Mil.	7.0	7●	100	300	25	1.0		32	70	$V_S-1.5$	100	3	30	40	1.2	V_S-2	yes		H,FE
µA747	Dual	Mil.	6.0		500	1500	25	1.0	.05	±30	90	±13	90	±3	±22	5.0	3.3	±12	yes		F,H,N
µA747C	Dual	Ind.	7.5		300	800	15	1.0	0.5	±30	90	±13	90	±3	±18	5.0	3.3	±12	yes		F,H,N
SE5535	Dual	Mil.	3.0	15	20	100	25 •	1.0	15	±30	90	±13	70	±3	±22	5.0	3.3	±12	yes		H,N
NE5535	Dual	Ind.	6.0	6●	80	200	25	1.0	15	±30	90	±13	70	±3	±18	5.0	2.0●	±12	yes		H,N
LM124	Quad	Mil.	7.0	7●	100	300	25	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		F
LM224	Quad	Ext.	9.0	7●	150	500	15	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		F,N
LM324	Quad	Ind.	9.0	7●	150	500	15	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		F,N
SA534	Quad	Ext.	9.0	7●	150	500	15	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		N,F
LM2902	Quad	Ext.	15.0	7●	200	1000	15	1.0		26	85	$V_S-1.5$	100	3	26	40	2.0	V_S-2	yes		N
SE5538	Dual	Mil.	3.0	15	20	100	25	6.0	60	±30	90	±13	70	±15	±22	25▲	3.6	±12	yes		H,N
NE5538	Dual	Ind.	6.0	6●	80	200	25	6.0	60	±30	90	±13	70	±15	±18	25▲	2.2●	±12	yes		H,N
SE5530	Dual	Mil.	3.0	15	20	100	25	3.0	35	±30	90■		70	±3	±22		3.6	±13	yes		H,N
NE5530	Dual	Ind.	6.0	6●	80	200	25	3.0	35	±30	90■		70	±3	±18		2.2	±13	yes		H,N
NE5532/A	Dual	Ind.	5.0		200	1000	10	10	9	±5	100		80	±5	±22		16	±15	yes	6	H,FE,N
NE5533/A	Dual	Ind.	5.0		400	2000	15	10	13	±5	100		80	±5	±22		8	±15	yes	4.5	N,F

NOTES

1. Military −55°C-+125°C
   Extended −25°C-+85°C
   Industrial 0°C-+70°C
2. Specifications guaranteed over full temperature range unless otherwise indicated by following marks:
   ● Typical over full temperature range ▲ Guaranteed at 25°C ■ Typical at 25°C

SIGNETICS REPLACEMENT STANDARDS

MC1458 DUAL OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES		QR&A		COMMENTS
						SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	.8	Slew Rate	10 to 60 V/μ sec	NE/SE	5530	Yes		
					5538	Yes		
				NE	5532	Yes		
					5532A	Yes		
					5533	Yes		
					5533A	Yes		
	14	Full power out	30 to 300 kHz	NE/SE	5530	Yes		
					5538	Yes		
				NE	5532	Yes		
					5532A	Yes		
					5533			
					5533A			
	45	Noise	4, 5 nv/$\sqrt{Hz}$	NE	5532			
					5532A			
					5533	Yes		
					5533A	Yes		
	6	Offset voltage	4 mv	NE	5532			
					5532A			
					5533	Yes		
					5533A	Yes		
	500	Bias current	60 to 150 na	NE/SE	5530	Yes		
					5538	Yes		
	1	Gain bandwidth	1.5 ↓ 15 MHz	NE/SE	5530	Yes		
					5538	Yes		
				NE	5533	Yes		
					5533A	Yes		
					5532			
					5532A			
	2,000	Maximum loading	600 OHM	NE	5533			
					5533A	Yes		
					5532	Yes		
					5532A			

SIGNETICS REPLACEMENT STANDARDS

μa741 SINGLE OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES		QR&A SURE II	QR&A SUPR II	COMMENTS
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	0.5	Slew rate	10 to 600 V/μ sec	NE/SE	530	Yes		
					538	Yes		
					5534	Yes	Yes	
					5534A	Yes	Yes	*Not pin for pin replacement.
				NE	5539*			
	10	Full power out	300 to 350,000 kHz	NE/SE	530	Yes		
					538	Yes		
					5534	Yes	Yes	
					5534A	Yes	Yes	*Not pin for pin replacement.
				NE	5539*			
	45	Noise	4, 5 nv/$\sqrt{\text{Hz}}$	NE/SE	5534	Yes	Yes	
					5534A	Yes	Yes	
	5	Offset voltage	4 mv	NE/SE	5534	Yes	Yes	
					5534A	Yes	Yes	
	500	Bias current	60 to 150 na	NE/SE	530	Yes		
					538	Yes		
	1	Gain bandwidth	1.5 ↓ 1200 MHz	NE/SE	530	Yes		
					538	Yes		
					5534	Yes	Yes	
					5534A	Yes	Yes	*Not pin for pin replacement.
				NE	5539*			
	2,000	Maximum loading	600 OHM	NE/SE	5534	Yes	Yes	
					5534A	Yes	Yes	

LF355/356-H,N

DESCRIPTION

The LF355 and LF356 operational amplifiers employ well matched, high voltage JFET input structures on the same monolithic chip as bipolar devices. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low noise.

COMMON FEATURES

(TYPICAL)

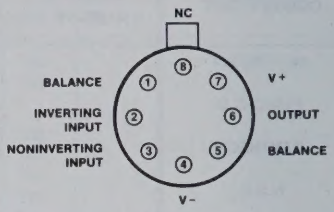
- **Low input bias current 50pA**
- **Low input offset current 10pA**
- **High input impedance $10^{12}\Omega$**
- **Low input offset voltage 3mV**
- **Low V_{OS} temperature drift $5\mu V/°C$**
- **Low input noise current $0.01pA/\sqrt{Hz}$**

APPLICATIONS

- **Precision high speed integrators**
- **Fast A/D, D/A converters**
- **High impedance buffers**
- **Wideband, low noise, low drift amplifier**

PIN CONFIGURATION

H PACKAGE*

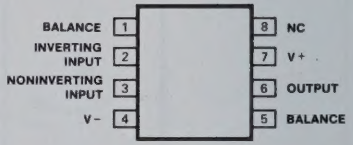

NC
8
BALANCE
1
7
V+
INVERTING INPUT
2
6
OUTPUT
NONINVERTING INPUT
3
5
BALANCE
4
V−

ORDER PART NO.

LF355H LF356H

*Metal cans (H) not recommended for new designs

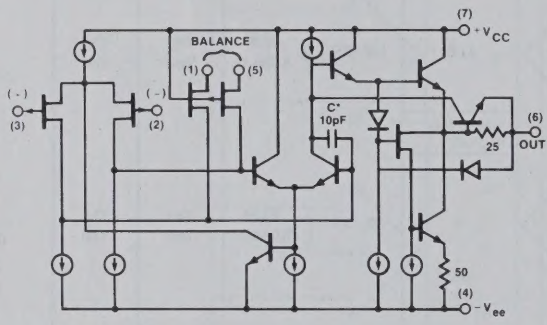
N PACKAGE


BALANCE
1
INVERTING INPUT
2
NONINVERTING INPUT
3
V−
4
8
NC
7
V+
6
OUTPUT
5
BALANCE

ORDER PART NO.

LF355N LF356N

EQUIVALENT SCHEMATIC


(7)
+VCC
BALANCE
(1)
(5)
(-)
(3)
(-)
(2)
C*
10pF
(6)
25
OUT
50
(4)
−Vee

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
T_j (Max)	100	°C
Input voltage range[1]	±20	V
Output short circuit duration	Continuous	
Storage temperature range	−65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

NOTE

1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

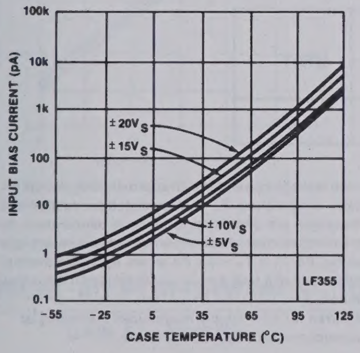
PARAMETER		TEST CONDITIONS	LF355			LF356			UNIT
			Min	Typ	Max	Min	Typ	Max	
SR	Slew rate	$A_V = 1$		5			12		V/µs
GBW	Gain bandwidth product			2.5			5		MHz
t_s	Settling time[1] to 0.01%			4			1.5		µs
e_n	Equiv. input noise volt.	$R_S = 100\Omega$ f = 100Hz f = 1000Hz		 25 20			 15 12		 nV/√Hz nV/√Hz
i_n	Equiv. input noise current	f = 100Hz f = 1000Hz		0.01 0.01			0.01 0.01		pA/√Hz pA/√Hz
C_{IN}	Input capacitance			3			3		pF

NOTE

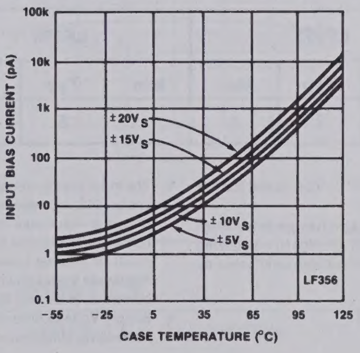
1. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

TYPICAL DC PERFORMANCE CHARACTERISTICS

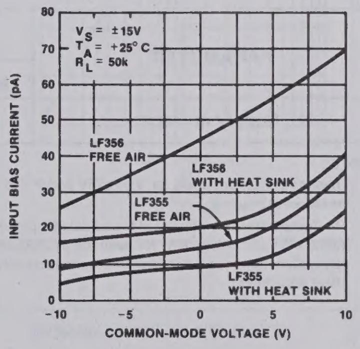
INPUT BIAS CURRENT



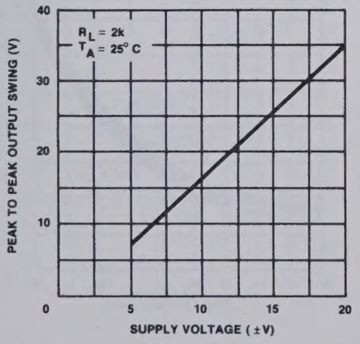
INPUT BIAS CURRENT



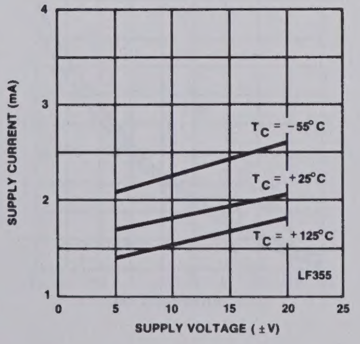
INPUT BIAS CURRENT



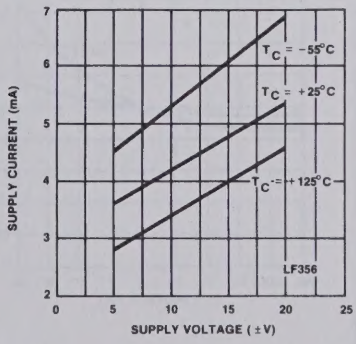
VOLTAGE SWING



SUPPLY CURRENT



SUPPLY CURRENT



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LF355/356			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	$R_s = 50\Omega$		3	10	mV
					13	mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	$R_s = 50\Omega$		5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	$R_s = 50\Omega$		0.5		$\mu V/°C$ per mV
I_{OS}	Input offset current[1,3]	$T_J = 25°C$		3	50	pA
		$T_J \le T_{high}$			2	nA
I_B	Input bias current[1,3]	$T_J = 25°C$		30	200	pA
		$T_J \le T_{high}$			8	nA
R_{IN}	Input resistance	$T_J = 25°C$				Ω
A_{VOL}	Large signal voltage gain	$V_s = \pm 15V$	25	10^{12}		V/mV
		$V_O = \pm 10V$, $R_L = 2k\Omega$		200		
		Over temp.	15			V/mV
V_O	Output voltage swing	$V_s = \pm 15V$, $R_L = 10k\Omega$	±12	±13		V
		$V_s = \pm 15V$, $R_L = 2k\Omega$	±10	±12		V
V_{CM}	Input common mode			+15.1		V
	Voltage range	$V_s = \pm 15V$	±10			V
				-12		V
CMRR	Common-mode rejection ratio		80	100		dB
PSRR	Supply volt. rej. ratio[4]		80	100		dB

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_s = \pm 15V$ unless otherwise specified.

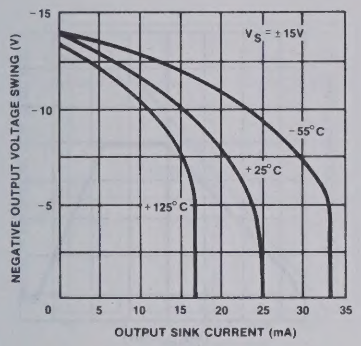
PARAMETER	LF355			LF356			UNIT
	Min	Typ	Max	Min	Typ	Max	
Supply current		2	4		5	10	mA

NOTES

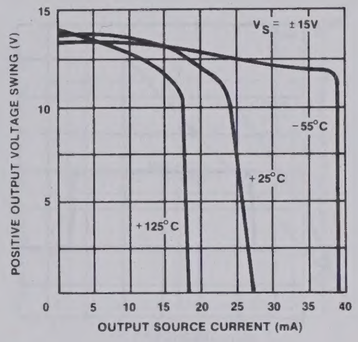
1. These specifications apply for $V_S = \pm 15V$ and $0° C \le T_A \le +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
2. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
4. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)

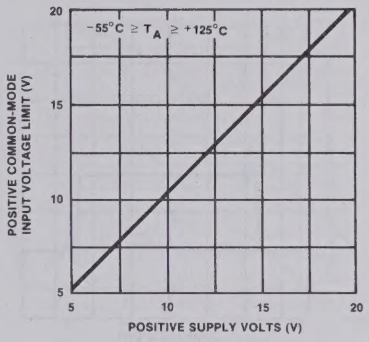
NEGATIVE CURRENT LIMIT



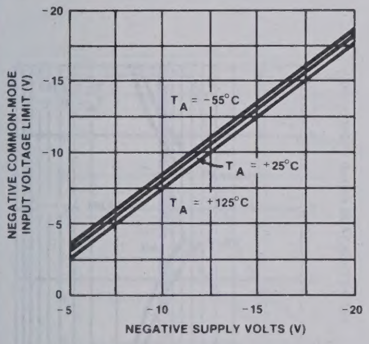
POSITIVE CURRENT LIMIT



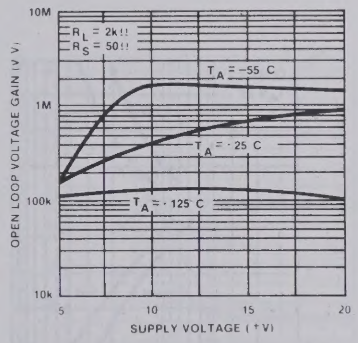
POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT



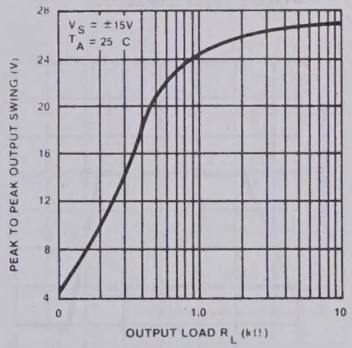
NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT



OPEN LOOP VOLTAGE GAIN

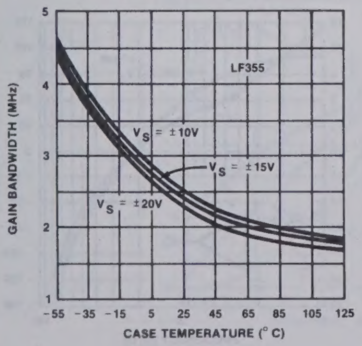


OUTPUT VOLTAGE SWING

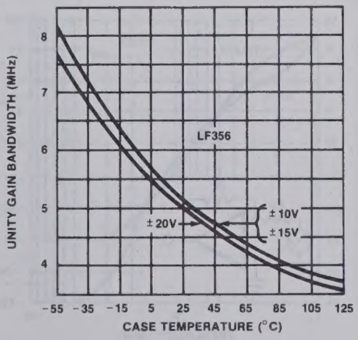


TYPICAL AC PERFORMANCE CHARACTERISTICS

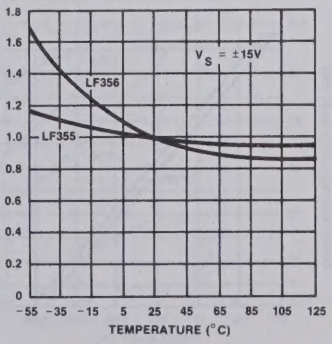
GAIN BANDWIDTH



UNITY GAIN BANDWIDTH

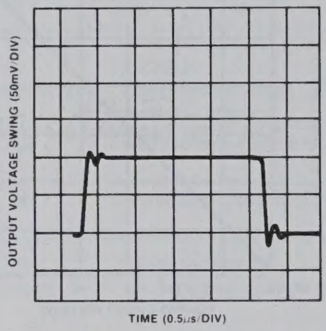


NORMALIZED SLEW RATE

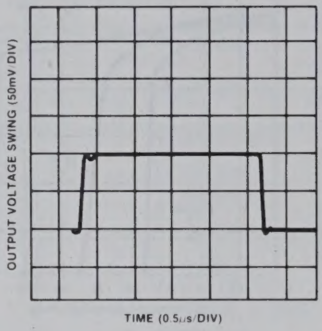


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

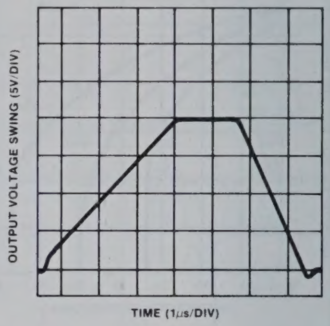
LF355 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



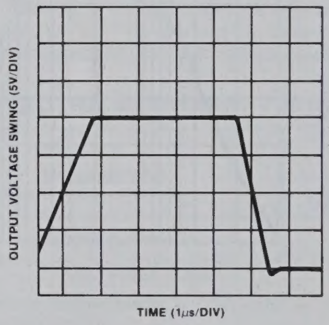
LF356 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



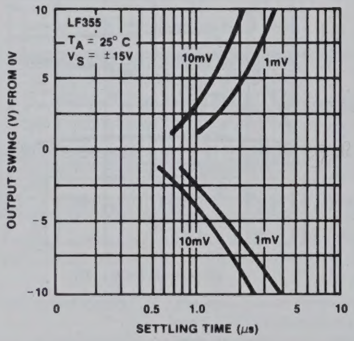
LF355 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



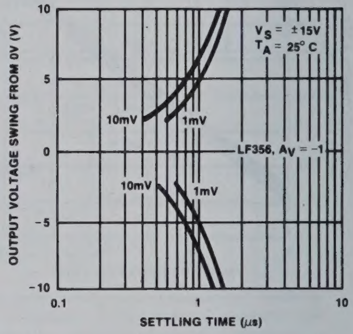
LF356 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



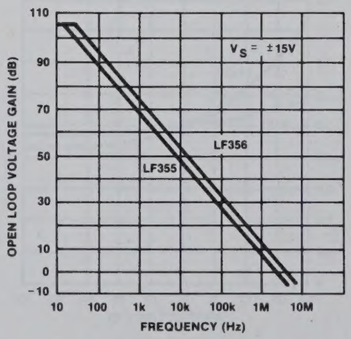
INVERTER SETTLING TIME



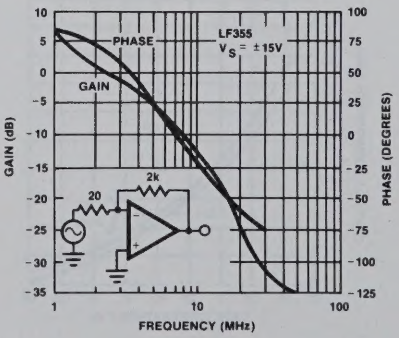
INVERTER SETTLING TIME



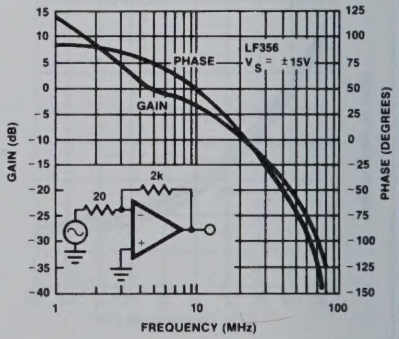
OPEN LOOP FREQUENCY RESPONSE



BODE PLOT

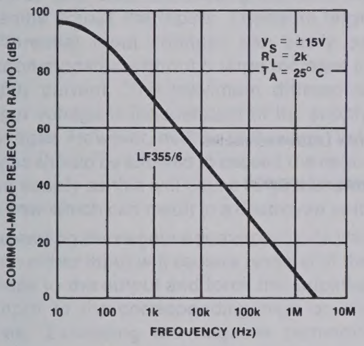


BODE PLOT

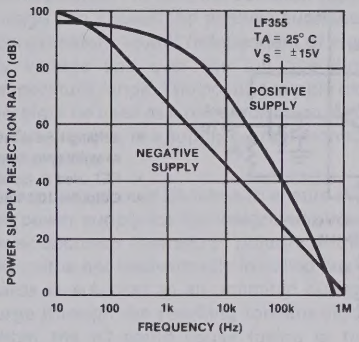


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

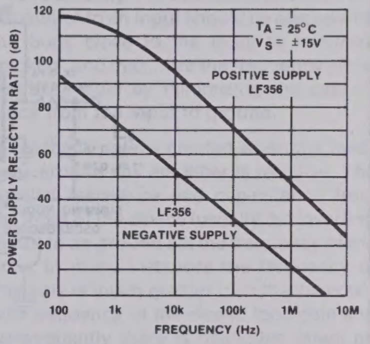
COMMON-MODE REJECTION RATIO



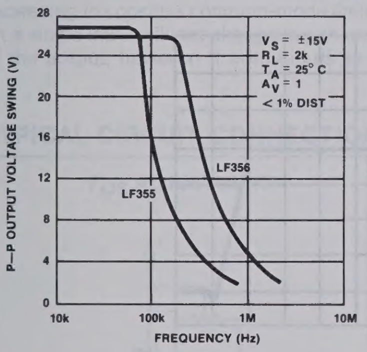
POWER SUPPLY REJECTION RATIO



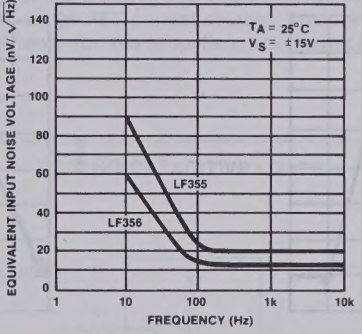
POWER SUPPLY REJECTION RATIO



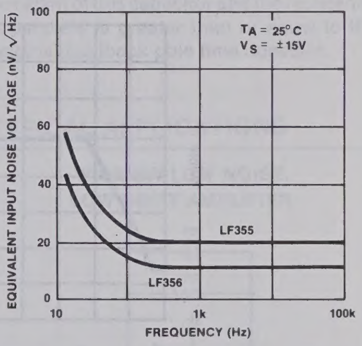
UNDISTORTED OUTPUT VOLTAGE SWING



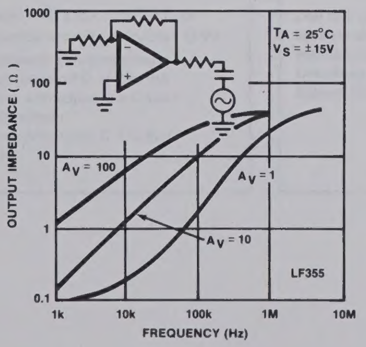
EQUIVALENT INPUT NOISE VOLTAGE



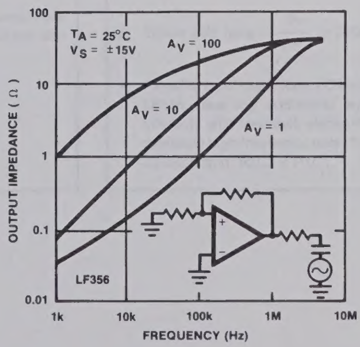
EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)



OUTPUT IMPEDANCE

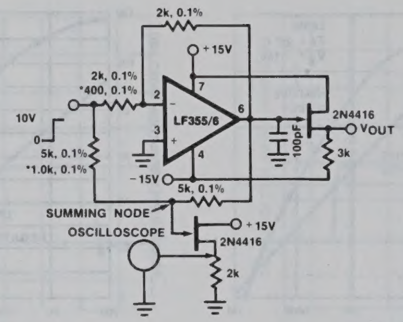


OUTPUT IMPEDANCE



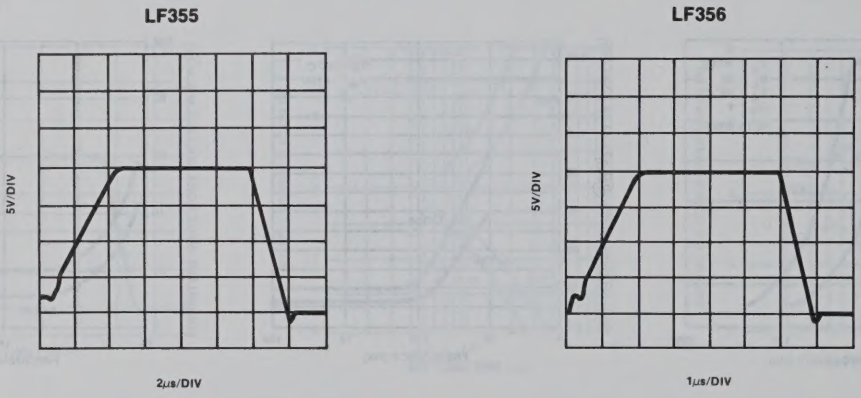
TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

SETTLING TIME TEST CIRCUIT


2k, 0.1%
+15V
2k, 0.1%
*400, 0.1%
10V
0
5k, 0.1%
*1.0k, 0.1%
2
3
7
6
4
LF355/6
2N4416
VOUT
100pF
3k
−15V
5k, 0.1%
SUMMING NODE
OSCILLOSCOPE
+15V
2N4416
2k

- Settling time is tested with the LF355/6 connected as unity gain inverter.
- FET used to isolate the probe capacitance
- Output = 10V step

LARGE SIGNAL INVERTER OUTPUT, V_{OUT} (FROM SETTLING TIME CIRCUIT)



APPLICATIONS

The LF355 and LF356 are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

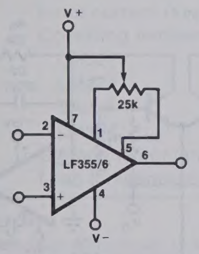
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

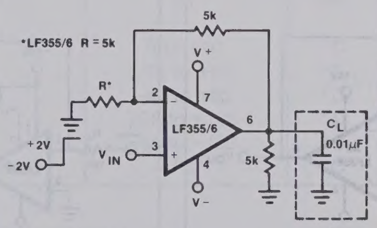
TYPICAL CIRCUIT CONNECTIONS

V_{OS} ADJUSTMENT



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100ppm/°C or less the additional drift with adjust is ≈ 0.5µV/°C/mV of adjustment
- Typical overall drift: 5µV/°C ± (0.5µV/°C/mV of adj.)

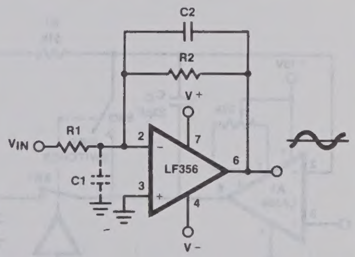
DRIVING CAPACITIVE LOADS



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. C_L max ≤ 0.01µF.
Overshoot ≤ 20%
Setting time (t_S) ≥ 5µs

TYPICAL APPLICATIONS

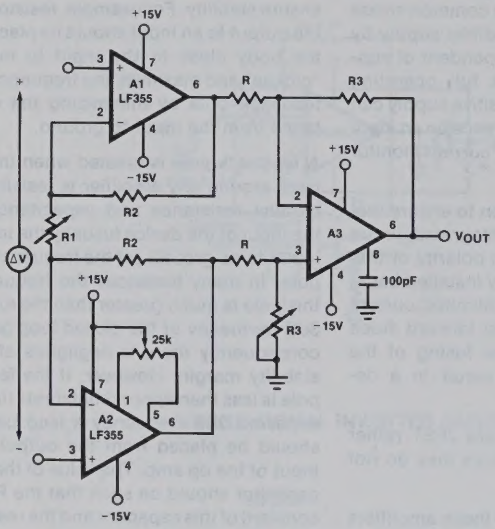
WIDE BW LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{MAX} = \frac{S_r}{2\pi/p} \cong 240\text{kHz}$
- Parasitic input capacitance C1 ≅ (3pF for LF355 and LF356, plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

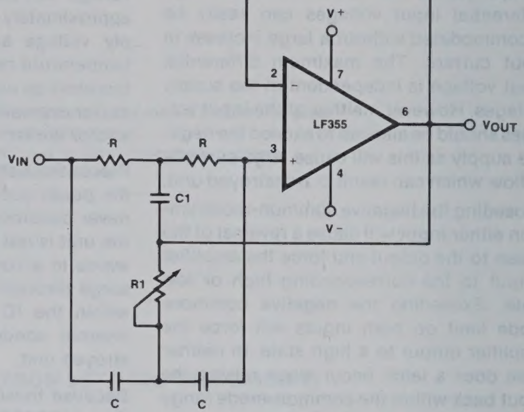
TYPICAL APPLICATIONS (Cont'd)

HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER


+15V
A1
LF355
R
R3
-15V
R2
R1
ΔV
R2
R
+15V
A3
VOUT
100pF
-15V
+15V
25k
R3
A2
LF355
-15V

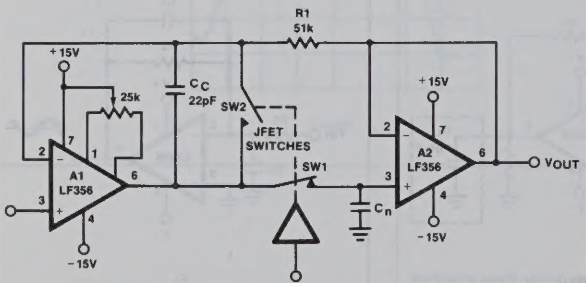
- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V$, $V- +2V \le V_{IN}$ Common-Mode $\le V+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120dB.

HIGH Q NOTCH FILTER


V+
LF355
VOUT
VIN
R
R
C1
V−
R1
C
C

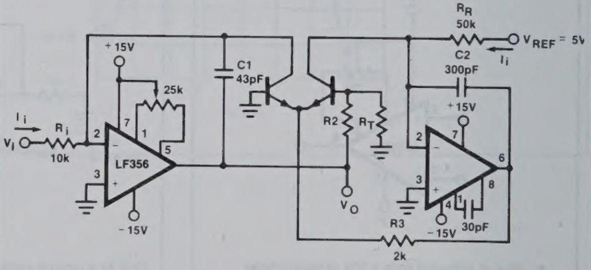
- 2R1 = R = 10MΩ
  2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120Hz, notch = 55dB, Q > 180
- Use LF355 for
  Δ Low I_B
  Δ Low supply current

HIGH ACCURACY SAMPLE AND HOLD


R1
51k
+15V
25k
CC
22pF
SW2
JFET
SWITCHES
SW1
A1
LF356
-15V
+15V
A2
LF356
VOUT
Cn
-15V

- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added on propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold.
- R1, C_C: additional compensation
- Use LF356 for
  Δ Fast settling time
  Δ Low V_{OS}

FAST LOGARITHMIC CONVERTER


RR
50k
VREF = 5V
Ii
C2
300pF
+15V
C1
43pF
25k
Ii
VI
Ri
10k
LF356
-15V
R2
RT
VO
+15V
R3
2k
-15V
30pF

$$|V_{OUT}| = \left[1 + \frac{R2}{R}\right]\frac{kT}{q} \ln V_I \left[\frac{R_r}{V_{REF} R_i}\right] = \log V_I \frac{1}{R_i I_R}$$

R2 = 15.71, R_1 = 1k, 0.3%°C (for temperature compensation)

- Dynamic range: $100\mu A \le I_i \le 1mA$ (5 decades, $|V_O|$ = 1V/decades)
- Transient response: $3\mu s$ for Δ, = decades
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF356 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C.

GENERAL PURPOSE SINGLE SUPPLY OPERATIONAL AMPLIFIER

LM124/224/324/SA534

LM124/224/324/SA534-F,N
LM324-D

DESCRIPTION

The LM124/SA534 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated.

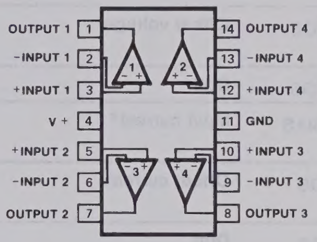
The input bias current is also temperature compensated.

FEATURES

- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  Single supply—(3Vdc to 30Vdc) or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nAdc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nAdc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—1.5Vdc swing)**
- **LM124 Mil std 883A,B,C available**

PIN CONFIGURATION

D,F,N PACKAGE



ORDER PART NO.

LM124N	LM224N	LM324N
LM124F	LM224F	LM324F
SA534N	SA534F	LM324D

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V+	Supply voltage	32 or ±16	Vdc
	Differential input voltage	32	Vdc
	Input voltage	-0.3 to +32	Vdc
	Power dissipation[1]		
	N package	570	mW
	F package	900	mW
	Output short-circuit to GND		
	1 amplifier[2]	Continuous	
	V+ < 15Vdc and $T_A = 25°C$		
	Input current ($V_{IN} < -0.3V$)[3]	50	mA
	Operating temperature range		
	LM324	0 to +70	°C
	LM224	-25 to +85	°C
	SA534	-40 to +85	°C
	LM124	-55 to +125	°C
	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. LM 124/224 can be derated based on a +150°C maximum junction temperature.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

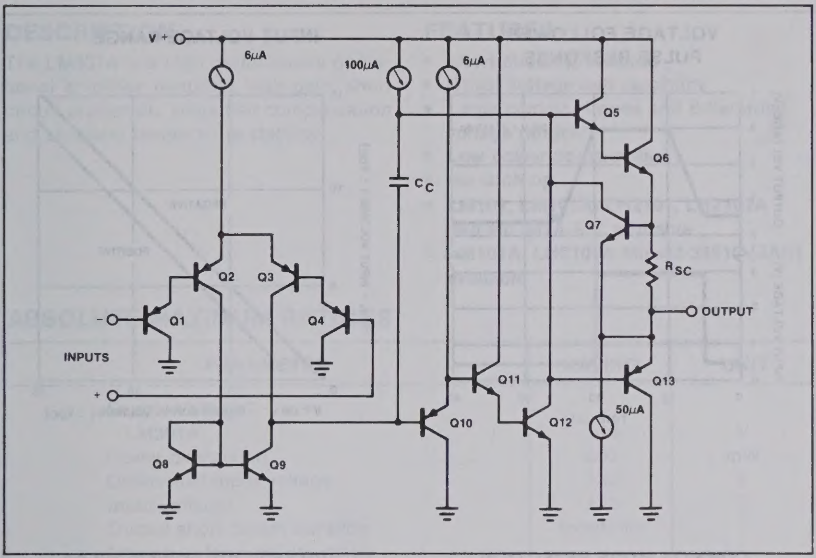
DC ELECTRICAL CHARACTERISTICS $V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$ $R_S = 0\Omega$, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	$R_S = 0\Omega$		7			7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$ $I_{IN}(+)$ or $I_{IN}(-)$, over temp.		45 40	150 300		45 40	250 500	nA nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$ $I_{IN}(+) - I_{IN}(-)$, over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift			10			10		pA/°C
V_{CM}	Common mode voltage range[3]	$V+ = 30V$ $V+ = 30V$, over temp.	0 0		V+−1.5 V+−2	0 0		V+−1.5 V+−2	V V
C_{MRR}	Common mode rejection ratio		70	85		65	70		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V+ = +30V$, over temp.	26			26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp.	27	28		27	28		V
V_{OL}		$R_L \leq 10k\Omega$, $V+ = 5V$, over temp.		5	20		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp. $R_L = \infty$, on all op amps, over temp.		1.5 0.7	3 1.2		1.5 0.7	3 1.2	mA
A_{VOL}	Large signal voltage gain	$V+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$ $V+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	50 25	100		25 15	100		V/mV V/mV
	Amplifier-to-amplifier coupling[5]	f = 1kHz to 20kHz, input referred		−120			−120		dB
P_{SRR}		$R_S \leq 0\Omega$	65	100		65	100		dB
	Output current Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$, over temp.	10	20		10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$, over temp.	5	8		5	8		mA
		$V_{IN}+ = 0Vdc$, $V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short circuit current[4]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V

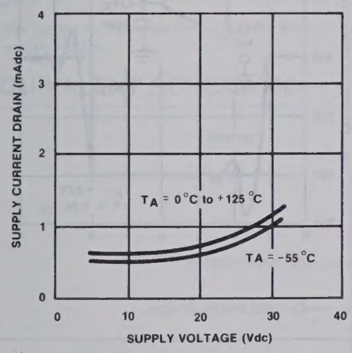
NOTES

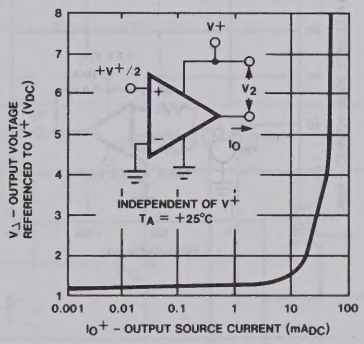
1. $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (0Vdc+ to V+ −1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32Vdc without damage.

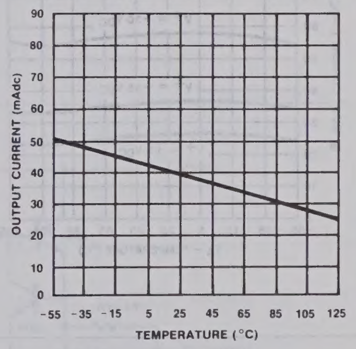
EQUIVALENT SCHEMATIC

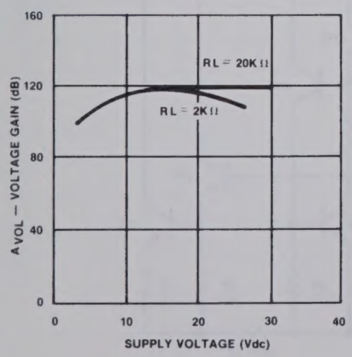

V+
6μA
100μA
6μA
Q5
Q6
CC
Q7
RSC
OUTPUT
Q2
Q3
Q1
Q4
INPUTS
+
Q11
Q13
50μA
Q10
Q12
Q8
Q9

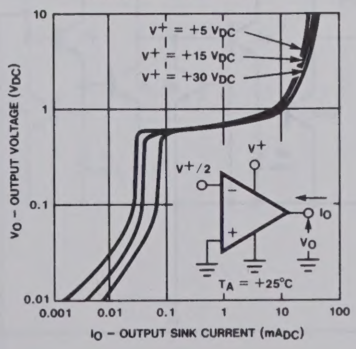
TYPICAL PERFORMANCE CHARACTERISTICS

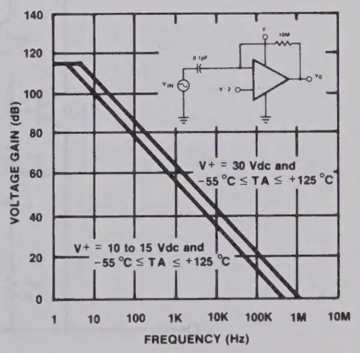

SUPPLY CURRENT


OUTPUT CHARACTERISTICS CURRENT SOURCING

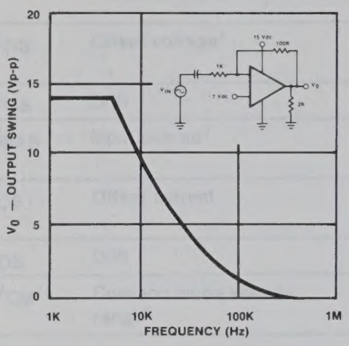

CURRENT LIMITING

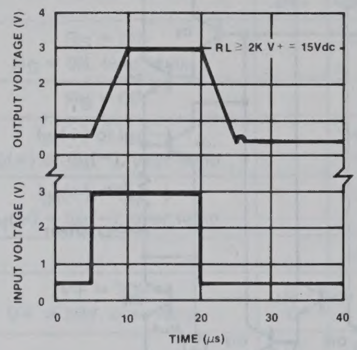

VOLTAGE GAIN

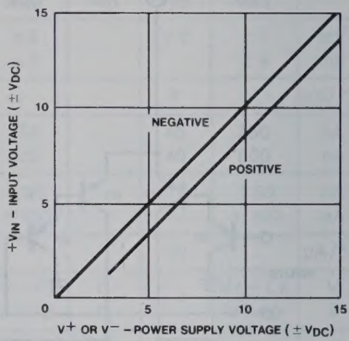

OUTPUT CHARACTERISTICS CURRENT SINKING

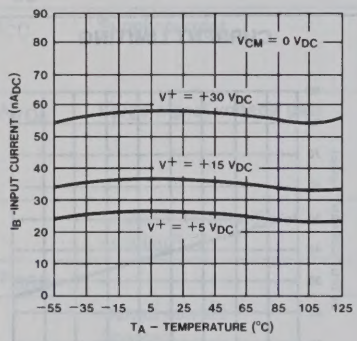

OPEN LOOP FREQUENCY RESPONSE

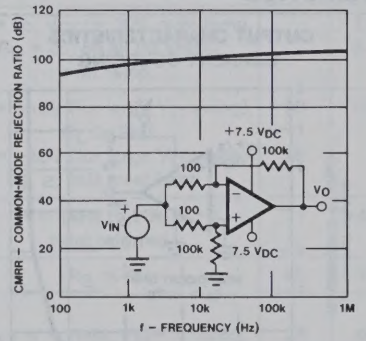
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

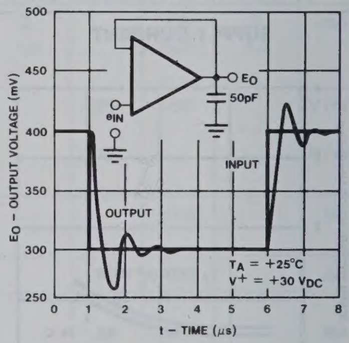

LARGE SIGNAL FREQUENCY RESPONSE


VOLTAGE FOLLOWER PULSE RESPONSE


INPUT VOLTAGE RANGE


INPUT CURRENT


COMMON MODE REJECTION RATIO


VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

HIGH PERFORMANCE AMPLIFIER LM301A

LM301A-N,FE,D

DESCRIPTION

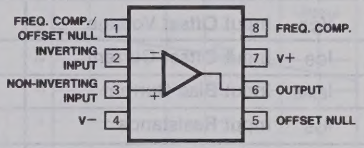
The LM301A is a high performance operational amplifier featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- **Short circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch up**
- **LM101, LM101A, LH2101, LH2101A Mil std 883A,B,C available**
- **LM101A, LH2101A Mil std 38510 (JAN) available**

PIN CONFIGURATIONS

D,N,FE PACKAGE


FREQ. COMP./ OFFSET NULL
1
INVERTING INPUT
2
−
NON-INVERTING INPUT
3
+
V−
4
8
FREQ. COMP.
7
V+
6
OUTPUT
5
OFFSET NULL

ORDER PART NO.

LM301AN
LM301AFE
LM301AD

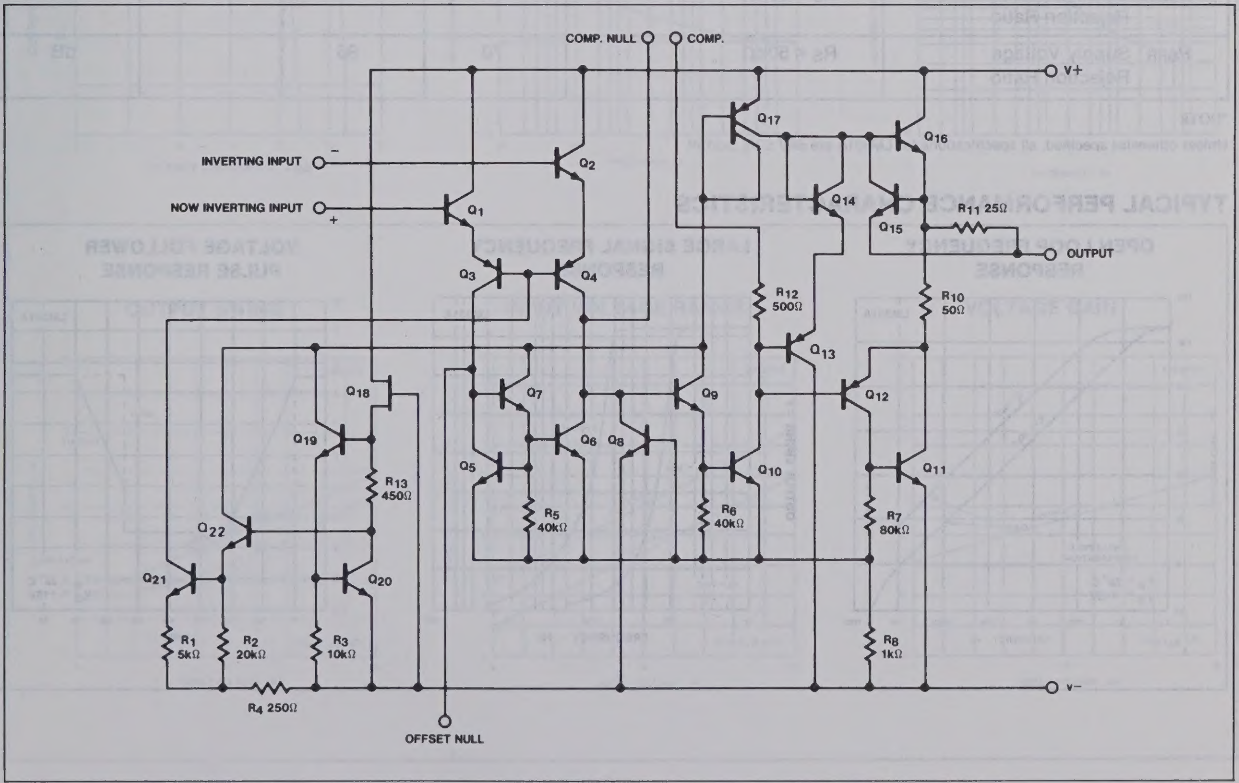
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage		
LM301A	±18	V
Power dissipation	500	mW
Differential input voltage	±30	V
Input voltage[1]	±15	V
Output short circuit duration	Indefinite	
Operating temperature range		
LM301A	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. For supply voltages less then ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC


COMP. NULL
COMP.
V+
INVERTING INPUT
−
NOW INVERTING INPUT
+
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
R1 5kΩ
R2 20kΩ
R3 10kΩ
R4 250Ω
R5 40kΩ
R6 40kΩ
R7 80kΩ
R8 1kΩ
R10 50Ω
R11 25Ω
R12 500Ω
R13 450Ω
OUTPUT
V−
OFFSET NULL

LM301A-N,FE,D

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A < 70°C$, $\pm 5V, \le V_S \le \pm 15V$ and $C_1 = 30pF$

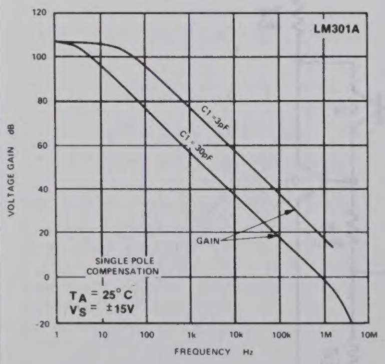
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	$T_A = 25°C$, $R_S < 50K\Omega$		2.0	7.5	mV
I_{OS}	Input Offset Current	$T_A = 25°C$		3	50	nA
I_{BIAS}	Input Bias Current	$T_A = 25°C$		70	250	nA
I_{OS}	Input Resistance	$T_A = 25°C$	0.5	2		MΩ
I_{CC}	Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	3.0	mA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$; $R_L > 2k\Omega$	25	160		V/mV
V_{OS}	Input Offset Voltage	$R_S < 50k\Omega$			10	mV
V_{OS}	Average Temperature Coefficient of Input Drift Offset Voltage			6.0	30	µV/°C
I_{OS}	Input Offset Current				70	nA
I_{OS}	Average Temperature Coefficient of Input Offset Current	$25°C < T_A < 70°C$ $0°C < T_A < 25°C$		0.01 0.02	0.3 0.6	nA/°C nA/°C
I_{BIAS}	Input Bias Current				300	nA
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L > 2k\Omega$	15			V/mV
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
V_{IN}	Input Voltage Range	$V_S = \pm 15V$	±12			V
C_{MRR}	Common Mode Rejection Ratio	$R_S < 50k\Omega$	70	90		dB
P_{SRR}	Supply Voltage Rejection Ratio	$R_S < 50k\Omega$	70	96		dB

*NOTE

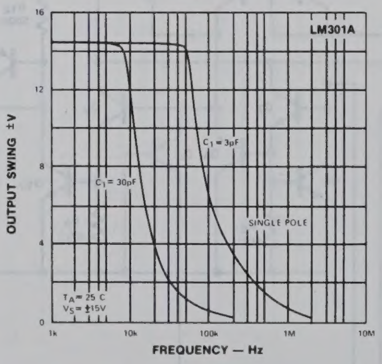
Unless otherwise specified, all specifications for LM301A are $\pm 5V \le V_S \le \pm 15V$.

TYPICAL PERFORMANCE CHARACTERISTICS

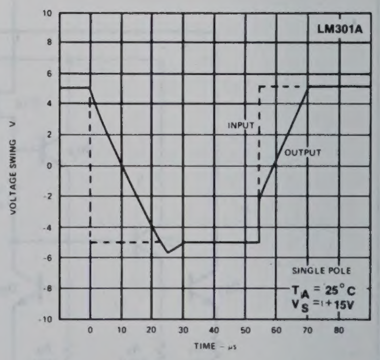
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

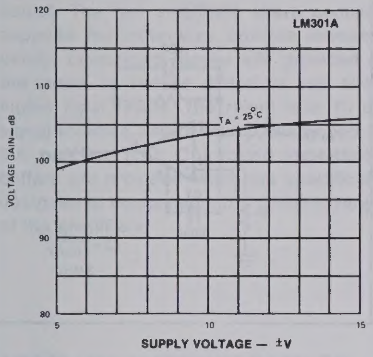


VOLTAGE FOLLOWER PULSE RESPONSE

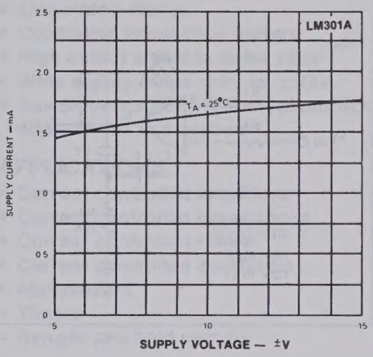


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

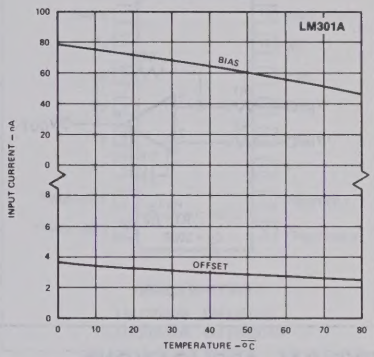
VOLTAGE GAIN



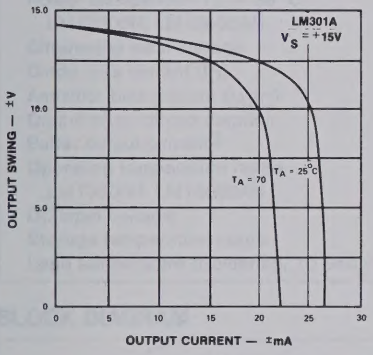
SUPPLY CURRENT



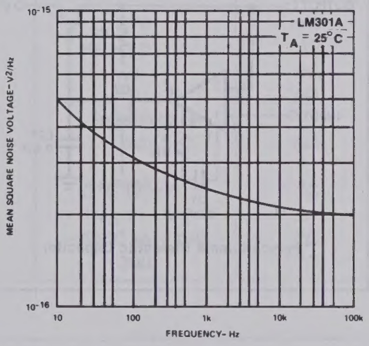
INPUT CURRENT



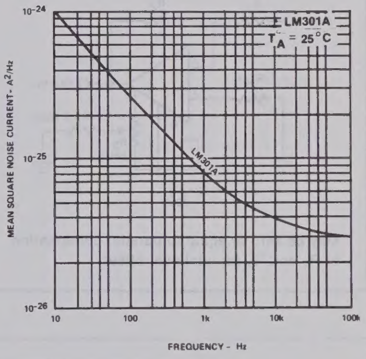
CURRENT LIMITING



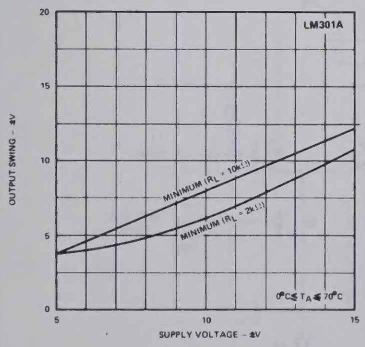
INPUT NOISE VOLTAGE



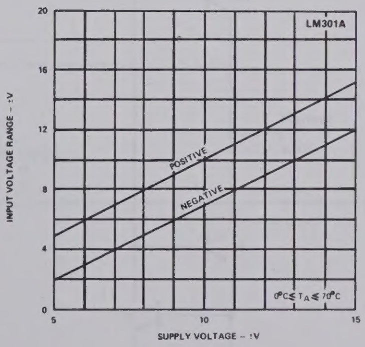
INPUT NOISE CURRENT



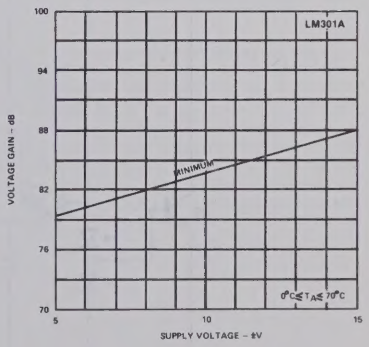
OUTPUT SWING



INPUT VOLTAGE RANGE

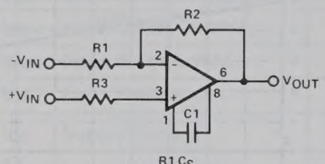


VOLTAGE GAIN



COMPENSATION CIRCUITS

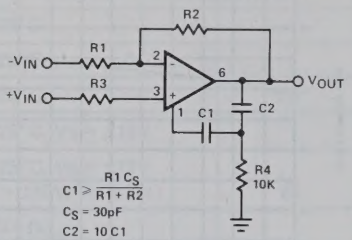
SINGLE POLE COMPENSATION


R2
R1
-VIN
2
6
VOUT
R3
+VIN
3
8
1
C1

$C1 \geq \frac{R1\,C_S}{R1 + R2}$

$C_S = 30pF$

TWO POLE COMPENSATION

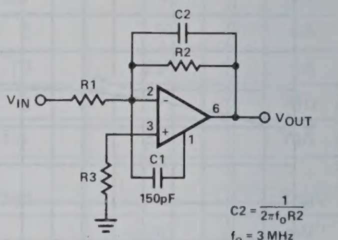

R2
R1
-VIN
2
6
VOUT
R3
+VIN
3
1
C1
C2
R4
10K

$C1 \geq \frac{R1\,C_S}{R1 + R2}$

$C_S = 30pF$

$C2 = 10\,C1$

FEED FORWARD COMPENSATION

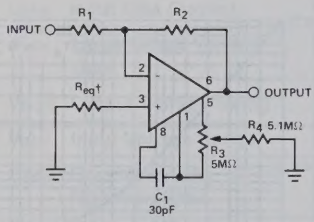

C2
R2
R1
VIN
2
6
VOUT
3
1
C1
R3
150pF

$C2 = \frac{1}{2\pi f_o R2}$

$f_o = 3\,MHz$

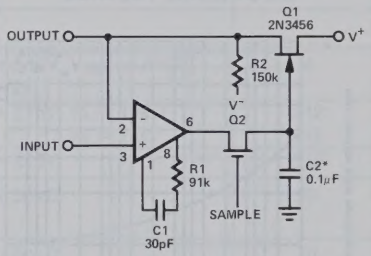
TYPICAL APPLICATIONS

INVERTING AMPLIFIER WITH BALANCING CIRCUIT


R1
R2
INPUT
2
6
OUTPUT
Req†
3
5
1
8
R4 5.1MΩ
R3
5MΩ
C1
30pF

†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

LOW DRIFT SAMPLE AND HOLD


Q1
2N3456
OUTPUT
V+
R2
150k
V−
Q2
2
6
INPUT
3
8
1
R1
91k
C2*
0.1μF
SAMPLE
C1
30pF

*Polycarbonate Dielectric Capacitor

DESCRIPTION

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are specifically designed to complement the dynamic range of the amplifiers.

FEATURES

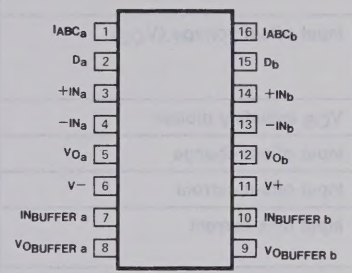
- **gm adjustable over 6 decades**
- **Excellent gm linearity**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **Controlled impedance buffers**
- **High output signal to noise ratio**
- **Wide supply range ±2V to ±22V.**
- **See Signetics NE5517 for typical circuit applications information**

APPLICATIONS

- **Current controlled amplifiers**
- **Current controlled impedances**
- **Current controlled filters**
- **Current controlled oscillators**
- **Multiplexers**
- **Timers**
- **Sample and hold circuits**

PIN DESCRIPTION

D,N PACKAGE


I_{ABCa} 1
D_a 2
$+IN_a$ 3
$-IN_a$ 4
V_{Oa} 5
V− 6
$IN_{BUFFER\ a}$ 7
$VO_{BUFFER\ a}$ 8
16 I_{ABCb}
15 D_b
14 $+IN_b$
13 $-IN_b$
12 V_{Ob}
11 V+
10 $IN_{BUFFER\ b}$
9 $VO_{BUFFER\ b}$

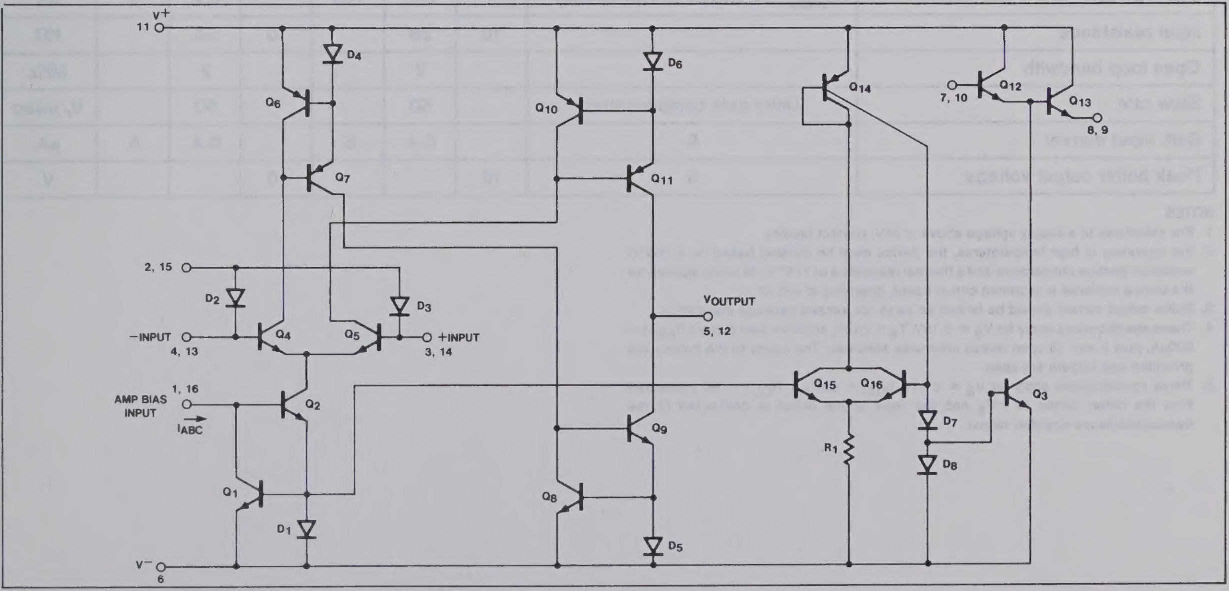
ORDER PART NO.

LM13600N LM13600D
LM13600AN LM13600AD

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage[1]		
LM13600	36 V_{DC} or ±18	V
LM13600A	44 V_{DC} or ±22	V
Power dissipation[2] $T_A = 25°C$		
LM13600N, LM13600AN	570	mW
Differential input voltage	±5	V
Diode bias current (I_D)	2	mA
Amplifier bias current (I_{ABC})	2	mA
Output short circuit duration	Indefinite	
Buffer output current[3]	20	mA
Operating temperature range		
LM13600N, LM13600AN	0°C to +70	°C
DC input voltage	$+V_S$ to $-V_S$	
Storage temperature range	−65°C to +150	°C
Lead temperature (Soldering, 10 Seconds)	300	°C

BLOCK DIAGRAM


V+
11
D4
Q6
Q7
Q10
D6
Q11
Q14
7, 10
Q12
Q13
8, 9
2, 15
D2
D3
V_{OUTPUT}
5, 12
−INPUT
4, 13
Q4
Q5
+INPUT
3, 14
AMP BIAS INPUT
1, 16
I_{ABC}
Q2
Q15
Q16
Q3
D7
D8
R1
Q9
Q1
D1
Q8
D5
V−
6

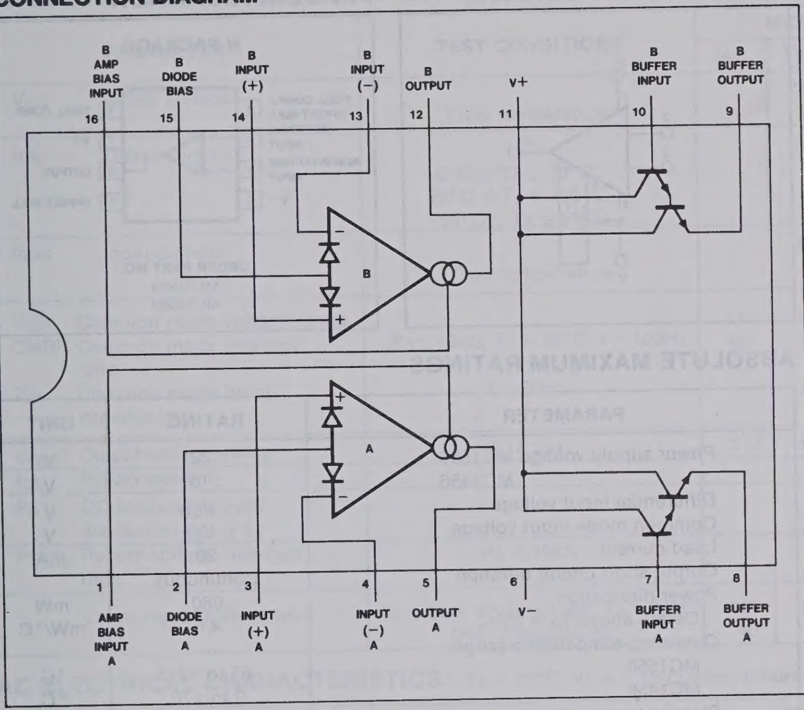
ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LM13600 Min	LM13600 Typ	LM13600 Max	LM13600A Min	LM13600A Typ	LM13600A Max	UNIT
Input offset voltage (V_{OS})			0.4	5		0.4	2	mV
	Over specified temperature range						5	mV
	I_{ABC} 5μA		0.3	5		0.3	2	mV
V_{OS} including diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input offset change	5 μA $\leq I_{ABC} \leq$ 500 μA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
Input bias current			0.4	5		0.4	5	μA
	Over specified temperature range		1	8		1	7	μA
Forward Transconductance (gm)		6700	9600	13000	7700	9600	12000	μmho
	Over specified temperature range	5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I_{ABC} = 5μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	RL = 0, Over specified temp range	300			300			μA
Peak output voltage								
positive	RL = ∞, 5 μA $\leq I_{ABC} \leq$ 500 μA	+12	+14.2		+12	+14.2		V
negative	RL = ∞, 5 μA $\leq I_{ABC} \leq$ 500 μA	−12	−14.4		−12	−14.4		V
Supply current	I_{ABC} = 500 μA, Both channels		2.6			2.6		mA
V_{OS} sensitivity								
positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input[5] 20 Hz < f < 20 KHz		100			100		dB
Diff. input current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwith			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V

NOTES

1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.
4. These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for $V_S = \pm 15V$, I_{ABC} = 500 μA, R_{OUT} = 5Ω connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

CONNECTION DIAGRAM


B AMP BIAS INPUT
16
B DIODE BIAS
15
B INPUT (+)
14
B INPUT (−)
13
B OUTPUT
12
V+
11
B BUFFER INPUT
10
B BUFFER OUTPUT
9
B
A
1
AMP BIAS INPUT A
2
DIODE BIAS A
3
INPUT (+) A
4
INPUT (−) A
5
OUTPUT A
6
V−
7
BUFFER INPUT A
8
BUFFER OUTPUT A

HIGH PERFORMANCE OPERATIONAL AMPLIFIER MC1456/1556

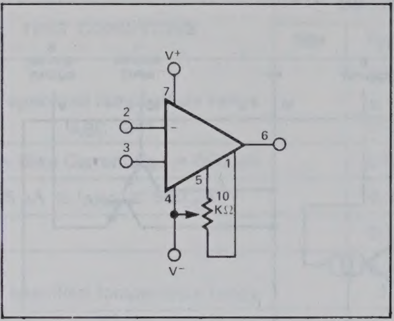
DESCRIPTION

The MC1456/1556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The MC1456/1556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

FEATURES

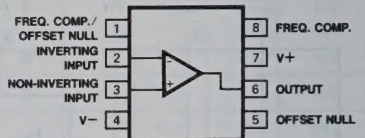
- **Low input bias current—15nA maximum**
- **Low input offset current—2.0nA maximum**
- **Low input offset voltage—4.0mV maximum**
- **High slew rate—2.5V/μs typical**
- **Large power bandwidth—40kHz typical**
- **Low power consumption—45mW maximum**
- **Offset voltage null capability**
- **Output short circuit protection**
- **Input over-voltage protection**
- **Mil std 883A,B,C, available**

OFFSET ADJUST CIRCUIT


V+
7
2
3
−
+
6
5
1
4
10 KΩ
V−

PIN CONFIGURATION

N PACKAGE

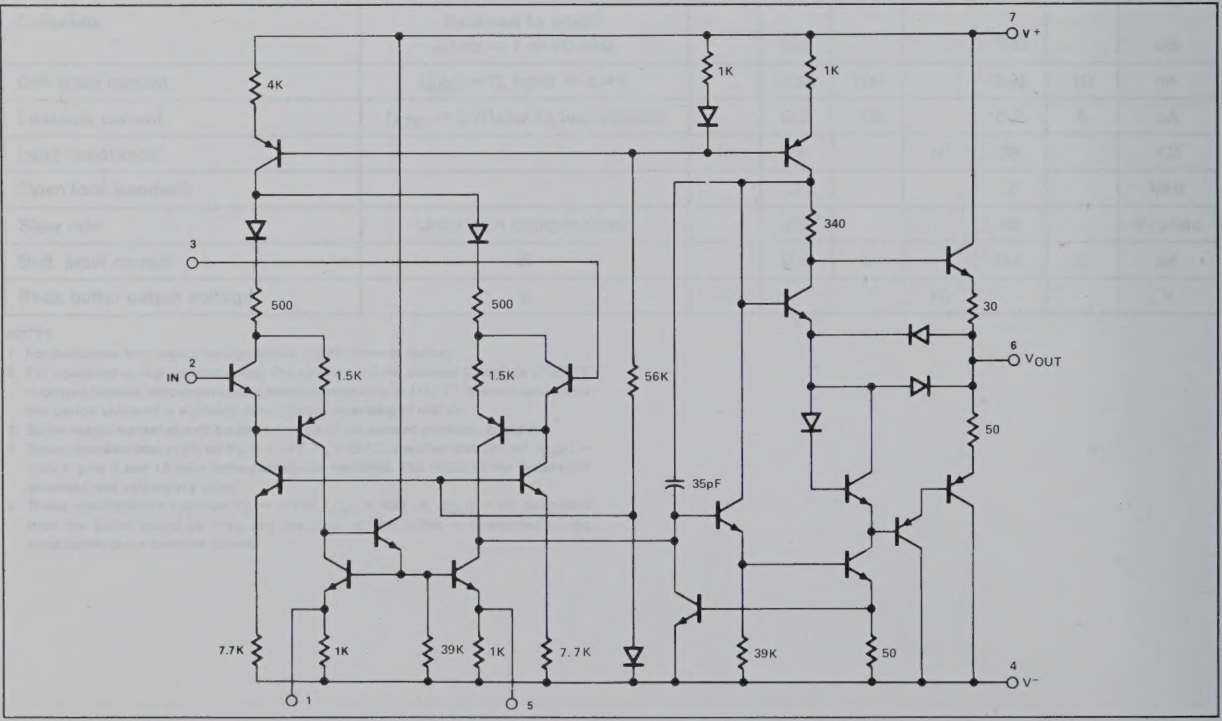

FREQ. COMP./ OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V− 4
8 FREQ. COMP.
7 V+
6 OUTPUT
5 OFFSET NULL
−
+

ORDER PART NO.
MC1456N
MC1556N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage MC1556	±22	V
MC1456	±18	V
Differential input voltage	$\pm V_{CC}$	V
Common mode input voltage	$\pm V_{CC}$	V
Load current	20	mA
Output short circuit duration	Continuous	
Power dissipation	680	mW
Derate above $T_A = 25°C$	4.6	mW/°C
Operating temperature range		
MC1556	-55 to +125	°C
MC1456	0 to +70	°C
Storage temperature range	-65 to +150	°C

EQUIVALENT SCHEMATIC


7
V+
4K
1K
1K
340
3
500
500
30
2
IN
1.5K
1.5K
56K
6
VOUT
50
35pF
7.7K
1K
39K
1K
7.7K
39K
50
4
V−
1
5

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified

PARAMETER		TEST CONDITIONS	MC1556			MC1456			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			2.0	4.0		5.0	10.0	mVdc
		Over temperature			6.0			14.0	mVdc
I_{OS}	Offset current			1.0	2.0		5.0	10.0	nA
		$0°C \leq T_A \leq 70°C$						14	nA
		$25°C \leq T_A \leq 125°C$			3.0				nA
		$-55°C \leq T_A \leq 25°C$			5.0				nA
I_{BIAS}	Input current			8.0	15		15.0	30.0	nA
		Over temperature			30			40	nA
V_{CM}	Common mode voltage range		±12	±13		±11	±12		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$, $f = 100Hz$	80	110		70	110		dB
Z_{IN}	Common mode input impedance	f = 20Hz		250			250		MΩ
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$	±12	±13		±11	±12		V
I_{CC}	Supply current			1.0	1.5		1.3	3.0	mA
P_D	DC quiescent power dissipation ($V_O = 0$)			30	45		40	90	mW
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		50	100		75	200	μV/V
	Large signal voltage gain	$R_L \leq 2k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$	100	200		70	100		V/mV
		Over temperature	40			40			V/mV

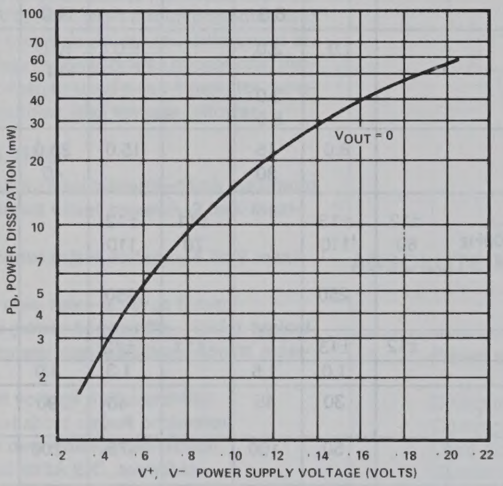
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

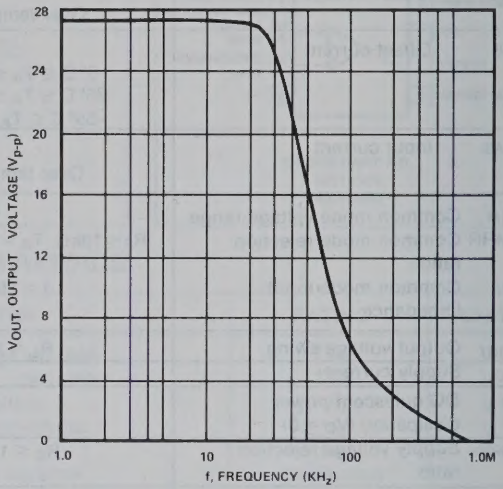
PARAMETER		TEST CONDITIONS	MC1556			MC1456			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential input impedance								
c_p	Parallel input capacitance	Open loop f = 20Hz		6.0			6.0		pF
r_p	Parallel input resistance			5			3		MΩ
e_n	Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $f = 1.0kHz$, BW = 1.0kHz		45			45		$nV/\sqrt{Hz}$
BW_p	Power bandwidth	$A_V = 1$, $R_L = 2k\Omega$, THD ≤ 5% $V_{OUT} = \pm 10V$		40			40		kHz
	Phase margin (open loop, unity gain)			70			70		degrees
	Gain margin			18			18		dB
S_R	Slew rate (unity gain)			2.5			2.5		V/μsec
Z_{OUT}	Output impedance	f = 20Hz		1.0	2.0		1.0	2.5	kΩ
BW	Unity gain crossover frequency (open loop)			1.0			1.0		MHz

TYPICAL PERFORMANCE CHARACTERISTICS

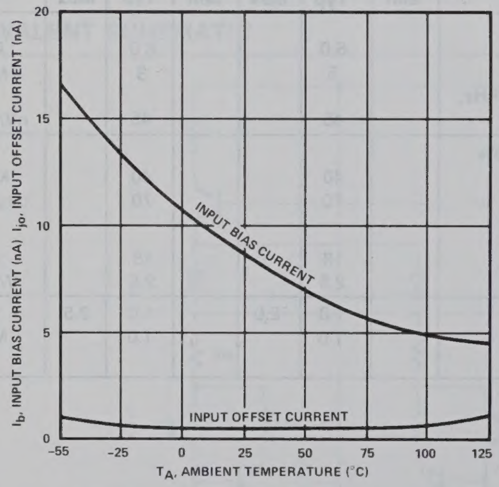
POWER DISSIPATION vs POWER SUPPLY VOLTAGE



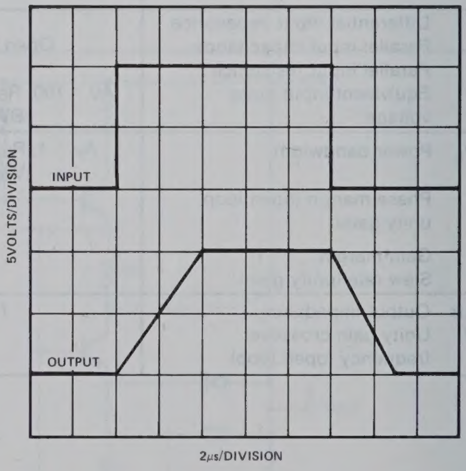
POWER BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE FOR MC1556



VOLTAGE FOLLOWER PULSE RESPONSE



MC1458/1558-N,H,FE,F
SA1458-N
MC1458-D

DESCRIPTION

The MC1458 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The MC1458 is short-circuit protected and allows for nulling of offset voltage.

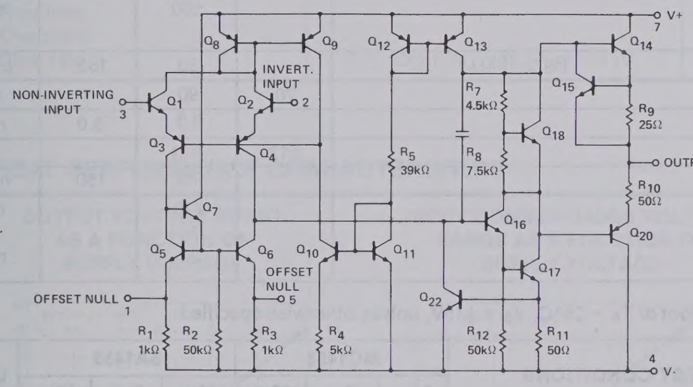
The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**
- **MC1558 Mil std 883A,B,C available**

EQUIVALENT SCHEMATIC

ONE AMPLIFIER OF MC1458, SA1458, MC1558


V+
7
Q8
Q9
Q12
Q13
Q14
INVERT. INPUT
2
NON-INVERTING INPUT
3
Q1
Q2
Q15
R7 4.5kΩ
R9 25Ω
Q3
Q4
Q18
R5 39kΩ
R8 7.5kΩ
OUTPUT
R10 50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
OFFSET NULL
5
Q17
OFFSET NULL
1
Q22
R1 1kΩ
R2 50kΩ
R3 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
4
V-

ABSOLUTE MAXIMUM RATINGS

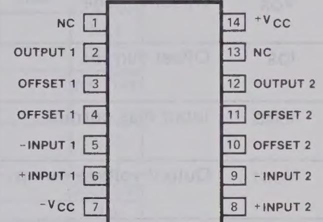
PARAMETER	RATING	UNIT
Supply voltage		
MC1458	±18	V
SA1458	±18	V
MC1558	±22	V
Internal power dissipation		
N package	500	mW
H package[1]	800	mW
F,FE package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
MC1458	0 to +70	°C
SA1458	-40 to +85	°C
MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Ratings based on thermal resistances, junction to ambient, of 240°C/W, 150°C/W, 110°C/W for N, H, F and FE packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

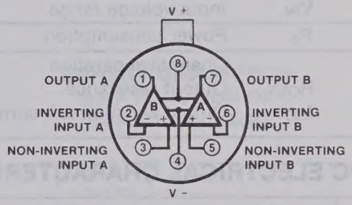
PIN CONFIGURATIONS

F PACKAGE


NC 1
OUTPUT 1 2
OFFSET 1 3
OFFSET 1 4
-INPUT 1 5
+INPUT 1 6
-VCC 7
14 +VCC
13 NC
12 OUTPUT 2
11 OFFSET 2
10 OFFSET 2
9 -INPUT 2
8 +INPUT 2

ORDER PART NO.
MC1458F
MC1558F

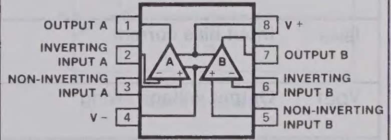
H PACKAGE*


V +
OUTPUT A
1
8
7
OUTPUT B
INVERTING INPUT A
2
B
A
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
4
5
NON-INVERTING INPUT B
V -

ORDER PART NO.
MC1458H
MC1558H

*Metal cans (H) not recommended for new designs

D,N,FE PACKAGE


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
V - 4
A
B
8 V +
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B

ORDER PART NO.

MC1458N	MC1458FE
MC1558N	MC1558FE
SA1458N	MC1458D

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	R_S = 10kΩ R_S = 10kΩ, over temp.		1.0	5.0 6.0	mV mV
I_{OS}	Offset current	 Over temp.		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 1500	nA nA
V_{OUT}	Output voltage swing	R_L = 10kΩ, over temp. R_L = 2kΩ, over temp.	±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	R_L = 2kΩ, V_O = ±10V R_L = 2kΩ, V_O = ±10V, over temp.	50 25	100		V/mV V/mV
	Offset voltage adjustment range			±30		mV
P_{SRR}	Supply voltage rejection ratio	R_S ≤ 10kΩ		30	150	μV/V
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		±12	±13		V
P_d	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

DC ELECTRICAL CHARACTERISTICS

(Cont'd) T_A = 25°C, V_S = ±15V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S = 10kΩ R_S = 10kΩ, over temp.		2.0	6.0 7.5		2.0	6.0 7.5	mV mV
I_{OS}	Offset current	 Over temp.		20	200 300		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 800		80	500 1500	nA nA
V_{OUT}	Output voltage swing	R_L = 10kΩ R_L = 2kΩ, over temp.	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	R_L = 2kΩ, V_O = ±10V R_L = 2kΩ, V_O = ±10V, over temp.	25 15	200		20 15	200		V/mV V/mV
	Offset voltage adjustment range			±30			±30		mV
P_{SRR}	Supply voltage rejection ratio	R_S ≤ 10kΩ		30	150		30	150	μV/V
CMRR	Common mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		±12	±13		±12	±13		V
R_{IN}	Input resistance								MΩ
P_d	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

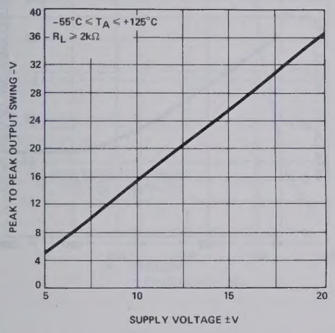
MC1458/1558-N,H,FE,F
SA1458-N
MC1458-D

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

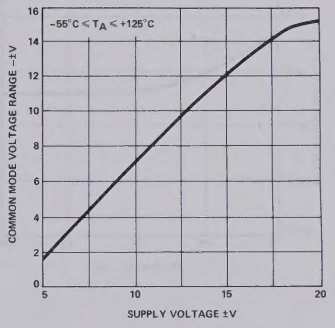
PARAMETER	TEST CONDITIONS	MC1458 SA1458, MC1558 Min	Typ	Max	UNIT
Parallel input resistance	Open loop, f = 20Hz	0.3			MΩ
Common mode input impedance	f = 20Hz		200		MΩ
Equivalent input noise voltage	$A_V = 100$, $R_S = 10kΩ$, $B_W = 1.0kHz$ f = 1.0kHz		45		$nV\sqrt{Hz}$
Power bandwidth	$A_V = 1$, $R_L = 2.0kΩ$, THD ≤ 5% $V_{OUT} = 20Vp\text{-}p$		14		kHz
Phase margin			65		degrees
Gain margin			11		dB
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2kΩ$, $C_L ≤ 100pf$				
Rise time			0.3		μs
Overshoot			5.0		%
Slew rate	$C ≤ 100pf$, $R_L ≥ 2k$, $V_{IN} = ±10V$		0.8		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

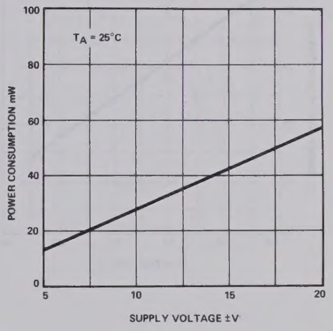
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



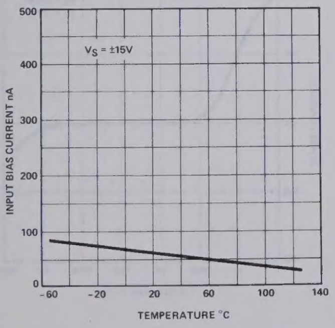
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



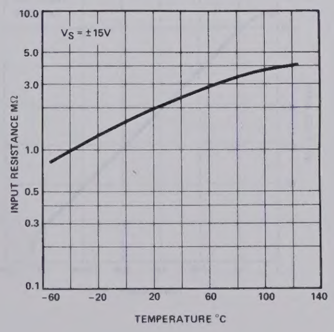
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



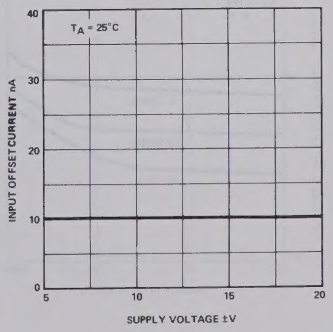
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



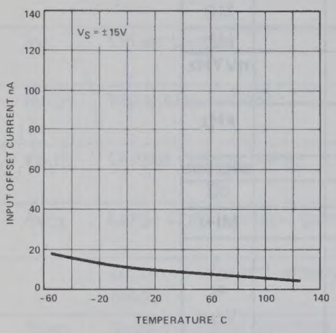
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



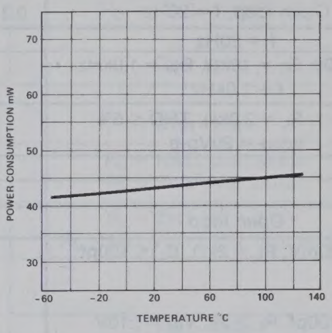
MC1458/1558-N,H,FE,F
SA1458-N
MC1458-D

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

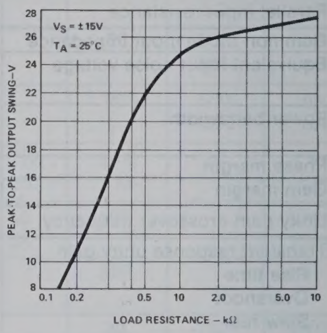
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



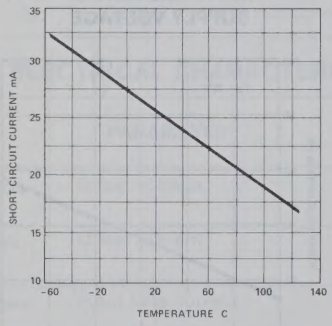
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



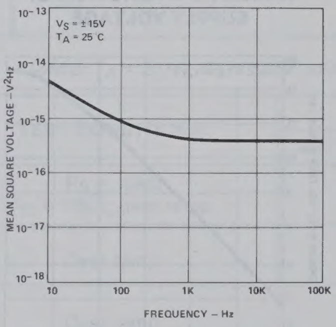
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



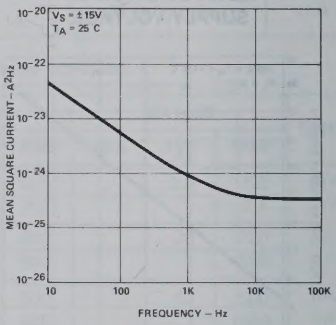
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



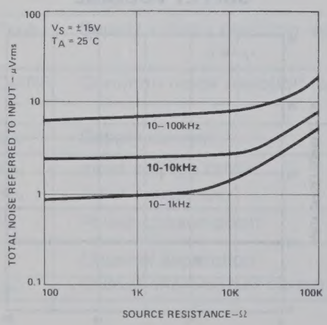
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



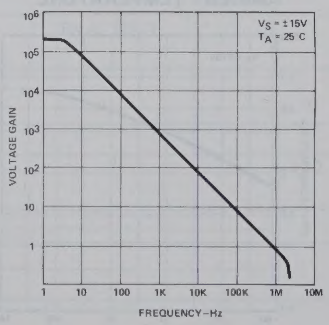
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



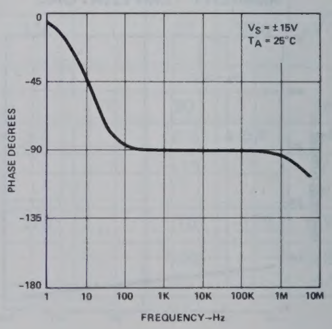
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



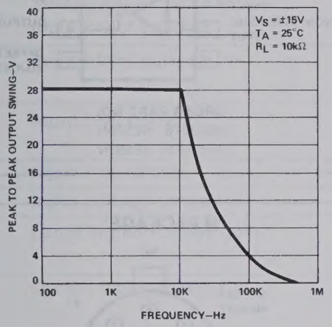
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



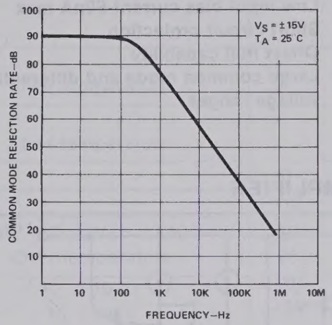
MC1458/1558-N,H,FE,F
SA1458-N
MC1458-D

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

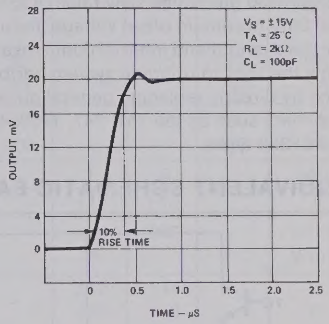
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



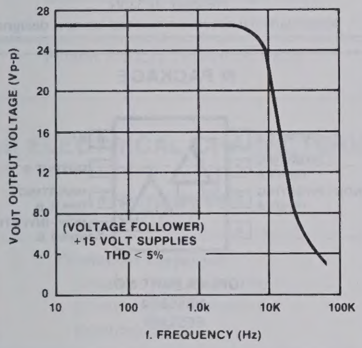
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



NE / SE530-FE,N,H • NE / SE5530-H,N

DESCRIPTION

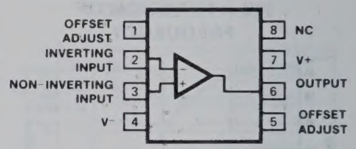
The 530/5530 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated, the SE530/5530 guarantee slew rates of 25V/μs with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741, 747, 1458, 4558 and LF356 types.

FEATURES

- **Gain bandwidth product—3MHz**
- **35V/μs slew rate (Gain = -1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV max**
- **Low input bias current-60nA max**
- **Short circuit protection**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

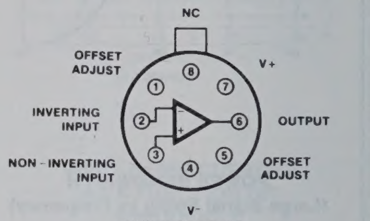
PIN CONFIGURATIONS

FE,N PACKAGE


OFFSET ADJUST
INVERTING INPUT
NON-INVERTING INPUT
V-
1
2
3
4
8
7
6
5
NC
V+
OUTPUT
OFFSET ADJUST

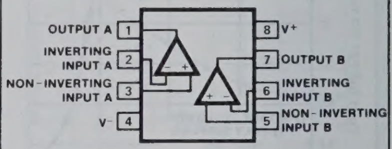
ORDER PART NO.
NE530FE, NE530N
SE530FE, SE530N

H PACKAGE*


NC
OFFSET ADJUST
V+
INVERTING INPUT
OUTPUT
NON-INVERTING INPUT
OFFSET ADJUST
V-
①
②
③
④
⑤
⑥
⑦
⑧

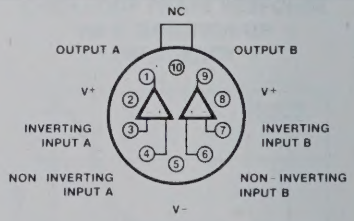
ORDER PART NO.
NE530H SE530H
*Metal cans (H) not recommended for new designs.

N PACKAGE


OUTPUT A
INVERTING INPUT A
NON-INVERTING INPUT A
V-
1
2
3
4
8
7
6
5
V+
OUTPUT B
INVERTING INPUT B
NON-INVERTING INPUT B

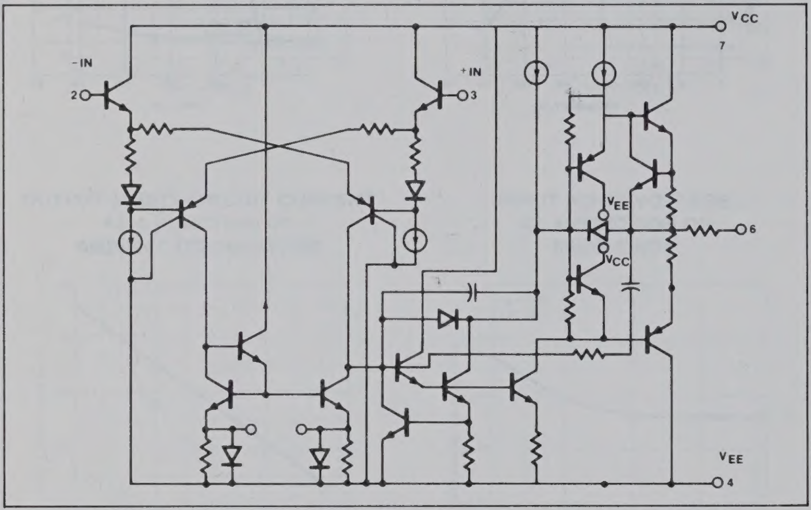
ORDER PART NO.
NE5530N
SE5530N

H PACKAGE*


NC
OUTPUT A
OUTPUT B
V+
V+
INVERTING INPUT A
INVERTING INPUT B
NON INVERTING INPUT A
NON-INVERTING INPUT B
V-
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩

ORDER PART NO.
NE5530H
SE5530H
*Metal cans (H) not recommended for new designs.

EQUIVALENT SCHEMATIC EACH AMPLIFIER


VCC
7
-IN
2
+IN
3
VEE
VCC
6
VEE
4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE530/5530	±22	V
NE530/5530	±18	V
Internal power dissipation		
N Package	500	mW
H Package	800	mW
FE Package	1000	mW
Differential input voltage	±30	V
Input voltage	±15	V
Operating temperature range		
SE530/5530	-55 to +125	°C
NE530/5530	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature range (Solder, 60sec)	300	°C
Output short circuit	Indefinite	

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = \pm15V$ unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \le 10k\Omega$ Over temperature		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
Temperature coefficient of input offset voltage			3	15		6		$\mu V/°C$
Input offset current	 Over temperature		5	20 40		15	40 80	nA nA
Input bias current	 Over temperature		45	80 200		65	150 200	nA nA
Input resistance		3	10		1	6		$M\Omega$
Input voltage range		±12	±13		±12	±13		V
Large signal voltage gain	$R_L \ge 2k\Omega$, $V_O = \pm10V$ Over temperature	50 25	200		50 25	200		V/mV V/mV
Output voltage swing	$R_L \ge 10k\Omega$ $R_L \ge 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V V
Output short circuit current			25			25		mA
Output resistance			100			100		Ω
Supply current	Each amplifier Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
Common mode rejection ratio	$R_S \le 10k\Omega$ Over temperature	70	90		70	90		dB
Power supply rejection ratio	$R_S \le 10k\Omega$ Over temperature		30	150		30	150	$\mu V/V$

AC ELECTRICAL CHARACTERISTICS

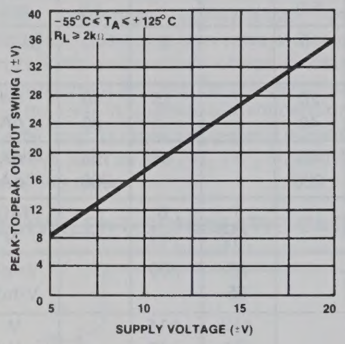
$T_A = 25°C$, $V_{CC} = \pm15V$ unless otherwise specified.

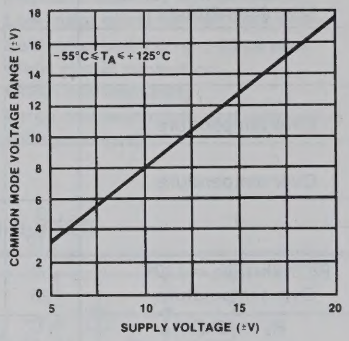
PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response Small signal rise time Small signal overshoot Settling time	 TO 0.1% (10V step)		 .06 13 0.9			 .06 13 0.9		 μs % μs
Slew rate Unity gain inverting Unity gain non-inverting	±15V supply, $V_O = \pm10V$, $R_L \ge 2k\Omega$	 25 18	 35 25		 20 12	 35 25		 $V/\mu s$ $V/\mu s$
Power bandwidth	5% THD, $V_O = \pm10V$, $R_L \ge 2k\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Channel separation			120			120		dB

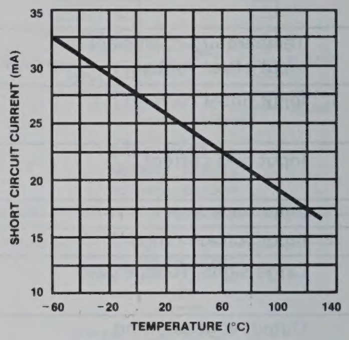
NOTE

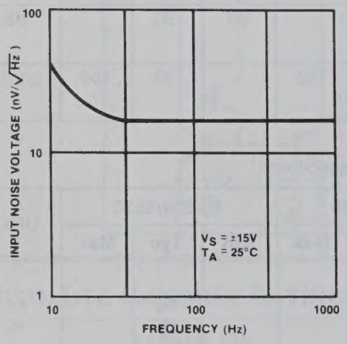
1. Operating temperature range for the SE530/5530 is -55°C to +125°C.
Operating temperature range for the NE530/5530 is 0°C to +70°C.

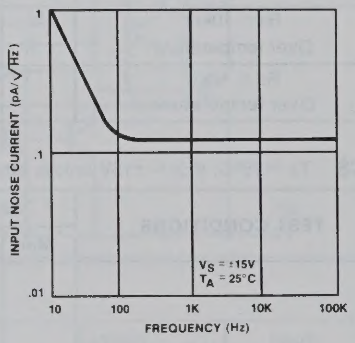
TYPICAL PERFORMANCE CHARACTERISTICS

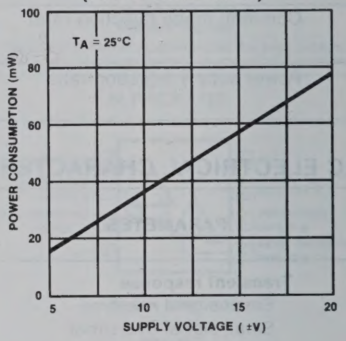

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

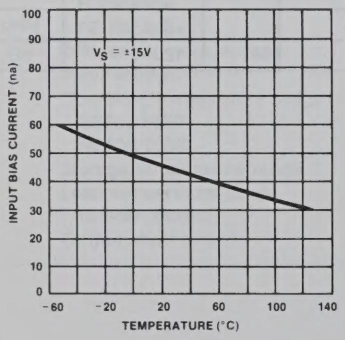

INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

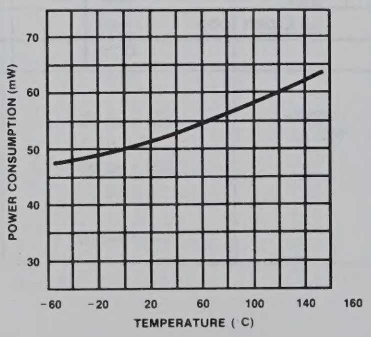

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

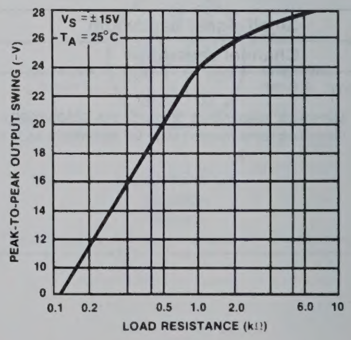

INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (EACH AMPLIFIER)

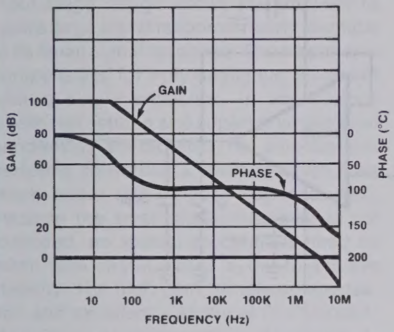

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (EACH AMPLIFIER)

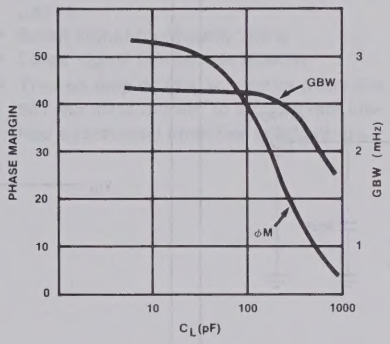

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

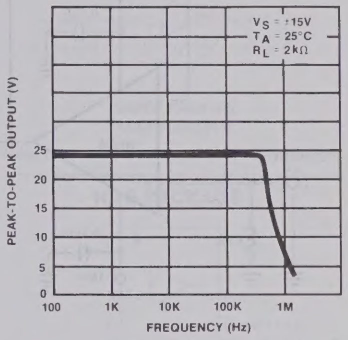
NE530 OPEN-LOOP GAIN AND PHASE vs FREQUENCY



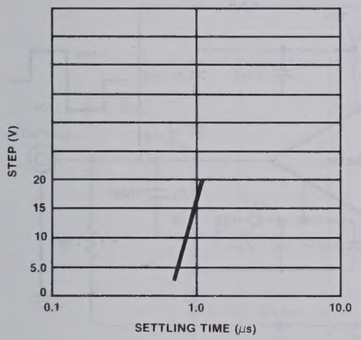
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN vs LOAD CAPACITANCE



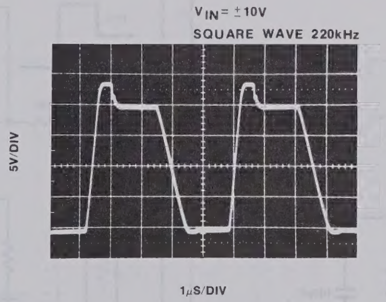
POWER BANDWIDTH



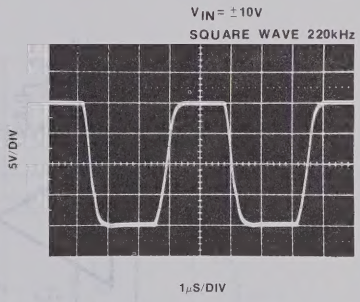
INPUT VOLTAGE STEP vs SETTLING TIME TO 10mV



SLEW RATE—VOLTAGE FOLLOWER

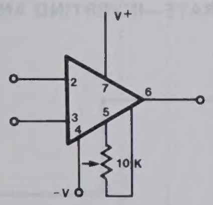


SLEW RATE (-1 AMPLIFIER)



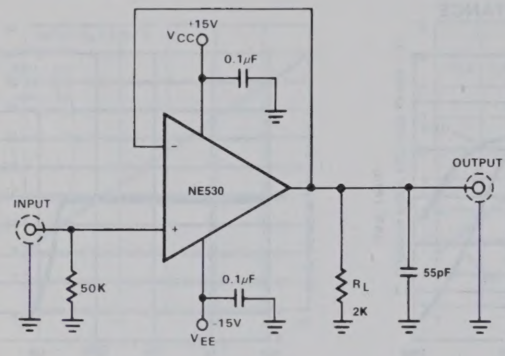
TYPICAL CIRCUIT CONNECTION

OFFSET ADJUST CIRCUIT



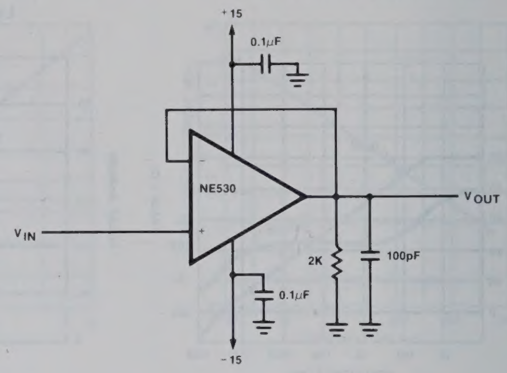
TEST LOAD CIRCUITS

SMALL SIGNAL TRANSIENT RESPONSE

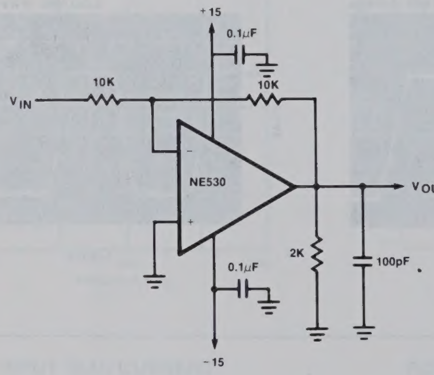

+15V
VCC
0.1μF
−
+
NE530
INPUT
50K
0.1μF
−15V
VEE
RL
2K
55pF
OUTPUT

Pins not shown are not connected.
All resistor values are typical and in ohms.

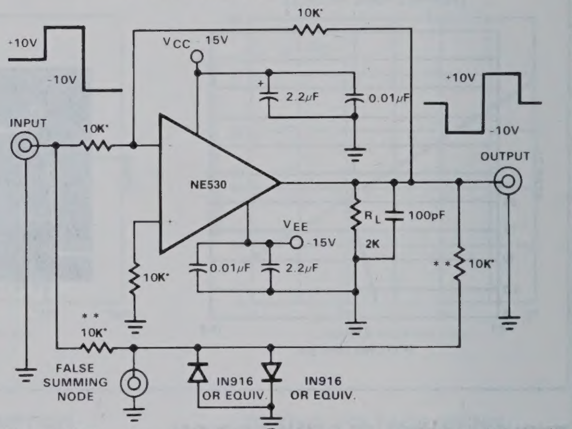
SLEW RATE—VOLTAGE FOLLOWER


+15
0.1μF
−
+
NE530
VIN
VOUT
2K
100pF
0.1μF
−15

SLEW RATE—INVERTING AMPLIFIER


+15
0.1μF
10K
10K
VIN
−
+
NE530
VOUT
2K
100pF
0.1μF
−15

SLEW RATE AND SETTLING TIME

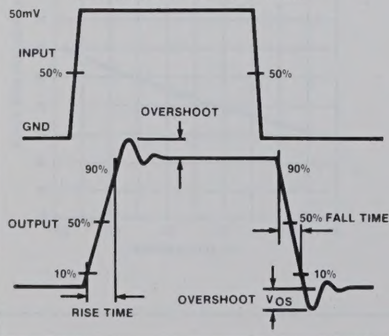

+10V
−10V
10K*
VCC 15V
2.2μF
0.01μF
+10V
−10V
INPUT
10K*
NE530
OUTPUT
RL
2K
100pF
VEE
−15V
0.01μF
2.2μF
10K*
* *
10K*
* *
10K*
FALSE SUMMING NODE
IN916 OR EQUIV.
IN916 OR EQUIV.

Pins not shown are not connected.
All resistor values are typical and in ohms.

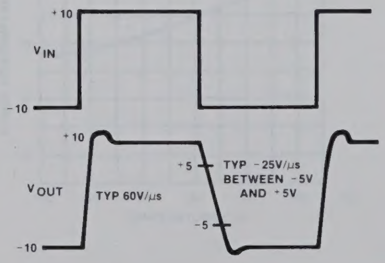
*Match to within 0.01%.
**Open for slew rate.

VOLTAGE WAVEFORMS

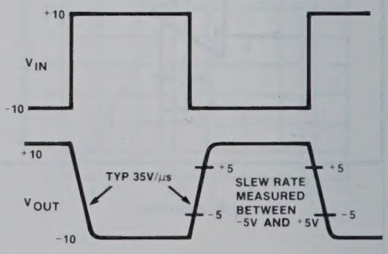
SMALL SIGNAL TRANSIENT RESPONSE DEFINITIONS


50mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT 50%
50% FALL TIME
10%
10%
RISE TIME
OVERSHOOT
VOS

SLEW RATE—VOLTAGE FOLLOWER


+10
VIN
−10
+10
+5
TYP −25V/μs BETWEEN −5V AND +5V
VOUT
TYP 60V/μs
−5
−10

SLEW RATE—INVERTING AMPLIFIER


+10
VIN
−10
+10
TYP 35V/μs
+5
+5
SLEW RATE MEASURED BETWEEN −5V AND +5V
VOUT
−5
−5
−10

HIGH SLEW RATE OPERATIONAL AMPLIFIER NE/SE531

NE/SE531-N,H,FE

DESCRIPTION

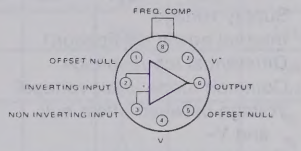
The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μsec slew rate at unity gain**
- **Pin for pin replacement for μA709, μA748 or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small signal bandwidth 1MHz**
- **Large signal bandwidth 500KHz**
- **True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.**

PIN CONFIGURATIONS

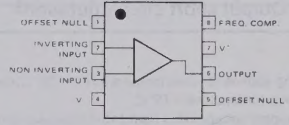
H PACKAGE*


FREQ. COMP.
OFFSET NULL
V+
INVERTING INPUT
OUTPUT
NON INVERTING INPUT
OFFSET NULL
V-
1
2
3
4
5
6
7
8

ORDER PART NO.
NE531H/SE531H

*Metal cans (H) not recommended for new designs

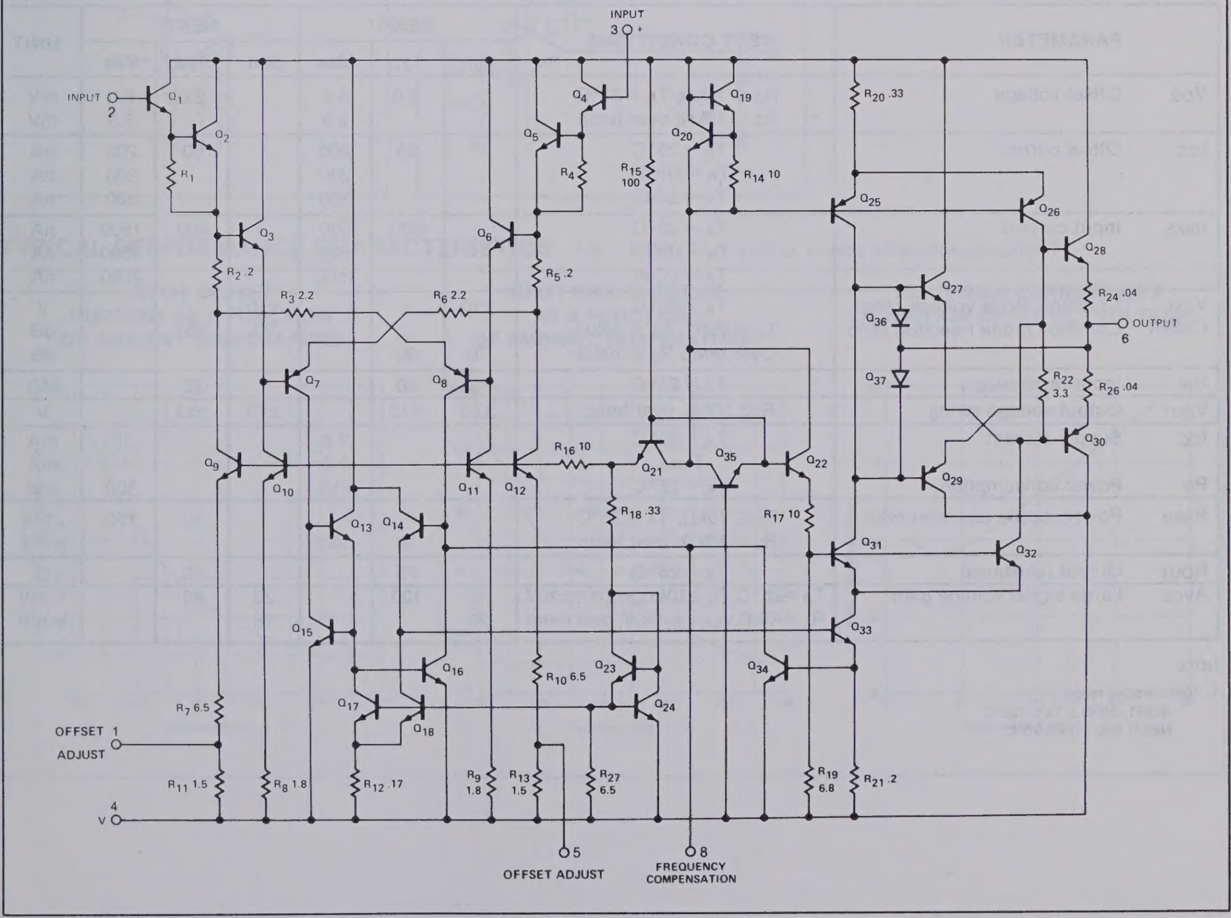
N,FE PACKAGE


OFFSET NULL
INVERTING INPUT
NON INVERTING INPUT
V-
FREQ. COMP.
V+
OUTPUT
OFFSET NULL
1
2
3
4
5
6
7
8

ORDER PART NO.

NE531N	SE531N
NE531FE	SE531FE

EQUIVALENT SCHEMATIC


INPUT 3 +
INPUT 2 -
Q1
Q2
R1
Q3
R2 .2
R3 2.2
Q4
Q5
R4
Q6
R5 .2
R6 2.2
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
R15 100
R14 10
R16 10
Q21
R18 .33
Q35
Q22
R17 10
R20 .33
Q25
Q26
Q27
Q28
Q36
Q37
R22 3.3
R24 .04
R26 .04
OUTPUT 6
Q29
Q30
Q31
Q32
Q33
Q34
Q23
Q24
R10 6.5
R7 6.5
OFFSET 1 ADJUST
R11 1.5
R8 1.8
R12 .17
R9 1.8
R13 1.5
R27 6.5
R19 6.8
R21 .2
4 V-
5 OFFSET ADJUST
8 FREQUENCY COMPENSATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation[1]	300	mW
Differential input voltage	±15	V
Common mode input voltage[2]	±15	V
Voltage between offset null and V−	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	−55 to +125	°C
Storage temperature range	−65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	SE531[1] Min	SE531[1] Typ	SE531[1] Max	NE531 Min	NE531 Typ	NE531 Max	UNIT
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp			6.0			7.5	mV
I_{OS}	Offset current	$T_A = 25°C$		30	200		50	200	nA
		T_A = HIGH			200			200	nA
		T_A = LOW			500			300	nA
I_{BIAS}	Input current	$T_A = 25°C$		300	500		400	1500	nA
		T_A = HIGH			500			1500	nA
		T_A = LOW			1500			2000	nA
V_{CM}	Common mode voltage range	$T_A = 25°C$	±10			±10			V
CMRR	Common mode rejection ratio	$T_A = 25°C$, $R_S \leq 10k\Omega$				70	100		dB
		Over temp $R_S \leq 10k\Omega$	70	90					dB
R_{IN}	Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	$T_A = 25°C$			7.0			10	mA
		T_{MAX}			7.0			10	mA
P_D	Power consumption	$T_A = 25°C$			210			300	mW
P_{SRR}	Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp		10	150				μV/V
R_{OUT}	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$T_A = 25°C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$	50	100		20	60		V/mV
		$R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	25			15			V/mV

NOTE

1. Temperature range:
   SE531 $-55°C \leq T_A \leq 125°C$
   NE531 $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

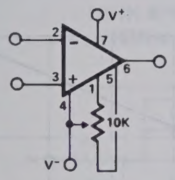
PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1%) (.01%)	$A_V = +1$, $V_{IN} = \pm 10V$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot	$A_V = +1$, $V_{IN} = \pm 10V$		2			2		%
Small signal overshoot	$A_V = +1$, $V_{IN} = 400mV$		5			5		%
Small signal risetime	$A_V = +1$, $V_{IN} = 400mV$		300			300		ns
Slew rate	$A_V = 100$		35			35		V/μs
	$A_V = 10$		35			35		V/μs
	$A_V = 1$ (noninverting)		30		20	30		V/μs
	$A_V = 1$ (inverting)		35		25	35		V/μs

NOTE

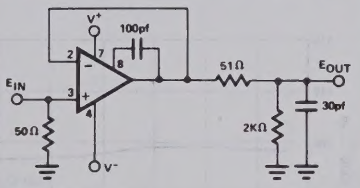
1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

OFFSET NULL CIRCUIT

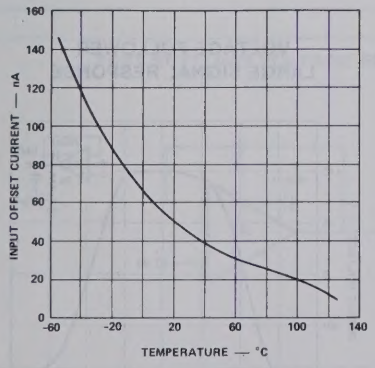


TRANSIENT RESPONSE CIRCUIT

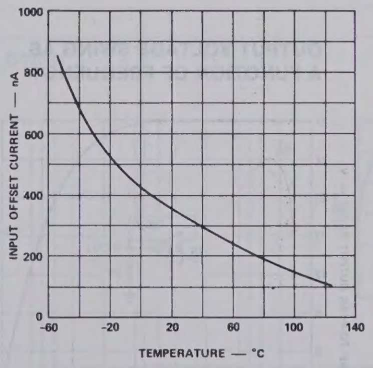


TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.)

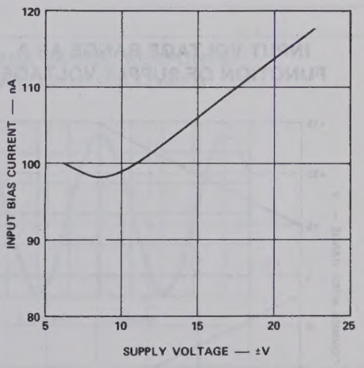
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

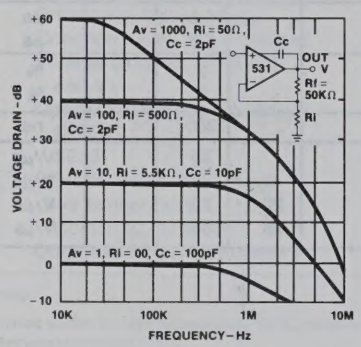


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

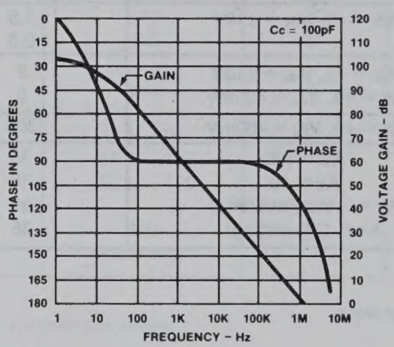


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

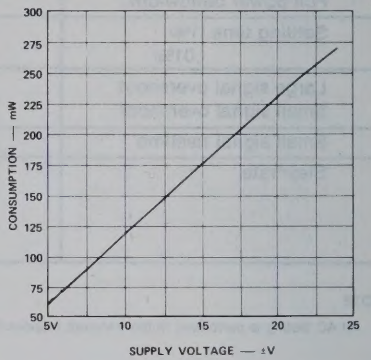
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



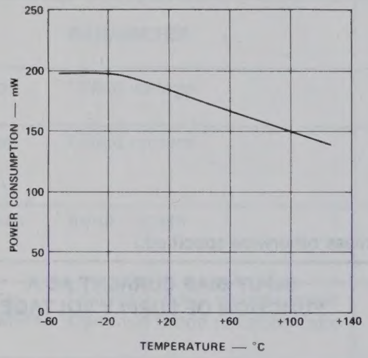
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



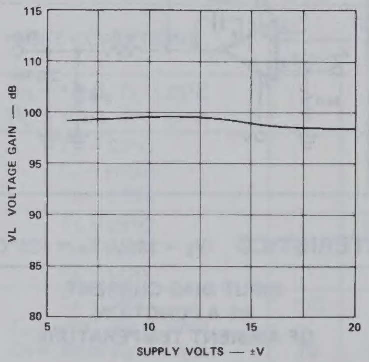
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



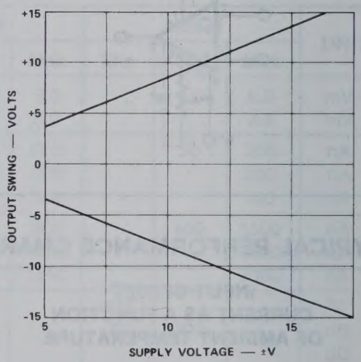
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



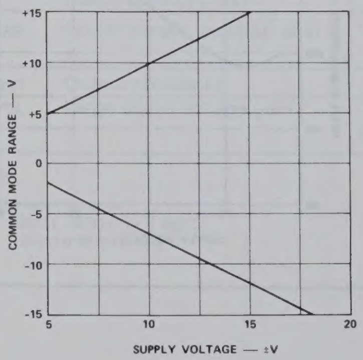
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



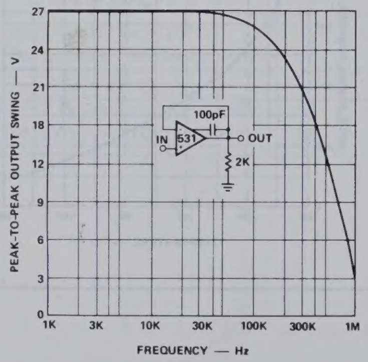
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



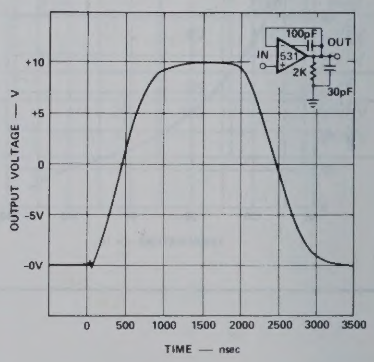
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

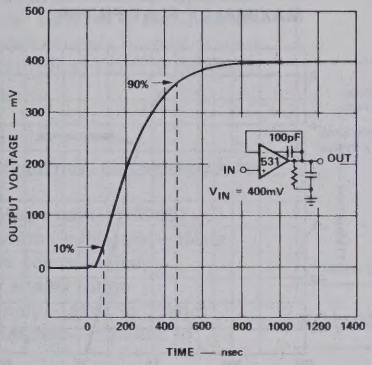


VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

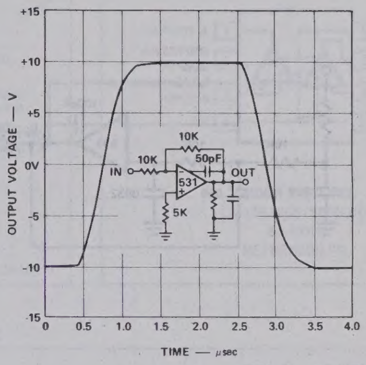


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

VOLTAGE FOLLOWER TRANSIENT RESPONSE

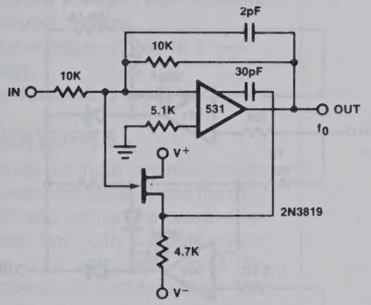


UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE

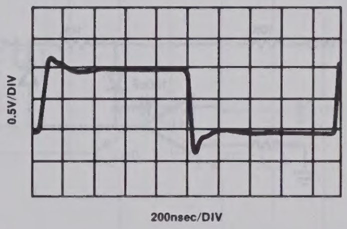


TYPICAL APPLICATIONS

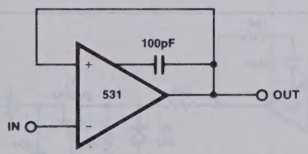
HIGH SPEED INVERTER (10MHz BANDWIDTH)


2pF
10K
10K
30pF
IN
531
OUT
f_0
5.1K
V+
2N3819
4.7K
V−

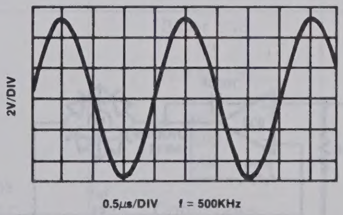
PULSE RESPONSE HIGH SPEED INVERTER



FAST SETTLING VOLTAGE FOLLOWER

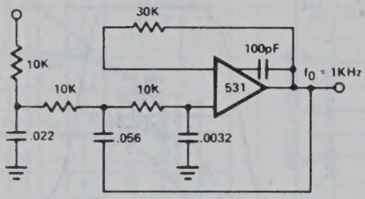

+
−
531
100pF
IN
OUT

LARGE SIGNAL RESPONSE VOLTAGE FOLLOWER

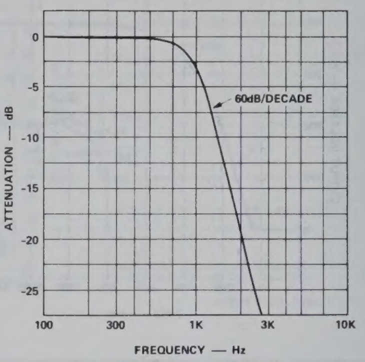


TYPICAL APPLICATIONS (Cont'd)

POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*


30K
10K
100pF
f_0 = 1KHz
10K
10K
531
.022
.056
.0032

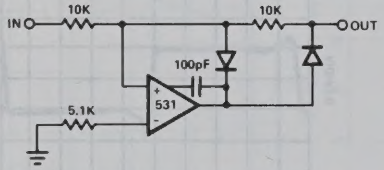
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



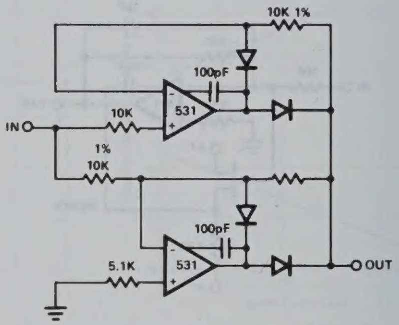
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

PRECISION RECTIFIERS

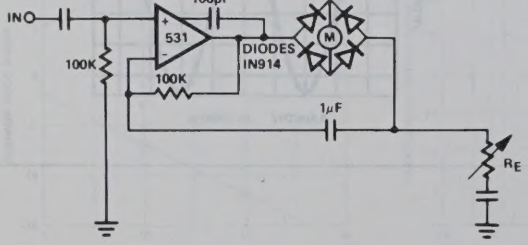
(a) HALF WAVE


IN
10K
10K
OUT
100pF
531
5.1K

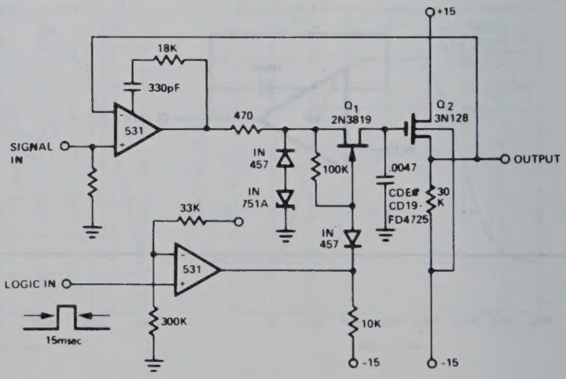
(b) FULL WAVE


10K 1%
100pF
531
IN
10K
1%
10K
100pF
531
5.1K
OUT

AC MILLIVOLTMETER


IN
100pF
531
M
DIODES
IN914
100K
100K
1μF
R_E

SAMPLE AND HOLD


+15
18K
330pF
531
470
Q1
2N3819
Q2
3N128
OUTPUT
SIGNAL IN
IN 457
100K
.0047
IN 751A
CDE#
CD19-
FD4725
30 K
33K
IN 457
531
LOGIC IN
15msec
300K
10K
-15
-15

DUAL OPERATIONAL AMPLIFIER SINGLE OR DUAL POWER SUPPLY OPERATION

NE/SE/SA532 LM158/258/358

NE/SE532-N,H,FE/SA532-N
LM158/258/358-N,H,FE

DESCRIPTION

The 532/358 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

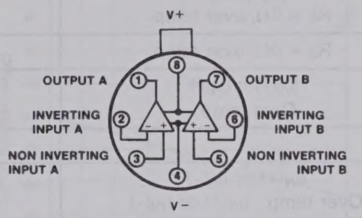
- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  - **single supply—(3Vdc to 30Vdc)**
  - **or dual supplies—(±1.5Vdc to ±15Vdc)**
- **Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nA dc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nA dc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+ − 1.5Vdc swing)**
- **SE532 Mil std 883A,B,C available**

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

PIN CONFIGURATIONS

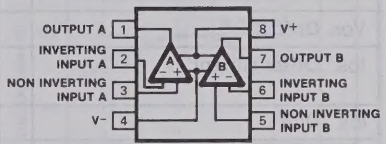
H PACKAGE*


V+
OUTPUT A
INVERTING INPUT A
NON INVERTING INPUT A
OUTPUT B
INVERTING INPUT B
NON INVERTING INPUT B
V−
1
2
3
4
5
6
7
8

ORDER PART NO.
LM158/258/358H
NE/SE532H

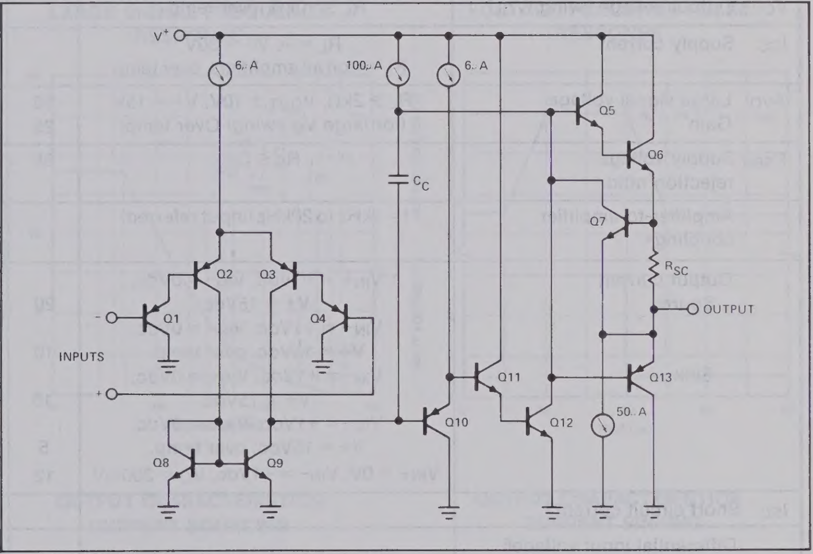
*Metal cans (H) not recommended for new designs

N,FE PACKAGE


OUTPUT A
INVERTING INPUT A
NON INVERTING INPUT A
V−
V+
OUTPUT B
INVERTING INPUT B
NON INVERTING INPUT B
1
2
3
4
5
6
7
8
A
B

ORDER PART NO.
LM158/258/358N,FE
SA532N
NE/SE532N,FE

EQUIVALENT CIRCUIT


V+
6μA
100μA
6μA
Q5
Q6
CC
Q7
RSC
OUTPUT
Q2
Q3
Q1
Q4
INPUTS
−
+
Q11
Q13
Q10
Q12
50μA
Q8
Q9

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation[1]		
FE package	900	mW
H package	680	mW
N package	500	mW
Output short-circuit to GND[5]		
V+ < 15 Vdc and $T_A = 25°C$	Continuous	
Operating temperature range		
NE532/LM358	0 to +70	°C
LM258	-25 to +85	°C
SA532N	-40 to +85	°C
SE532/LM158	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NE/SE532-N,H,FE/SA532-N
LM158/258/358-N,H,FE

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V+ = +5V$ unless otherwise specified.

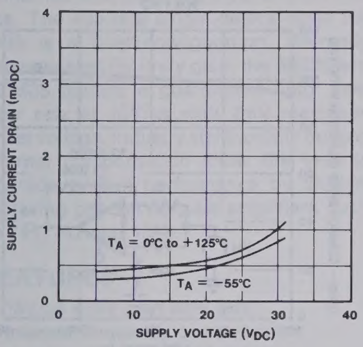
PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 0\Omega$		±2	±5		±2	±7	mV
	$R_S \leq 0\Omega$, over temp.			±7			±9	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		μV/°C
I_{OS} Offset current	$I_{IN}(+) - I_{IN}(-)$		±3	±30		±5	±50	nA
	Over temp.			±100			±150	nA
I_{OS} Drift			10			10		pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	300		40	500	nA
V_{CM} Common mode voltage range[3]	$V+ = 30V$	0		V+−1.5	0		V+−1.5	V
	Over temp., $V+ = 30V$	0		V+−2.0	0		V+−2.0	V
$CMRR$ Common mode rejection ratio		70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, $V+ = 30V$, over temp	26			26			V
	$R_L \geq 10k\Omega$, $V+ = 30V$, over temp	27	28		27	28		V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$, $V+ = 30V$		1.0	2.0		1.0	2.0	mA
	$R_L = \infty$ on all amplifiers, over temp		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, $V+ = 15V$	50	100		25	100		V/mV
	(for large V_O swing) Over temp.	25			15			V/mV
P_{SRR} Supply voltage rejection ratio	$R_S \leq 0\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		-120			-120		dB
Output current Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$, over temp.	10	20		10	20		mA
Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$, over temp.	5	8		5	8		mA
	$V_{IN}+ = 0V$, $V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC} Short circuit current[5]			40	60		40	60	mA
Differential input voltage[6]				V+			V+	V

NOTES

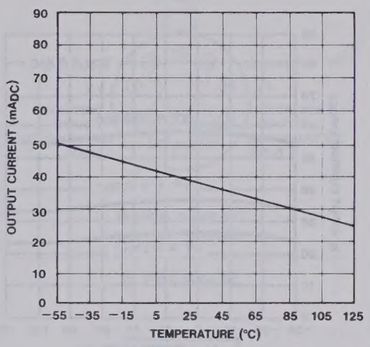
1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ −1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and case eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32Vdc without damage.
7. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.

TYPICAL PERFORMANCE CHARACTERISTICS

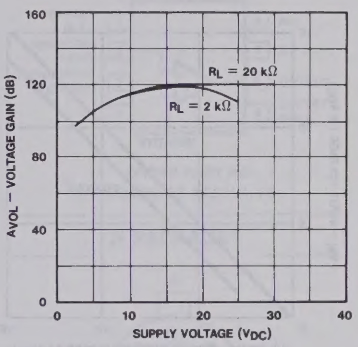
SUPPLY CURRENT



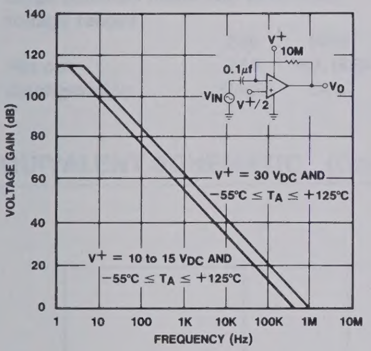
CURRENT LIMITING



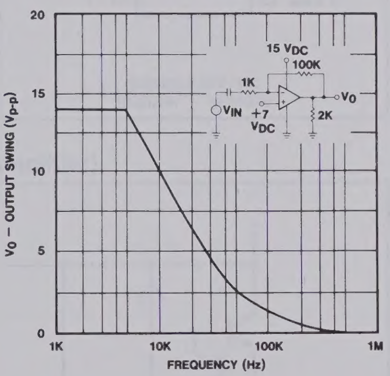
VOLTAGE GAIN



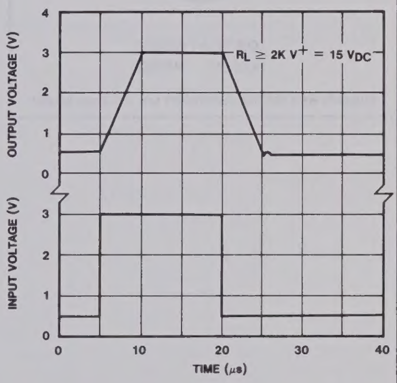
OPEN LOOP FREQUENCY RESPONSE



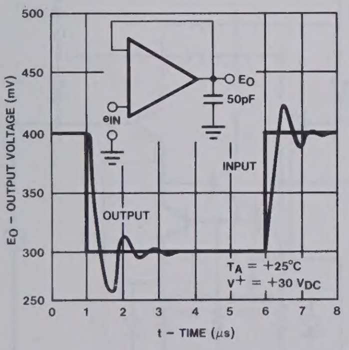
LARGE SIGNAL FREQUENCY RESPONSE



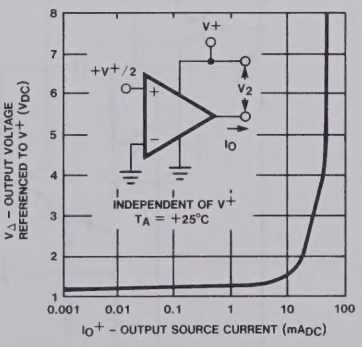
VOLTAGE FOLLOWER PULSE RESPONSE



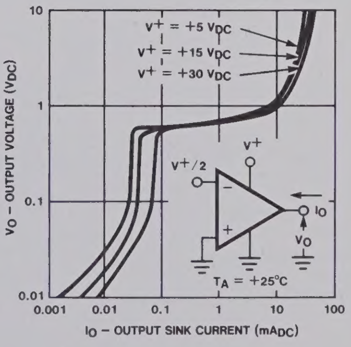
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



OUTPUT CHARACTERISTICS CURRENT SOURCING

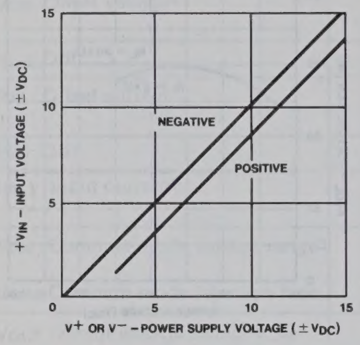


OUTPUT CHARACTERISTICS CURRENT SINKING

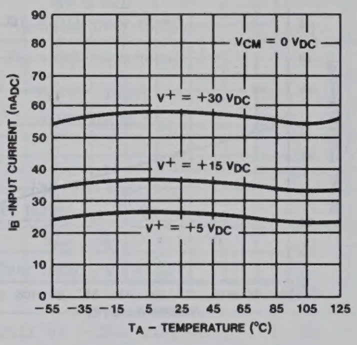


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

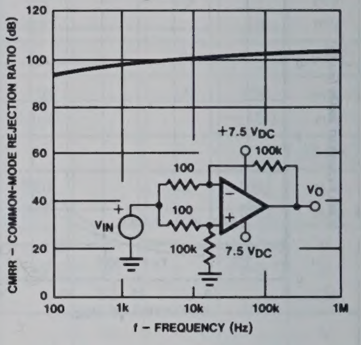
INPUT VOLTAGE RANGE



INPUT CURRENT



COMMON MODE REJECTION RATIO



SINGLE OR DUAL HIGH SLEW RATE OP AMP NE/SE535/5535

NE/SE535N,H,FE • NE/SE5535-H,N

DESCRIPTION

The 535 and 5535 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. The 535 is a single device while the 5535 is a dual configuration. Internally compensated for unity gain, the SE535 and SE5535 feature a guaranteed unity gain slew rate of 10V/μs with 2mV maximum offset voltage. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 741, 747 and 1558.

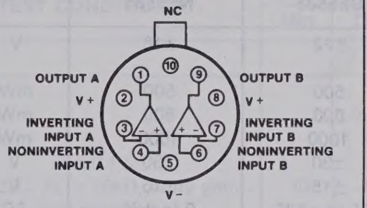
FEATURES

- **15V/μs unity gain slew rate**
- **Internal frequency compensation**
- **Low input offset voltage—2mV**
- **Low input bias current 80nA max**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

	535	5535
• **Pin out**	**741**	**747,1558**
• **Configuration**	**Single**	**Dual**

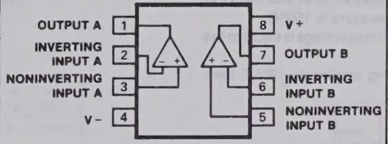
PIN CONFIGURATIONS

H PACKAGE*


NC
OUTPUT A
V+
INVERTING INPUT A
NONINVERTING INPUT A
OUTPUT B
V+
INVERTING INPUT B
NONINVERTING INPUT B
V−
1
2
3
4
5
6
7
8
9
10

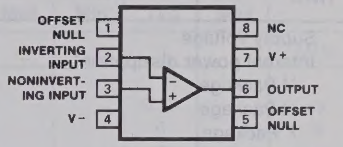
ORDER PART NO.
SE5535H NE5535H

N PACKAGE


OUTPUT A
INVERTING INPUT A
NONINVERTING INPUT A
V−
V+
OUTPUT B
INVERTING INPUT B
NONINVERTING INPUT B
1
2
3
4
5
6
7
8

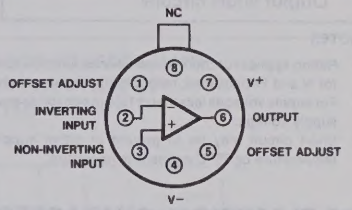
ORDER PART NO.
SE5535N NE5535N

FE, N PACKAGE


OFFSET NULL
INVERTING INPUT
NONINVERTING INPUT
V−
NC
V+
OUTPUT
OFFSET NULL
1
2
3
4
5
6
7
8

ORDER PART NO.
SE535N, FE NE535N, FE

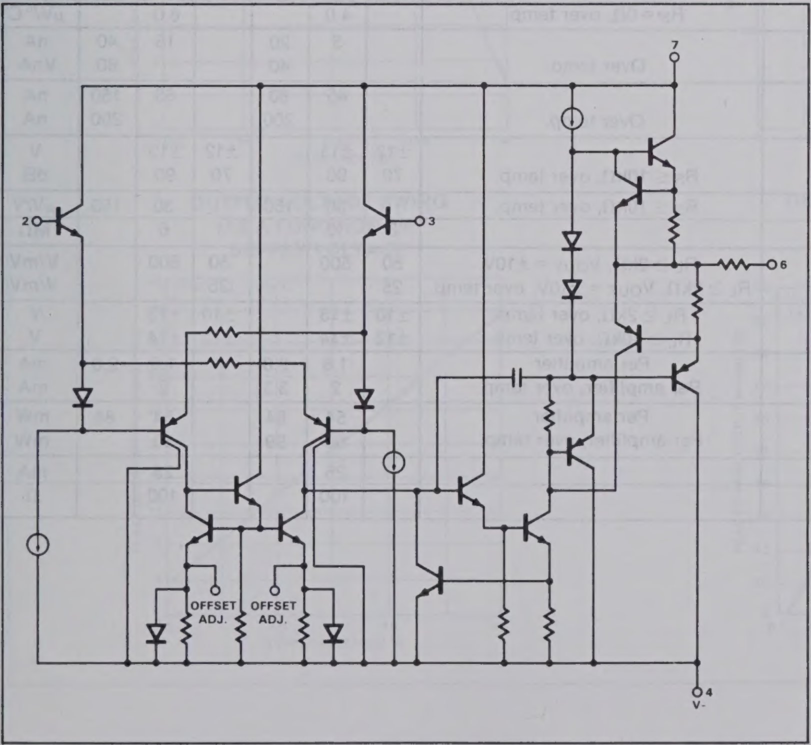
H PACKAGE*


NC
OFFSET ADJUST
INVERTING INPUT
NON-INVERTING INPUT
V+
OUTPUT
OFFSET ADJUST
V−
1
2
3
4
5
6
7
8

ORDER PART NO.
SE535H NE535H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC (One Amplifier)


7
2
3
6
OFFSET ADJ.
OFFSET ADJ.
4
V-

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SE535/ SE5535	NE535/ NE5535	UNIT
Supply voltage	±22	±18	V
Internal power dissipation[1]			
N Package	500	500	mW
H Package	800	800	mW
F Package	1000	1000	mW
Differential input voltage	±30	±30	V
Input voltage[2]	±15	±15	V
Operating temperature range	-55 to +125	0 to +70	°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature (solder, 60sec)	300	300	°C
Output short circuit[3]	Indefinite	Indefinite	

NOTES

1. Rating applies for thermal resistances junction to ambient of 240°C/W and 150°C/W for N and H packages, respectively. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.*

PARAMETER		TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp.			5.0			7.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		μV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temp.			40			80	VnA
I_B	Input current			45	80		65	150	nA
		Over temp.			200			200	nA
V_{CM}	Common mode voltage range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
P_{SRR}	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	50	500		50	500		V/mV
		$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$, over temp.	25			25			V/mV
V_{OUT}	Output voltage	$R_L \geq 2k\Omega$, over temp.	±10	±13		±10	±13		V
		$R_L \geq 10k\Omega$, over temp.	±12	±14		±12	±14		V
I_{CC}	Supply current	Per amplifier		1.8	2.8		1.8	2.8	mA
		Per amplifier, over temp.		2	3.3		2		mA
P_D	Power dissipation	Per amplifier		54	84		54	84	mW
		Per amplifier, over temp.		60	99		60		mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

*NOTE

Temperature range

SE types -55°C ≤ T_A ≤ 125°C

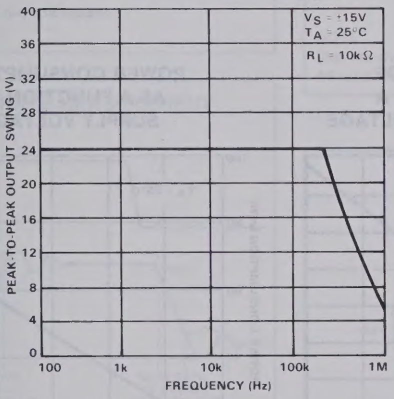
NE types 0°C ≤ T_A ≤ 70°C

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

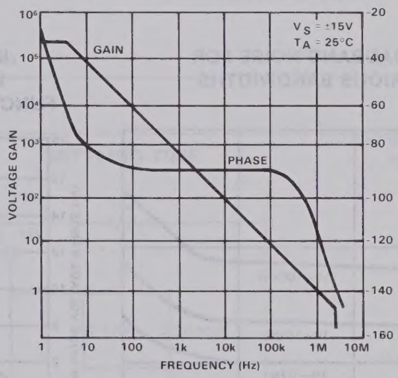
PARAMETER	TEST CONDITIONS	SE535/SE5535 Min	SE535/SE5535 Typ	SE535/SE5535 Max	NE535/NE5535 Min	NE535/NE5535 Typ	NE535/NE5535 Max	UNIT
Gain/bandwidth product			1			1		MHz
Transient response								
Small signal rise time			0.25			0.25		μs
Small signal overshoot			6			6		%
Settling time	To 0.1%		3			3		μs
Slew rate	T_A = 25C, $R_L \geq 10k\Omega$, unity gain, non-inverting	10	15		10	15		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

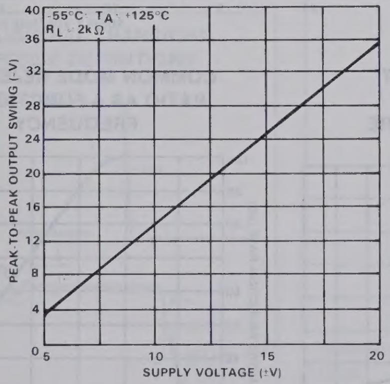
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



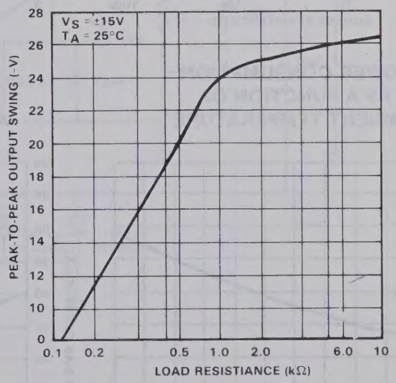
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

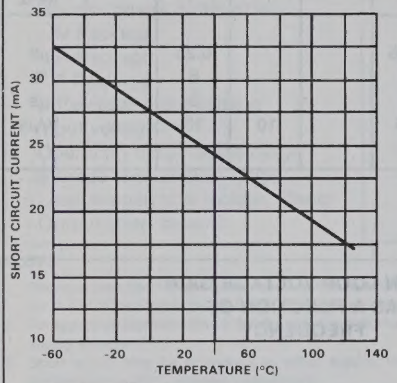


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

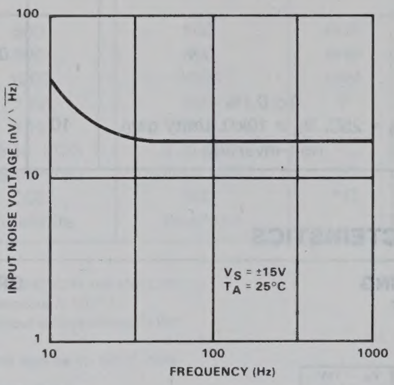


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

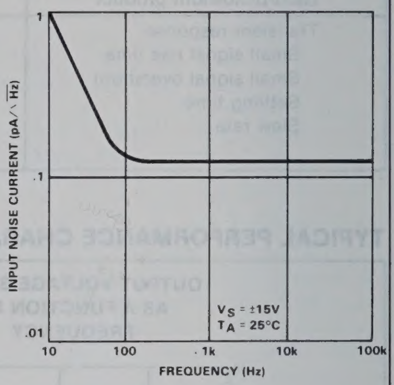
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



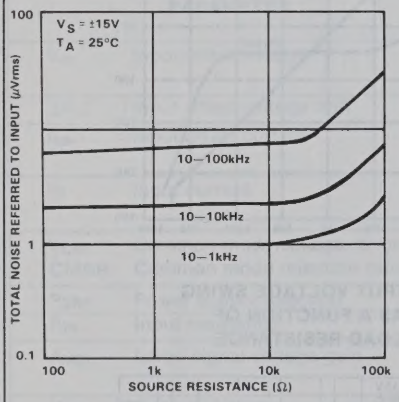
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



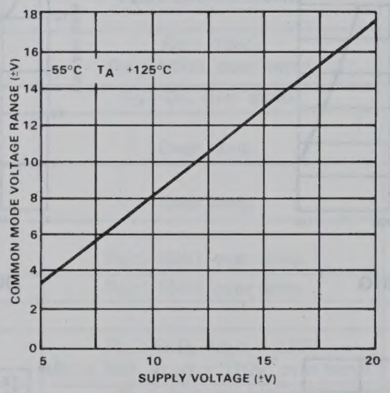
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



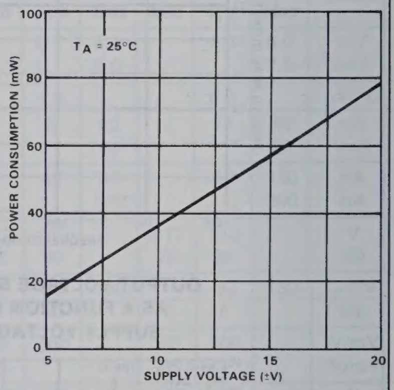
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



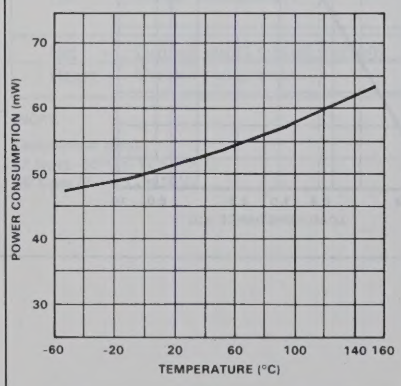
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



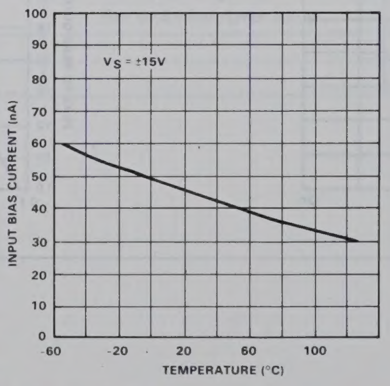
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



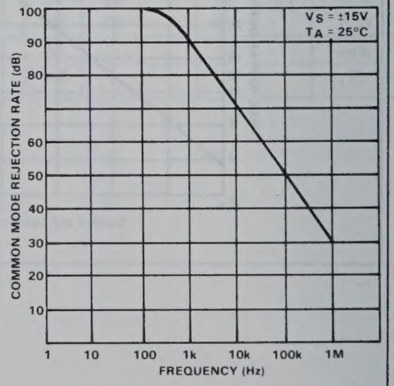
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

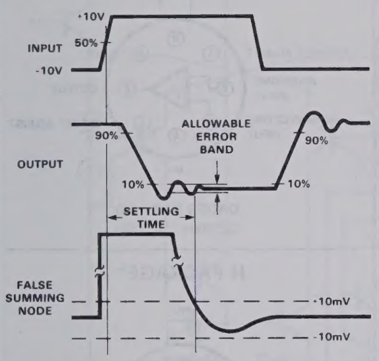


COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

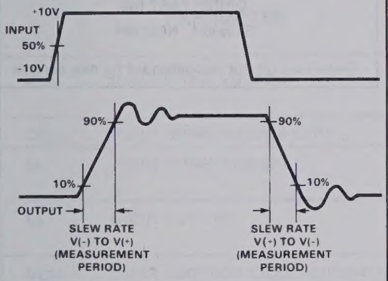


VOLTAGE WAVEFORMS

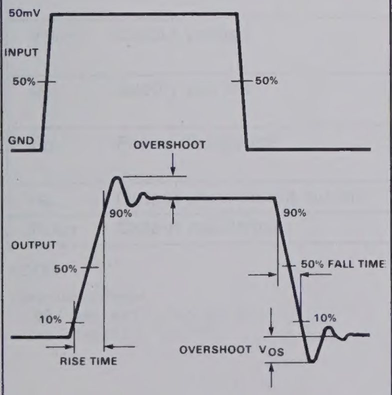
SETTLING TIME MEASUREMENT


+10V
INPUT
50%
-10V
ALLOWABLE ERROR BAND
90%
90%
OUTPUT
10%
10%
SETTLING TIME
FALSE SUMMING NODE
+10mV
-10mV

SLEW RATE MEASUREMENT

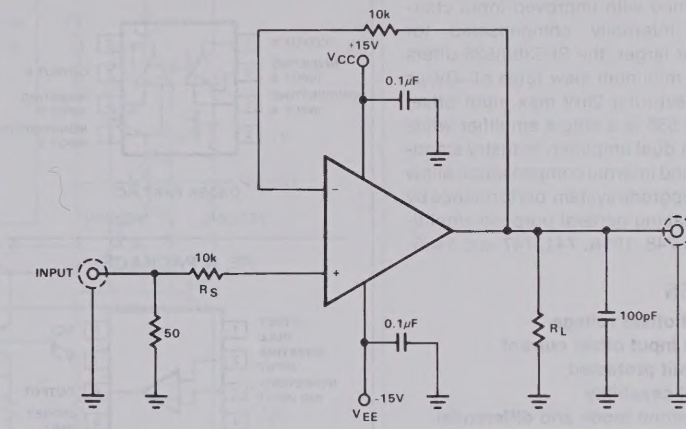

+10V
INPUT
50%
-10V
90%
90%
10%
10%
OUTPUT
SLEW RATE V(-) TO V(+) (MEASUREMENT PERIOD)
SLEW RATE V(+) TO V(-) (MEASUREMENT PERIOD)

SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS


50mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT
50%
50% FALL TIME
10%
10%
RISE TIME
OVERSHOOT V_{OS}

TEST CIRCUITS

SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE

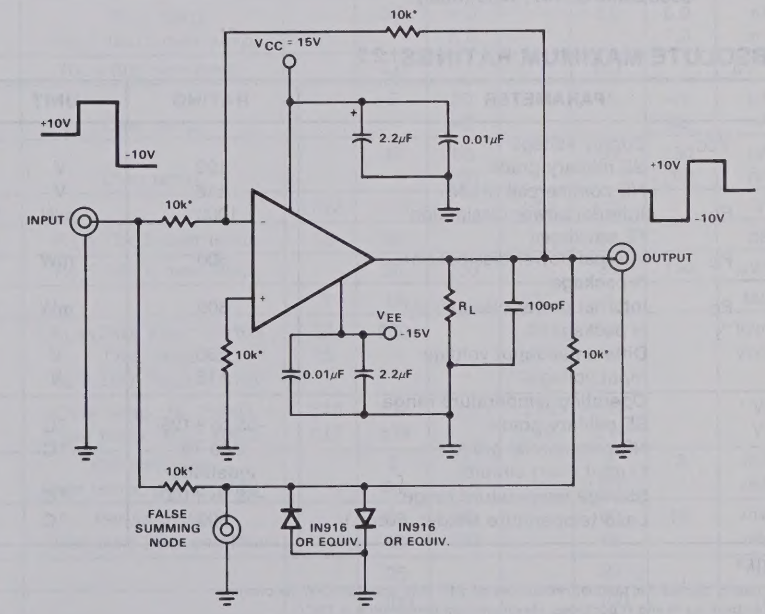

10k
+15V
V_{CC}
0.1μF
-
+
OUTPUT
INPUT
10k
R_S
50
0.1μF
R_L
100pF
-15V
V_{EE}

NOTE

Pins not shown are not connected.

All resistors values are typical and in ohms.

SETTLING TIME


10k*
V_{CC} = 15V
+
2.2μF
0.01μF
+10V
-10V
+10V
-10V
10k*
INPUT
-
+
OUTPUT
R_L
100pF
V_{EE}
-15V
10k*
10k*
0.01μF
2.2μF
10k*
FALSE SUMMING NODE
IN916 OR EQUIV.
IN916 OR EQUIV.

*Match to within 0.01%.

NOTE

Pins not shown are not connected.

All resistors values are typical and in ohms.

DUAL HIGH SLEW RATE OP AMPS NE/SE538/5538

NE/SE538-N,H,FE • NE/SE5538-H,N

DESCRIPTION

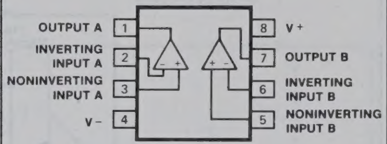
The NE/SE538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/5538 offers guaranteed minimum slew rates of 40V/μs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual amplifier. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

FEATURES

- **2mV input offset voltage**
- **80nA max input offset current**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**
- **60V/μs slew rate (gain of +5, −4 min)**
- **6MHz gain bandwidth product (gain +5, −4 minimum)**
- **Internal frequency compensation (gain of +5, −4 minimum)**
- **Pin out: 538 same as 741 (single)**
  5538 same as 747, 1458 (dual)

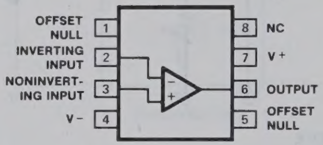
PIN CONFIGURATIONS

N PACKAGE


OUTPUT A
INVERTING INPUT A
NONINVERTING INPUT A
V−
1
2
3
4
8
7
6
5
V+
OUTPUT B
INVERTING INPUT B
NONINVERTING INPUT B

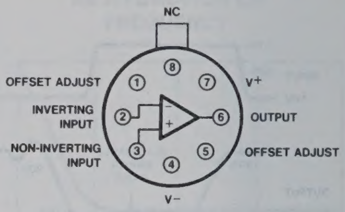
ORDER PART NO.
SE5538N, NE5538N

FE, N PACKAGE


OFFSET NULL
INVERTING INPUT
NONINVERTING INPUT
V−
1
2
3
4
8
7
6
5
NC
V+
OUTPUT
OFFSET NULL

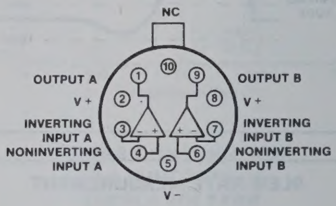
ORDER PART NO.
SE538N, FE NE538N, FE

H PACKAGE*


NC
OFFSET ADJUST
INVERTING INPUT
NON-INVERTING INPUT
V−
V+
OUTPUT
OFFSET ADJUST
1
2
3
4
5
6
7
8

ORDER PART NO.
SE538H NE538H

H PACKAGE*


NC
OUTPUT A
V+
INVERTING INPUT A
NONINVERTING INPUT A
V−
OUTPUT B
V+
INVERTING INPUT B
NONINVERTING INPUT B
1
2
3
4
5
6
7
8
9
10

ORDER PART NO.
SE5538H NE5538H

*Metal cans (H) not recommended for new designs

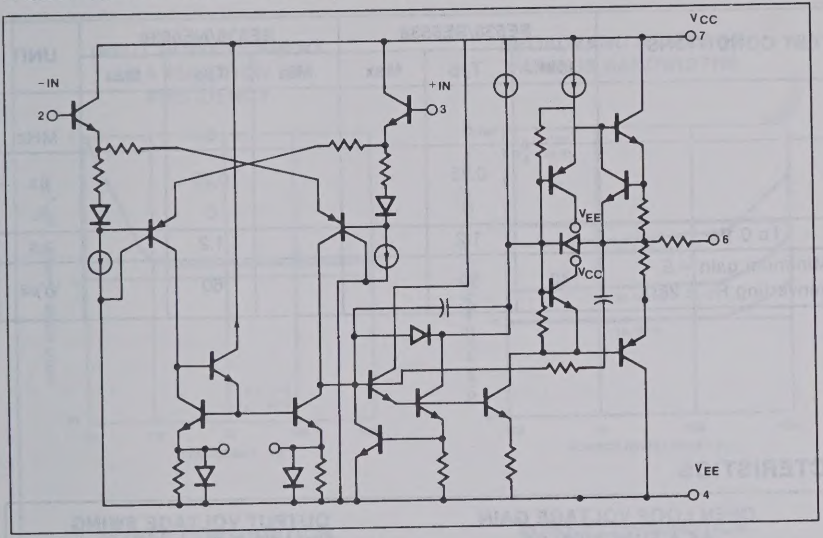
ABSOLUTE MAXIMUM RATINGS[1,2,3]

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		
	SE military grade	±22	V
	NE commercial grade	±18	V
P_D	Internal power dissipation FE package	1000	mW
P_D	Internal power dissipation[1] N package	500	mW
P_D	Internal power dissipation[1] H package	800	mW
	Differential input voltage	±30	V
	Input voltage[2]	±15	V
	Operating temperature range		
	SE military grade	-55 to +125	°C
	NE commercial grade	0 to 70	°C
	Output short circuit[3]	indefinite	
	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60sec.)	300	°C

NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and H packages. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \le 10k\Omega$ $R_S \le 10k\Omega$, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		μV/°C
I_{OS}	Input offset current	 Over temp.		5	20 40		15	40 80	nA nA
I_B	Input current	 Over temp.		45	80 200		65	150 200	nA nA
V_{CM}	Input common mode voltage range		±12	±13		±12	±13		V
$CMRR$	Common mode rejection ratio	$R_S \le 10k\Omega$, over temp.	70	90		70	90		dB
$PSRR$	Power supply rejection	$R_S \le 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \ge 2k\Omega$, $V_{OUT} = \pm 10V$ Over temp., $R_L \ge 2k\Omega$, $V_{OUT} = \pm 10V$	50 25	200		50 25	200		V/mV V/mV
V_{OUT}	Output voltage	Over temp., $R_L \ge 2k\Omega$ Over temp., $R_L \ge 10k\Omega$	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I_{CC}	Supply current	Per amplifier Over temp., per amplifier		2 2.2	3 3.6		2 2.2	3	mA mA
P_D	Power dissipation	Per amplifier Over temp., per amplifier		60 66	90 108		60 66	90	mW mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

NOTE

Temperature Range

SE Types $-55°C \le T_A \le 125°C$

NE Types $0°C \le T_A \le 70°C$

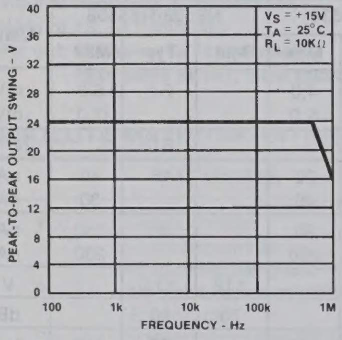
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.

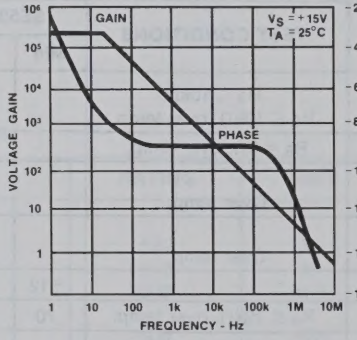
PARAMETER	TEST CONDITIONS	SE538/SE5538			SE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response Small signal rise time Small signal overshoot			0.25 6			0.25 6		µs %
Settling time	To 0.1%		1.2			1.2		µs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

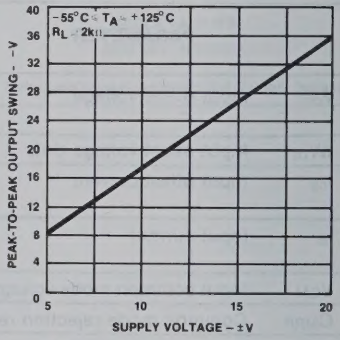
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



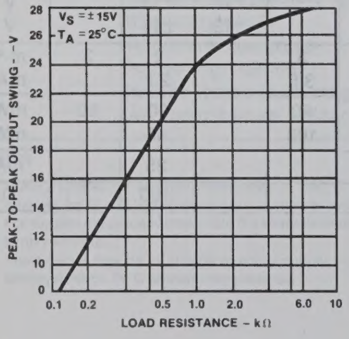
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



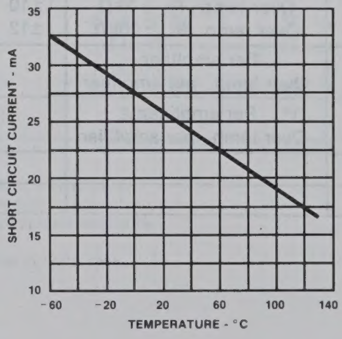
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



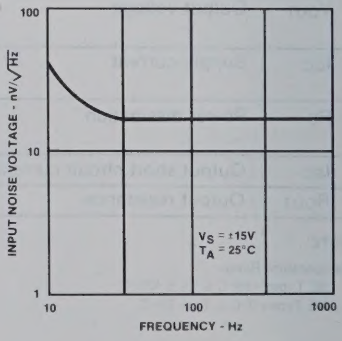
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

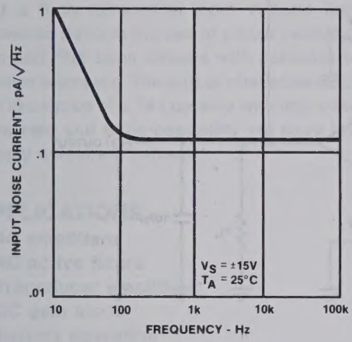


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

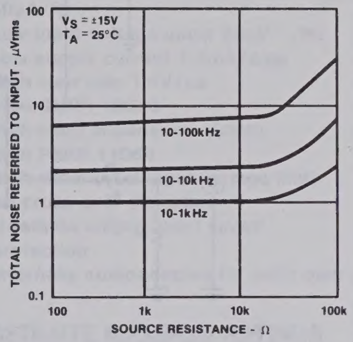


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

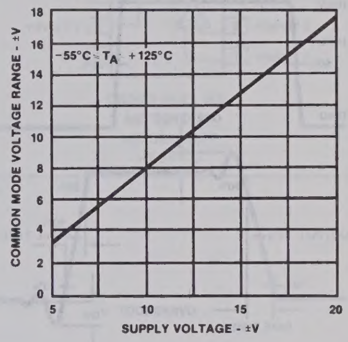
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



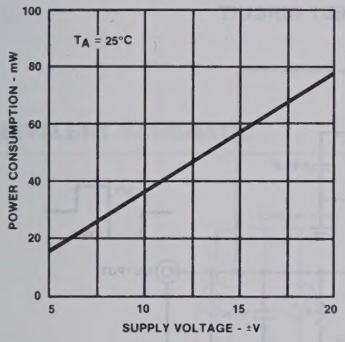
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



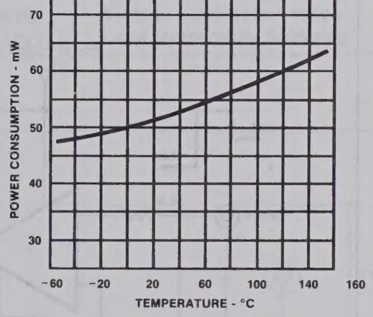
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



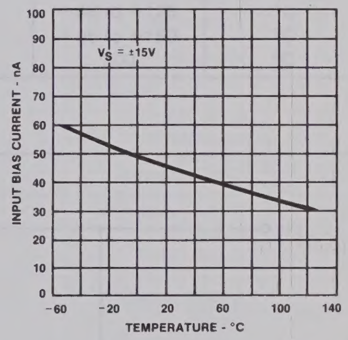
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



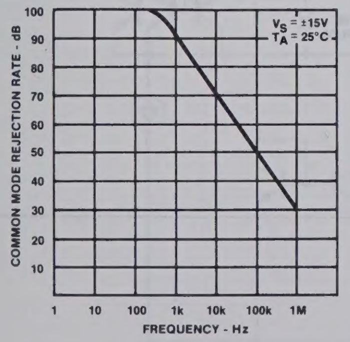
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



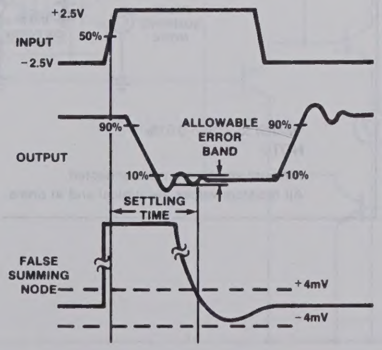
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



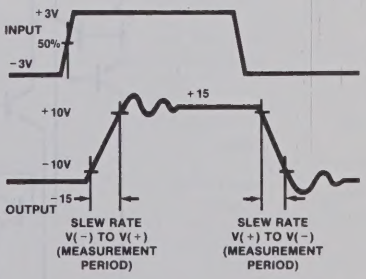
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SETTLING TIME MEASUREMENT WAVEFORMS

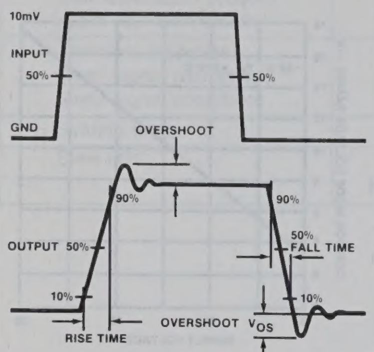

+2.5V
INPUT
50%
−2.5V
OUTPUT
90%
ALLOWABLE ERROR BAND
90%
10%
10%
SETTLING TIME
FALSE SUMMING NODE
+4mV
−4mV

SLEW RATE MEASUREMENT VCC = ±20V


+3V
INPUT
50%
−3V
+15
+10V
−10V
−15
OUTPUT
SLEW RATE V(−) TO V(+) (MEASUREMENT PERIOD)
SLEW RATE V(+) TO V(−) (MEASUREMENT PERIOD)

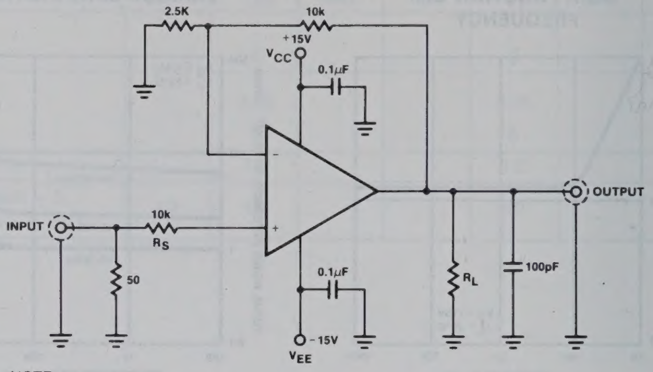
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS


10mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT 50%
50%
FALL TIME
10%
10%
OVERSHOOT V_{OS}
RISE TIME

TEST LOAD CIRCUITS

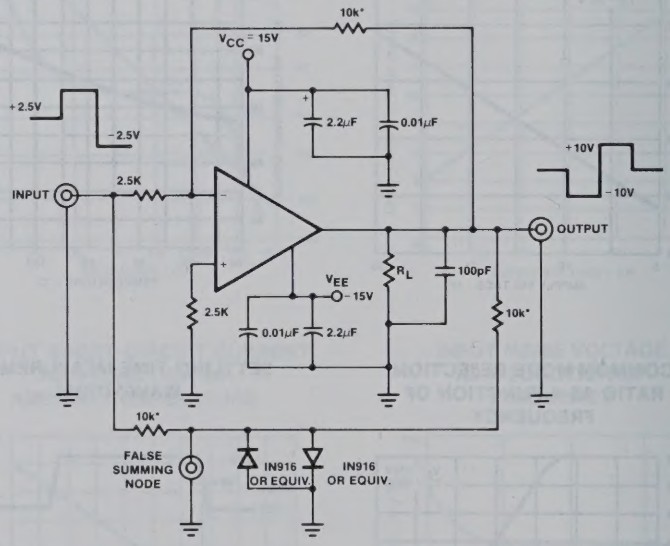
SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE TEST CIRCUIT


2.5K
10k
+15V
V_{CC}
0.1µF
−
+
INPUT
10k
R_S
50
0.1µF
−15V
V_{EE}
R_L
100pF
OUTPUT

NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

TEST LOAD CIRCUITS (Cont'd)

SETTLING TIME TEST CIRCUIT


10k*
V_{CC} = 15V
+
2.2µF
0.01µF
+2.5V
−2.5V
INPUT
2.5K
−
+
+10V
−10V
OUTPUT
V_{EE}
−15V
R_L
100pF
2.5K
0.01µF
2.2µF
10k*
10k*
FALSE SUMMING NODE
IN916 OR EQUIV.
IN916 OR EQUIV.

*Match to within 0.01%.
NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER NE/SE5512

NE/SE5512-D,N,FE

DESCRIPTION

The 5512 series of high performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

APPLICATIONS

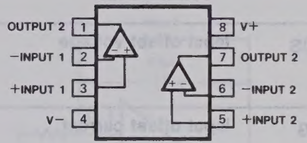
- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Battery operation**
- **Instrumentation applications**

FEATURES

- **Low input bias < ±3nA**
- **Low input offset current < ±3nA**
- **Low input offset voltage < 1mV**
- **Low V_{OS} temperature drift 4μV/°C**
- **Low input bias temperature drift 30pA/°C**
- **Low input voltage noise 25nV/√Hz**
- **Low supply current 1.5mA/amp**
- **High slew rate 1.0V/μs**
- **High CMRR 100dB**
- **High input impedance 100MΩ**
- **High PSRR 110dB**
- **High differential input voltage limit**
- **No cross-over distortion**
- **Indefinite output short circuit protection**
- **Internally compensated for unity gain**

PIN CONFIGURATIONS

D,N,FE PACKAGE

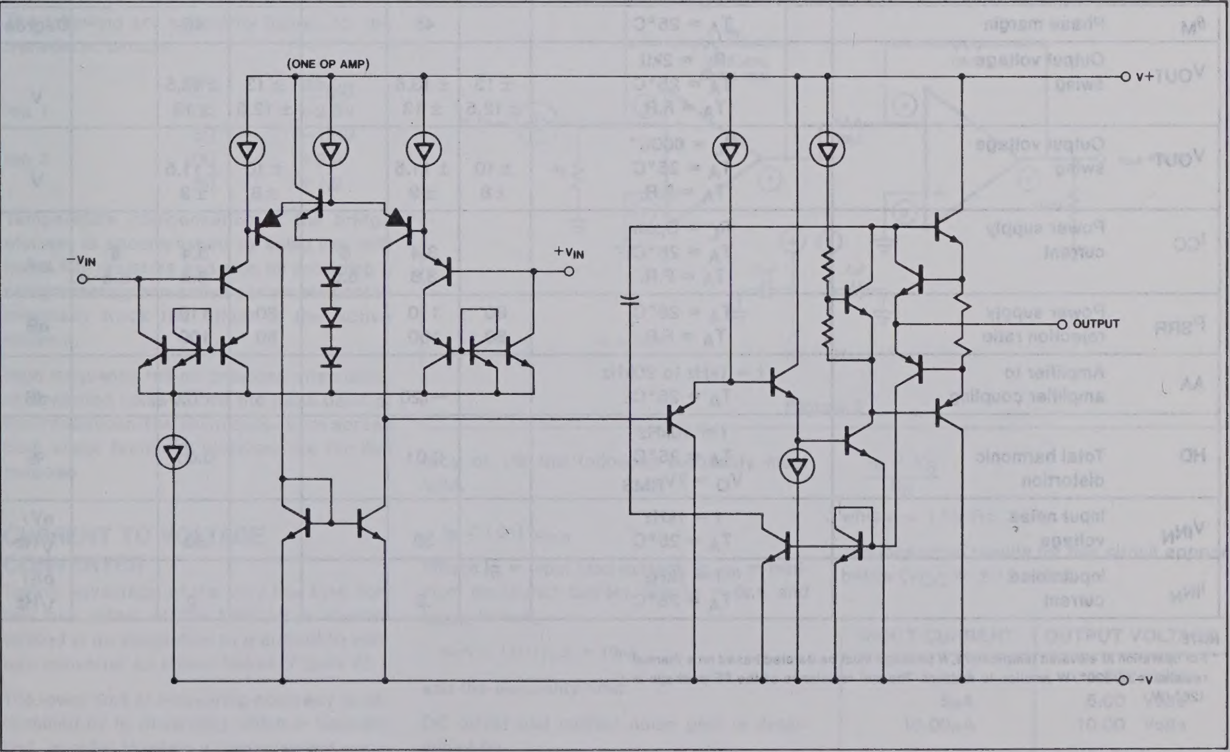


ORDER PART NO.
NE/SE5512N
NE/SE5512FE
NE5512D

ABSOLUTE MAXIMUM RATINGS

	Parameter	Rating	Unit
V_{CC}	Supply Voltage	± 16	V
V_D	Power dissipation	500	mW
T_A	Operating temperature range		
	NE5512	0 to 70	°C
	SE5512	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature soldering	300	°C

EQUIVALENT SCHEMATIC



ELECTRICAL PERFORMANCE CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = −55°C to +125°C (SE), 0°C to +70°C (NE)

PARAMETER		TEST CONDITIONS	SE5512			NE5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$ $T_A = +25°C$ T_A = F.R.		0.7 1	1.5 2.5		1 1.5	3 4	mV
I_{OS}	Input offset current	$R_S = 100k\Omega$ $T_A = +25°C$ T_A = F.R.		3 4	10 20		6 8	20 30	nA
I_B	Input bias current	$R_S = 100k\Omega$ $T_A = +25°C$ T_A = F.R.		3 4	10 20		6 8	20 30	nA
R_{IN}	Input resistance Differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$ T_A = F.R.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$ $V_{IN} = \pm 13.5V$ (RM) $T_A = 25°C$ $V_{IN} = \pm 13V$ (F.R.) T_A = F.R.	70	100		70	100		dB
A_{VOL} GAIN	Large-signal voltage gain	$R_L = 2k\Omega$ $T_A = 25°C$ $V_O = \pm 10V$ T_A = F.R.	50 25	200		50 25	200		V/mV
S.R.	Slew rate	$T_A = 25°C$	0.6	1			1		V/µs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		1			1		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degree
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ $T_A = 25°C$ T_A = F.R.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$* $T_A = 25°C$ T_A = F.R.	±10 ±8	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open $T_A = 25°C$ T_A = F.R.		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
P_{SRR}	Power supply rejection ratio	$T_A = 25°C$ T_A = F.R.	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz $T_A = 25°C$		−120			−120		dB
HD	Total harmonic distortion	f = 10kHz $T_A = 25°C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V_{INN}	Input noise voltage	f = 1kHz $T_A = 25°C$		30			30		nV/√Hz
I_{INN}	Input noise current	f = 1kHz $T_A = 25°C$		.2			.2		pA/√Hz

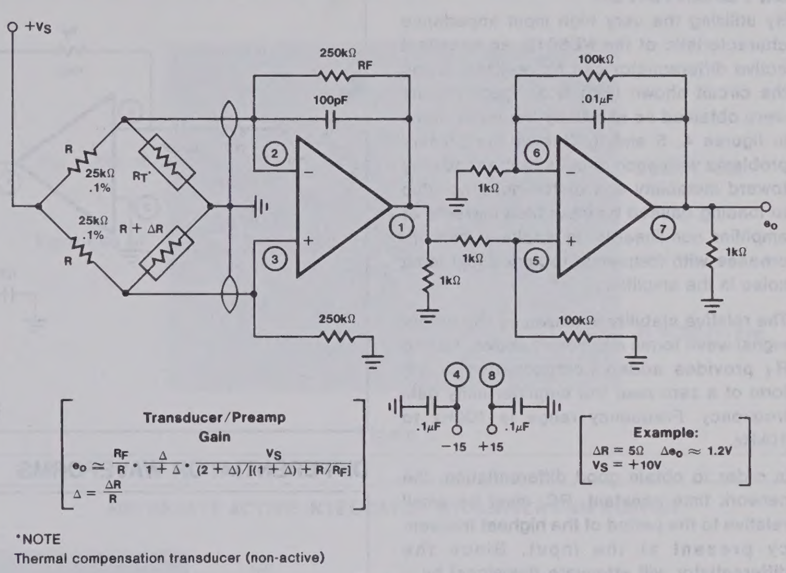
NOTE

* For operation at elevated temperature, N package must be derated based on a thermal resistance of 120°/W junction to ambient. Thermal resistance of the FE package is 125°/W.

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a possible solution to these general requirements (Figure 1).

NE/SE5512 BRIDGE TRANSDUCER AMPLIFIER



Transducer/Preamp Gain

$$e_o \cong \frac{R_F}{R} \cdot \frac{\Delta}{1+\Delta} \cdot \frac{V_S}{(2+\Delta)/[(1+\Delta)+R/R_F]}$$

$$\Delta = \frac{\Delta R}{R}$$

Example:
$\Delta R = 5\Omega$ $\Delta e_o \approx 1.2V$
$V_S = +10V$

*NOTE
Thermal compensation transducer (non-active)

Figure 1

For V_S = 10 volts, the common mode voltage is approximately +5 volts, well within the common mode limits of the NE5512.

The sensitivity of the input stage is approximately

$$\frac{RF \cdot Vs}{2R}$$

to a change in transducer resistance ΔR. This gives a gain factor of ≃50 for V_S = 10V and R = 25kΩ. The second stage gain is ×100 giving a total gain of ≃5000.

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground. Common mode noise rejection is particularly important making matched differential impedance critical. The NE5512 typically provides 100dB of common mode rejection and will considerably reduce this undesirable effect.

The following are sensitivity figures for the transducer circuits.

	ΔR	ΔE_{out}
leg 1	10Ω	−2.6V
	5Ω	−1.3V
leg 2	10Ω	+2.4
	5Ω	+1.2

Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

CURRENT TO VOLTAGE CONVERTER

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in its adaptation to a current to voltage converter as shown below (Figure 2).

NE/SE5512 CURRENT TO VOLTAGE CONVERTER WITH 1% ACCURACY [SENSITIVITY: 1 VOLT PER MICROAMP]

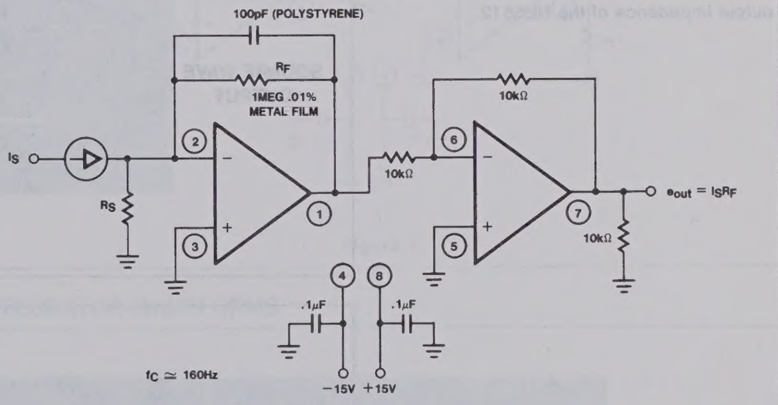


Figure 2

The lower limit of measuring accuracy is determined by I_B (inverting) which is typically 6nA. In order to attain a measurement accuracy of 1% the following inequality must hold,

$$I_B \lesssim (.01)\, I_{Smin}$$

Where I_B = input bias current, I_{Smin} = minimum measured current. For I_B = 6nA and I_{Smin} = 1µA,

$$6nA \lesssim (.01)\, 1\mu A = 10nA$$

and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≃ 1 for $R_S \gg R_F$.

The measured results for this circuit appear below (V_{CC} = ± 15 volts).

INPUT CURRENT	OUTPUT VOLTAGE
1µA	1.008 Volts
5µA	5.00 Volts
10.00µA	10.00 Volts

NE5512 OPERATIONAL DIFFERENTIATOR

By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the wave forms in figures 4, 5 and 6. One of the primary problems with such circuits is the tendency toward instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency requiring low input noise in the amplifier.

The relative stability is shown by the output signal wave forms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC, must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.

NE/SE5512 ACTIVE DIFFERENTIATOR WITH INVERTING ×10 BUFFER

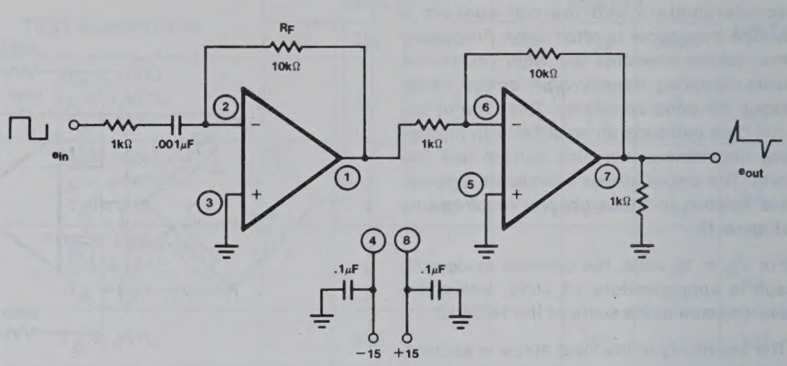


Figure 3

DIFFERENTIATOR WAVEFORMS

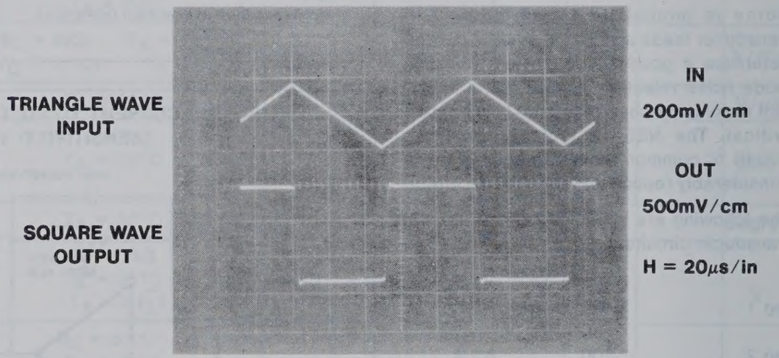


Figure 4

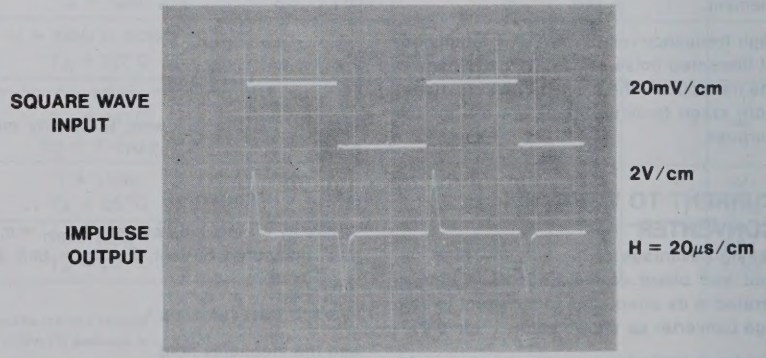


Figure 5

THE OPERATIONAL INTEGRATOR

The operational compliment of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). To obtain satisfactory integration the time constant must fulfill the following requirement:

$$RC \geqq 15T$$

Where T is the period of the input wave form. For the ideal integrator

$$e_{out} = \frac{1}{RC} \int e_{in}\, dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The wave forms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of $\geqq 89°$ for sine wave input over the active frequency range. For a square wave the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

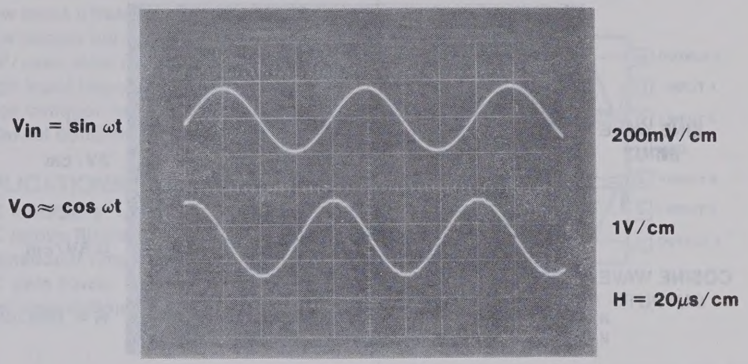


Figure 6

NE/SE5512 ACTIVE INTEGRATOR WITH INVERTING BUFFER

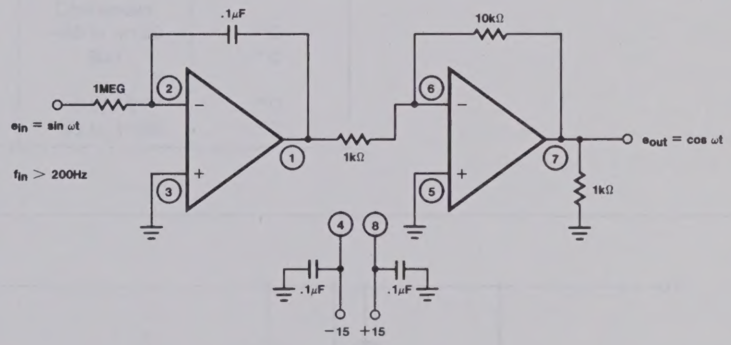


Figure 7

INTEGRATOR WAVEFORMS

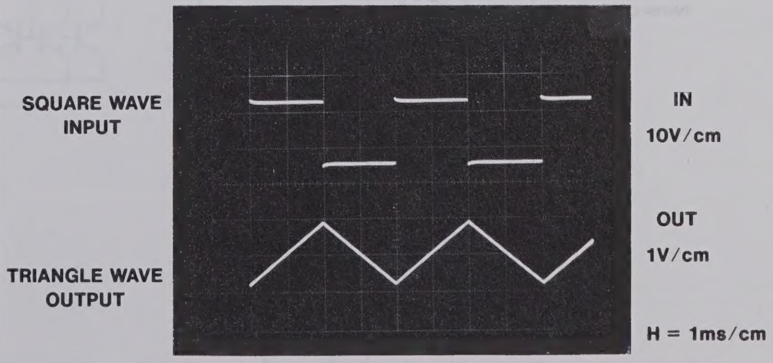


Figure 8

INTEGRATOR WAVEFORMS

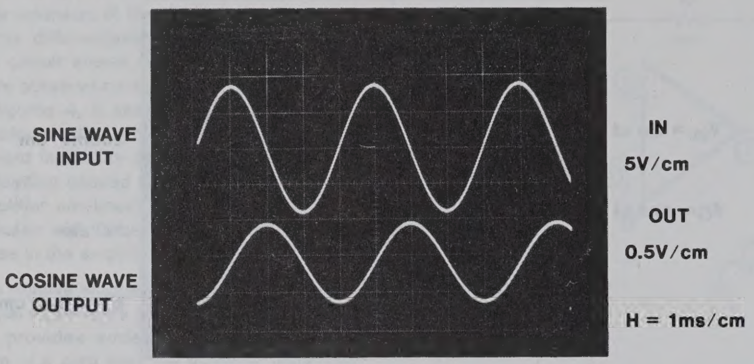


Figure 9

QUAD HIGH PERFORMANCE OP AMP NE/SE5514

NE/SE5514-F,N

DESCRIPTION

The NE/SE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pin-out is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FEATURES

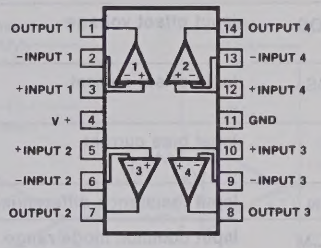
- Low input bias current: $< \pm 3$nA
- Low input offset current: $< \pm 3$nA
- Low input offset voltage: <1mV
- Low supply current: 1.5mA/Amp
- 1 V/μsec slew rate
- High input impedance: 100MΩ
- High common mode impedance: 10GΩ
- Internal compensation for unity gain

APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Instrumentation amplifier

PIN CONFIGURATION

F,N PACKAGE

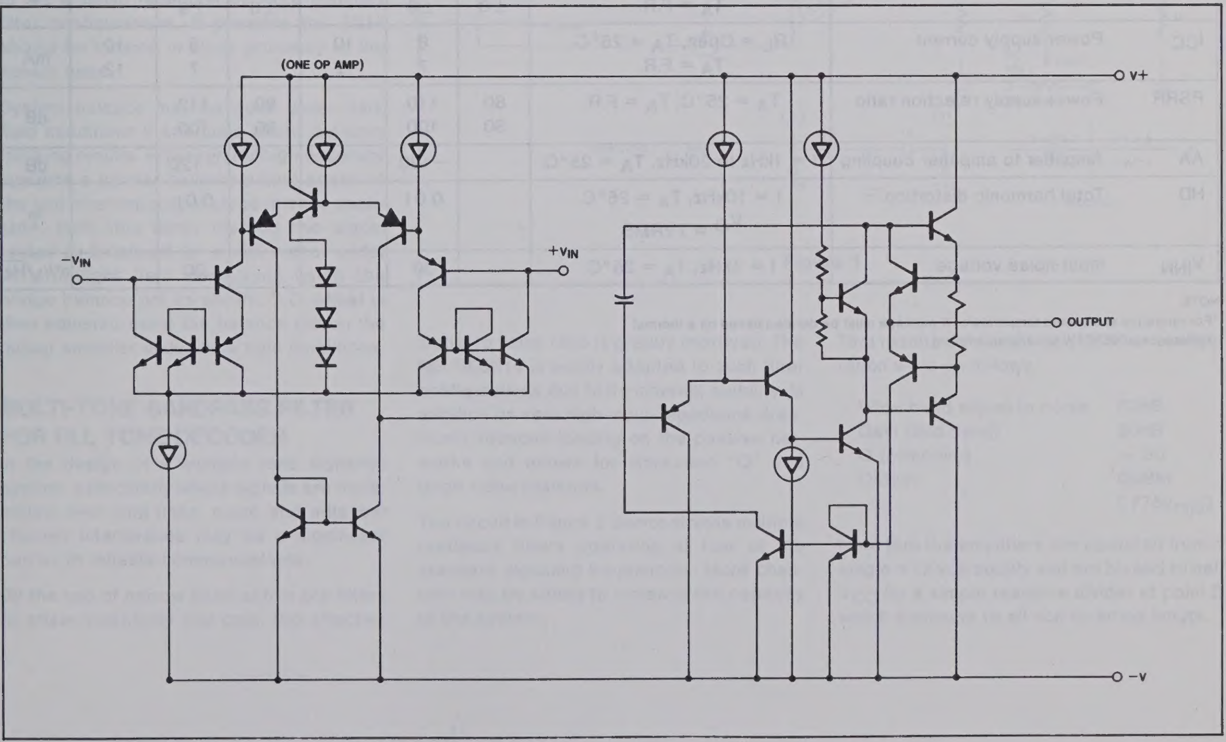

OUTPUT 1
−INPUT 1
+INPUT 1
V +
+INPUT 2
−INPUT 2
OUTPUT 2
1
2
3
4
5
6
7
14
13
12
11
10
9
8
OUTPUT 4
−INPUT 4
+INPUT 4
GND
+INPUT 3
−INPUT 3
OUTPUT 3

ORDER PART NO.
NE5514F,N
SE5514F,N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
TS	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature	300	°C
T_A	Operating temperature range		
	NE5514	0 to 70	°C
	SE5514	−55 to +125	°C

EQUIVALENT SCHEMATIC


(ONE OP AMP)
−VIN
+VIN
V+
OUTPUT
−V

NE / SE5514-F,N

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = −55°C to +125°C (SE) 0°C to 70°C (NE)

	PARAMETER	TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$, $T_A = +25°C$, T_A = F.R.		0.7 1	2 3		1 1.5	5 6	mV
I_{OS}	Input offset current	$R_S = 100k\Omega$, $T_A = +25°C$, T_A = F.R.		3 4	10 20		6 8	20 30	nA
I_B	Input bias current	$R_S = 100k\Omega$, $T_A = +25°C$, T_A = F.R.		3 4	10 20		6 8	20 30	nA
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$, T_A = F.R.	±13.5 ±13.5	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$, $V_{IN} = \pm 13.5V$ (RM), $T_A = 25°C$, $V_{IN} = \pm 13V$ (F.R.), T_A = F.R.	70	100		70	100		dB
AVOL GAIN	Large-signal voltage gain	$R_L = 2k\Omega$, $T_A = 25°C$ $V_C = \pm 10V$, T_A = F.R.	50 25	200		50 25			V/mV
S.R.	Slew rate	$T_A = 25°C$	0.6	1		0.6			V/μs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		1			1		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degr
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $T_A = 25°C$ T_A = F.R.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$*, $T_A = 25°C$ T_A = F.R.	±10 ±8	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open, $T_A = 25°C$ T_A = F.R.		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio	$T_A = 25°C$, T_A = F.R.	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		−120			−120		dB
HD	Total harmonic distortion	f = 10kHz, $T_A = 25°C$ V_O = 7VRMS		0.01			0.01		%
V_{INN}	Input-noise voltage	f = 1kHz, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$

NOTE

*For operation at elevated temperature, N package must be derated based on a thermal resistance of 95°C/W junction to ambient.

FOUR QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photoconductive mode (reverse biased) very small currents in the micro ampere range must be sensed in the photo active operating region. Dark currents in the nano amperes are common. Generally, for this reason, J-FET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6na) to allow its use under these circuit constraints as shown in a possible design used to sense four quadrant motion of a light source. By proper summing of the signals from the X and Y axes, four quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation. (See figure 1).

The wide input common mode voltage range of the device allows a +10 volt supply to be used to drive the signal bridge giving high sensitivity and improved signal to noise. Obviously, input balancing is critical to achieving common mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. D.C. offset is then adjusted using the balance pot on the output amplifier under dark field conditions.

FOUR QUADRANT PHOTO DETECTOR

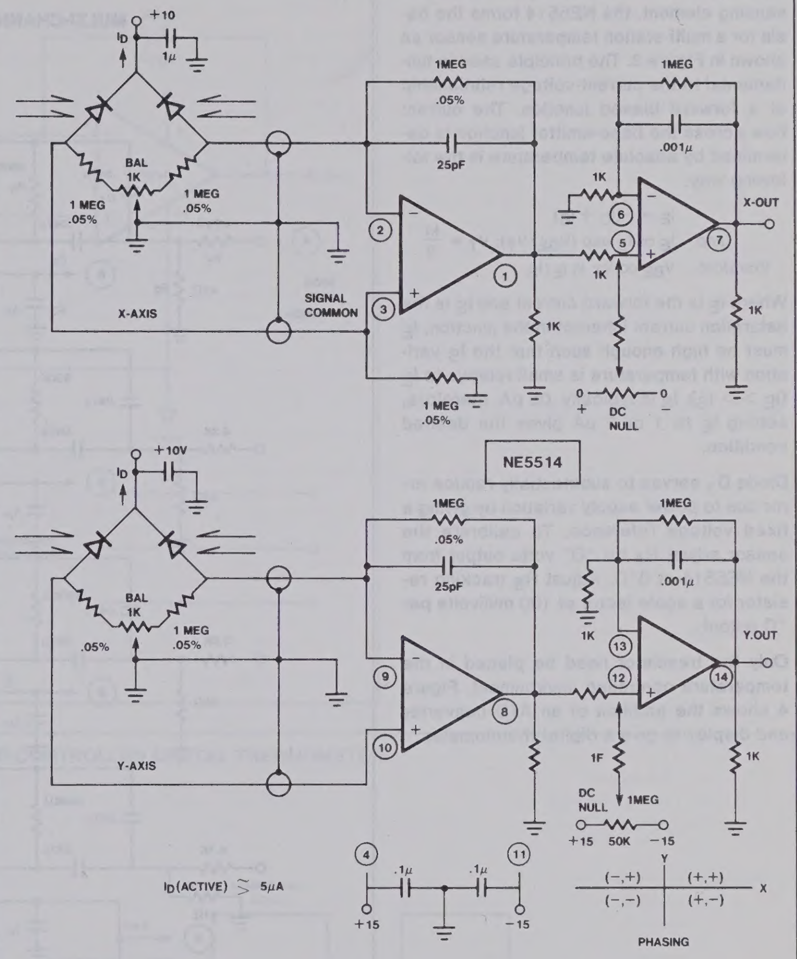


Figure 1

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications.

By the use of narrow band active pre-filters to attain selectivity and gain, the effective signal to noise ratio is greatly improved. The NE/SE5514 is easily adapted to such filter configurations due to its inherent stability. In addition its very high input impedance drastically reduces loading on the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 2 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from this filter configuration were as follows:

Wide band signal to noise	63dB
Gain (Mid band)	30dB
Q (effective)	≈ 30
Output	OdBM (.775v_{rms})

Note that the amplifiers are operated from a single +12 volt supply and are biased to half V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

4-STATION 0–50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 3. The principle used is fundamental to the current-voltage relationship of a forward biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

and $I_E \infty I_S \exp(V_{BE}/V_T)$; $V_T = \frac{kt}{q}$

therefore, $V_{BE} \infty V_T \ln I_E/I_S$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E >> I_S$). I_S is typically .05 pA, therefore, setting I_E to 1 or 2 μA gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "O" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100 millivolts per °C output.

Only the transistor need be placed in the temperature controlled environment. Figure 4 shows the addition of an A/D converter and display to give a digital thermometer.

NE/SE5514
MFB BANDPASS FILTER
FOR
MULTI-CHANNEL TONE DECODER

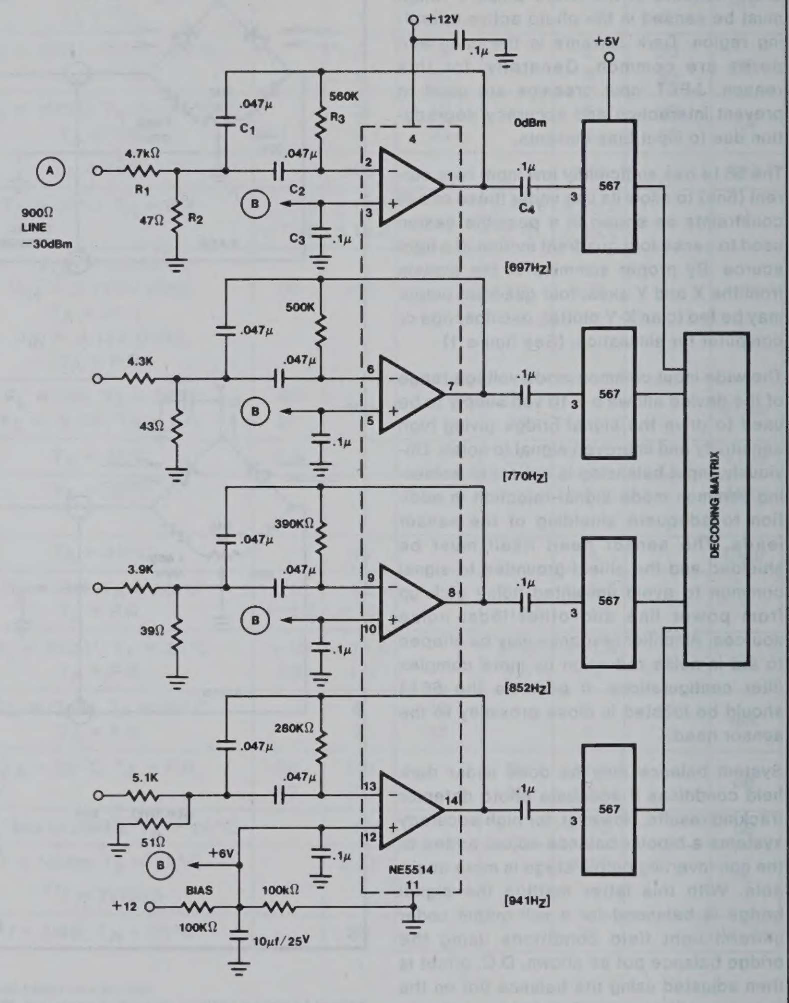

+12V
.1μ
+5V
.047μ
C1
560K
R3
4
0dBm
4.7kΩ
.047μ
A
R1
C2
2
1
.1μ
567
B
3
C4
3
900Ω
LINE
−30dBm
47Ω
R2
C3
.1μ
[697Hz]
500K
.047μ
4.3K
.047μ
6
7
.1μ
567
B
3
43Ω
5
.1μ
[770Hz]
DECODING MATRIX
390KΩ
.047μ
3.9K
.047μ
9
8
.1μ
567
B
3
39Ω
10
.1μ
[852Hz]
280KΩ
.047μ
5.1K
.047μ
13
14
.1μ
567
3
51Ω
12
.1μ
+6V
B
NE5514
11
BIAS
100kΩ
+12
100KΩ
[941Hz]
10μf/25V

Figure 2

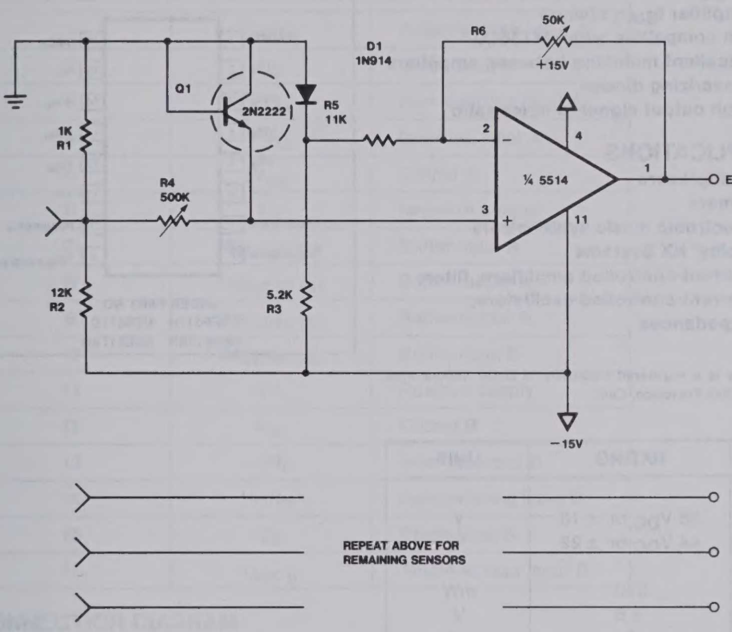

4-CHANNEL TEMPERATURE SENSOR (0–50°C)
Q1
2N2222
D1
1N914
R5
11K
R6
50K
+15V
1K
R1
R4
500K
12K
R2
5.2K
R3
2
3
4
1
11
¼ 5514
Eo
−15V
REPEAT ABOVE FOR REMAINING SENSORS

Figure 3

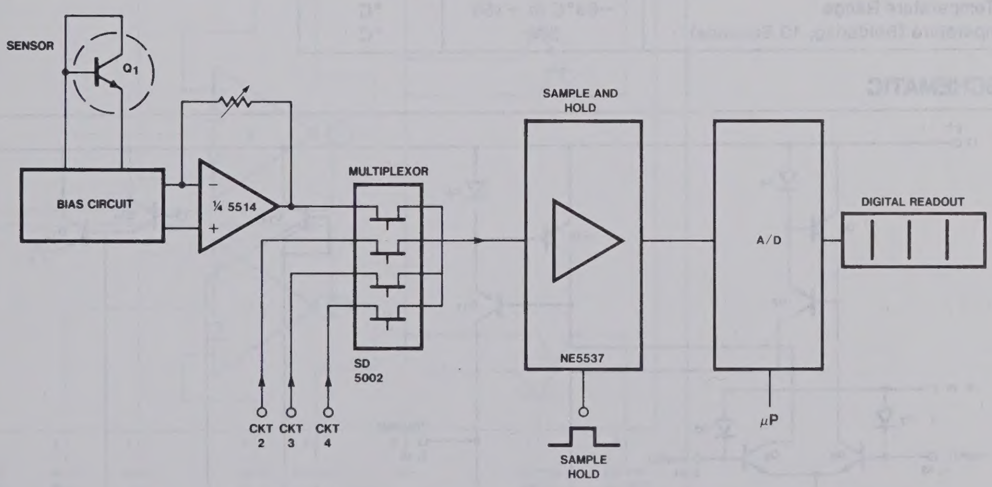

μP-CONTROLLED DIGITAL THERMOMETER
SENSOR
Q_1
BIAS CIRCUIT
¼ 5514
MULTIPLEXOR
SD 5002
CKT 2
CKT 3
CKT 4
SAMPLE AND HOLD
NE5537
SAMPLE HOLD
A/D
μP
DIGITAL READOUT

Figure 4

DESCRIPTION

The NE5517 contains two current controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Constant impedance buffers are provided which effectively eliminate changes in output offset voltage as the amplifier bias current is varied. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal to noise improvement referenced to .5 percent THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

FEATURES

- **Constant impedance buffers**
- **ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change**
- **Pin compatible with LM13600**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **High output signal-to-noise ratio**

APPLICATIONS

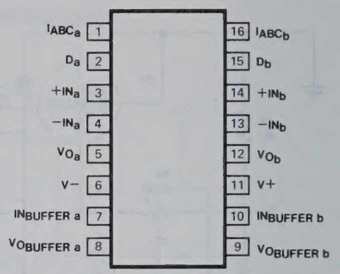
- **Multiplexers**
- **Timers**
- **Electronic music synthesizers**
- **Dolby* HX Systems**
- **Current-controlled amplifiers, filters**
- **Current-controlled oscillators, impedances**

NOTE

*Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

PIN CONFIGURATION

N PACKAGE



I_{ABCa} 1
D_a 2
$+IN_a$ 3
$-IN_a$ 4
V_{Oa} 5
V− 6
IN_{BUFFER} a 7
$V_{OBUFFER}$ a 8
16 I_{ABCb}
15 D_b
14 $+IN_b$
13 $-IN_b$
12 V_{Ob}
11 V+
10 IN_{BUFFER} b
9 $V_{OBUFFER}$ b

ORDER PART NO.

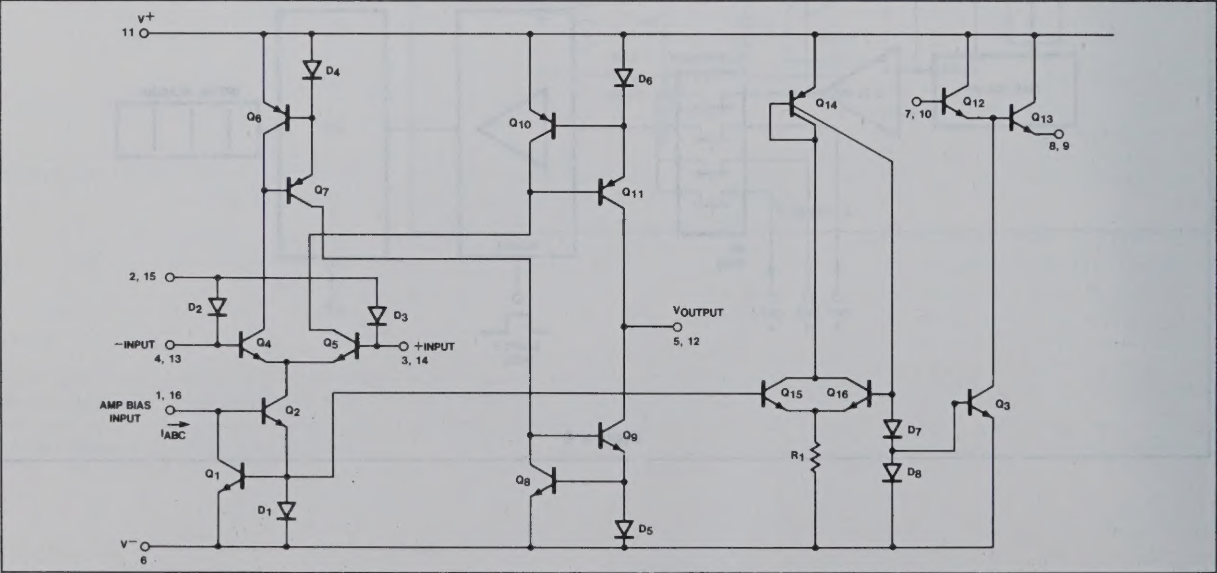
NE5517N NE5517D

NE5517AN NE5517AD

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage[1]		
NE5517	36 V_{DC} or ±18	V
NE5517A	44 V_{DC} or ±22	V
Power Dissipation[2] $T_A = 25°C$		
NE5517N, NE5517AN	570	mW
Differential Input Voltage	±5	V
Diode Bias Current (I_D)	2	mA
Amplifier Bias Current (I_{ABC})	2	mA
Output Short Circuit Duration	Indefinite	
Buffer Output Current[3]	20	mA
Operating Temperature Range		
NE5517N, NE5517AN	0°C to +70	°C
DC Input Voltage	$+V_S$ to $-V_S$	
Storage Temperature Range	−65°C to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C

CIRCUIT SCHEMATIC

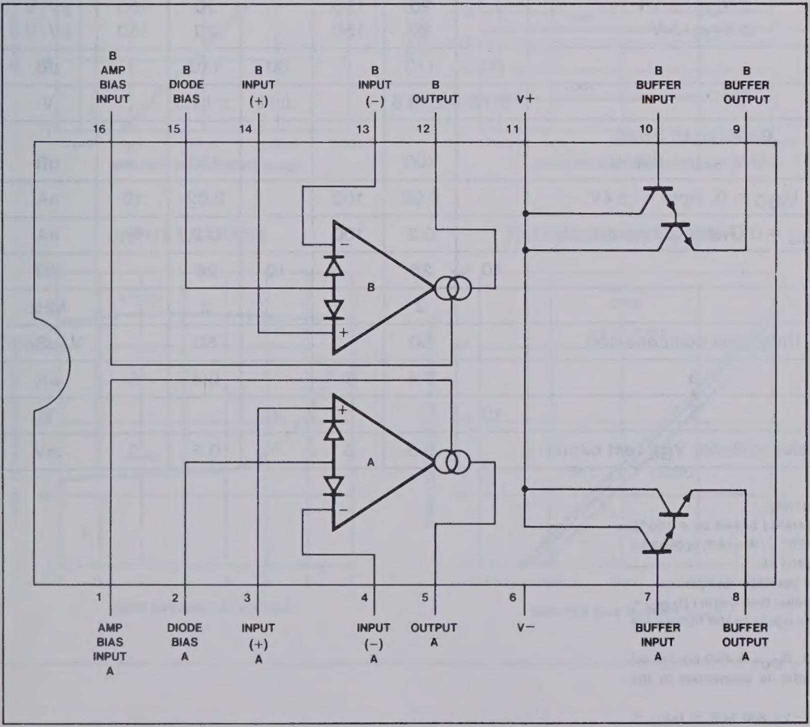


V+
11
D_4
Q_6
Q_7
D_6
Q_{10}
Q_{11}
Q_{14}
7, 10
Q_{12}
Q_{13}
8, 9
2, 15
D_2
D_3
−INPUT
4, 13
Q_4
Q_5
+INPUT
3, 14
V_{OUTPUT}
5, 12
AMP BIAS INPUT
1, 16
I_{ABC}
Q_2
Q_1
D_1
Q_9
Q_8
D_5
Q_{15}
Q_{16}
R_1
D_7
D_8
Q_3
V−
6

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	V_{oa}	Output A
6	V−	negative supply
7	$IN_{Buffer\ (a)}$	Buffer input A
8	$Vo_{Buffer\ (a)}$	Buffer output A
9	$Vo_{Buffer\ (b)}$	Buffer output B
10	$IN_{Buffer\ (b)}$	Buffer input B
11	V+	Positive supply
12	V_{ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

CONNECTION DIAGRAM


B AMP BIAS INPUT
B DIODE BIAS
B INPUT (+)
B INPUT (−)
B OUTPUT
V+
B BUFFER INPUT
B BUFFER OUTPUT
16
15
14
13
12
11
10
9
B
A
+
−
1
2
3
4
5
6
7
8
AMP BIAS INPUT A
DIODE BIAS A
INPUT (+) A
INPUT (−) A
OUTPUT A
V−
BUFFER INPUT A
BUFFER OUTPUT A

ELECTRICAL CHARACTERISTICS[4]

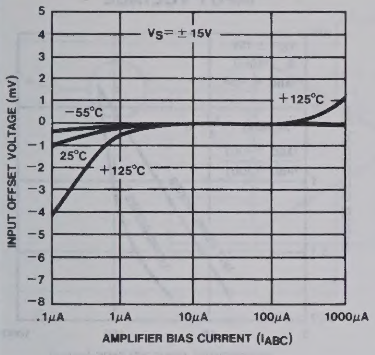
PARAMETER	TEST CONDITIONS	NE5517 Min	NE5517 Typ	NE5517 Max	NE5517A Min	NE5517A Typ	NE5517A Max	UNIT
Input offset voltage (V_{OS})			0.4	5		0.4	2	mV
	Over temperature range						5	mV
	I_{ABC} 5µA		0.3	5		0.3	2	mV
V_{OS} including diodes	Diode bias current (I_D) = 500µA		0.5	5		0.5	2	mV
Input offset change	5µA ≤ I_{ABC} ≤ 500µA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	µA
Input bias current			0.4	5		0.4	5	µA
	Over temperature range		1	8		1	7	µA
Forward Transconductance (gm)		6700	9600	13000	7700	9600	12000	µmho
	Over temperature range	5400			4000			µmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I_{ABC} = 5µA		5		3	5	7	µA
	RL = 0, I_{ABC} = 500µA	350	500	650	350	500	650	µA
	RL = 0,	300			300			µA
Peak output voltage								
Positive	RL = ∞, 5µA ≤ I_{ABC} ≤ 500µA	+12	+14.2		+12	+14.2		V
Negative	RL = ∞, 5µA ≤ I_{ABC} ≤ 500µA	−12	−14.4		−12	−14.4		V
Supply current	I_{ABC} = 500µA, both channels		2.6			2.6		mA
V_{OS} sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	µV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	µV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input[5] 20Hz < f < 20kHz		100			100		dB
Diff. input current	I_{ABC} = 0, input = ±4V		0.02	100		0.02	10	nA
Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/µSec
Buff. input current	5		0.4	5		0.4	5	µA
Peak buffer output voltage	5	10			10			V
ΔV_{BE} of buffer	6 Refer to Buffer V_{BE} test circuit		0.5	5		0.5	5	mV

NOTES

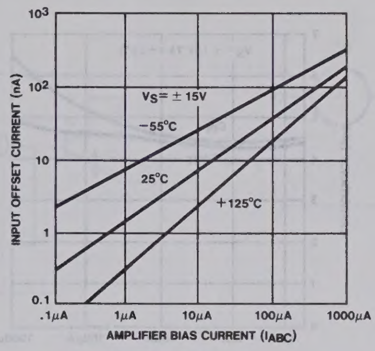
1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.
4. These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500µA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for $V_S = \pm 15V$, I_{ABC} = 500µA, R_{OUT} = 5kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
6. $V_S = \pm 15$, R_{OUT} = 5Ω connected from Buffer output to $-V_S$ and 5µA ≤ I_{ABC} ≤ 500µA.

TYPICAL PERFORMANCE CHARACTERISTICS

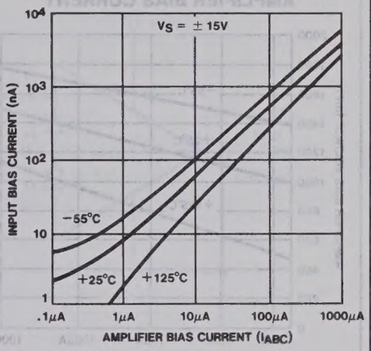
INPUT OFFSET VOLTAGE



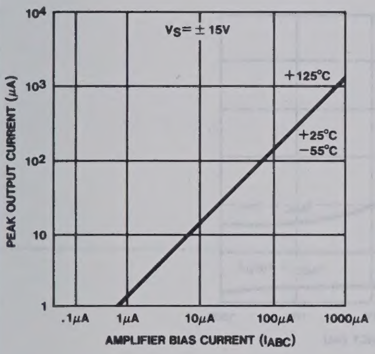
INPUT OFFSET CURRENT



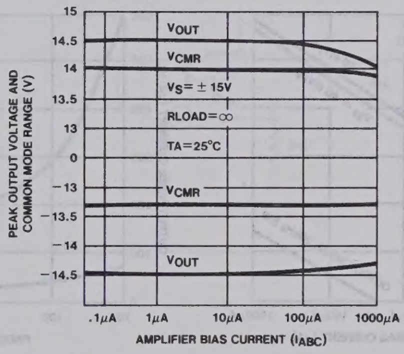
INPUT BIAS CURRENT



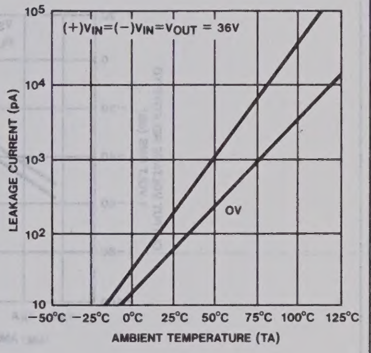
PEAK OUTPUT CURRENT



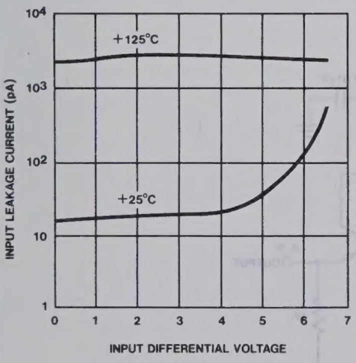
PEAK OUTPUT VOLTAGE AND COMMON MODE RANGE



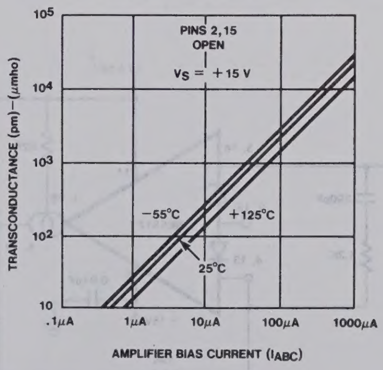
LEAKAGE CURRENT



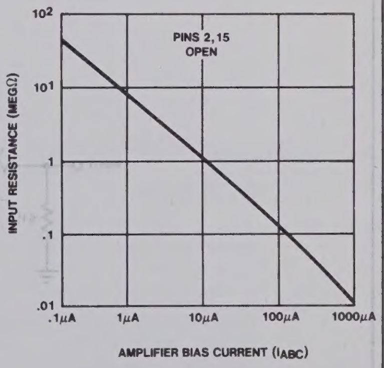
INPUT LEAKAGE



TRANSCONDUCTANCE

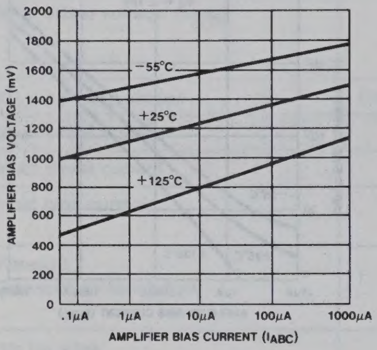


INPUT RESISTANCE

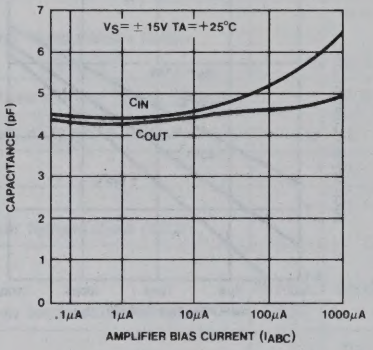


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

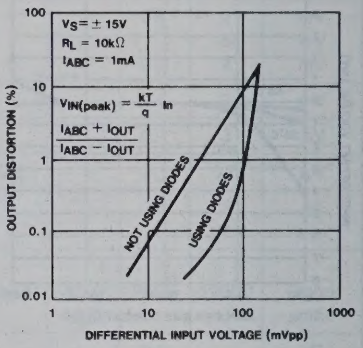
AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT



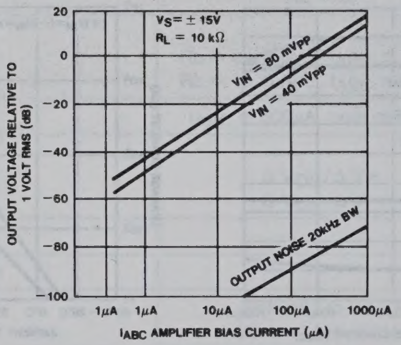
INPUT AND OUTPUT CAPACITANCE



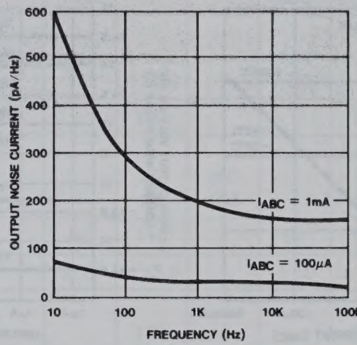
DISTORTION vs DIFFERENTIAL INPUT VOLTAGE



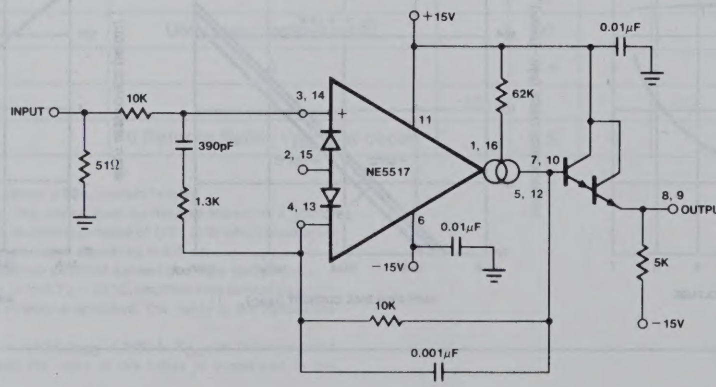
VOLTAGE vs AMPLIFIER BIAS CURRENT



OUTPUT NOISE vs FREQUENCY

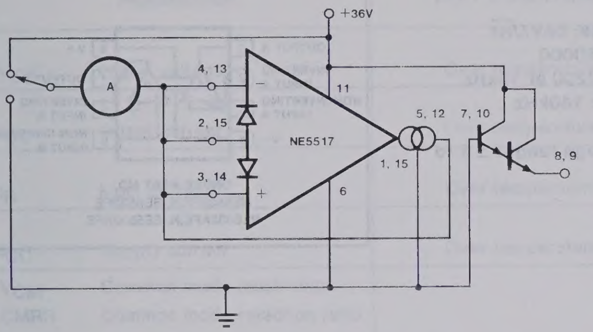


UNITY GAIN FOLLOWER

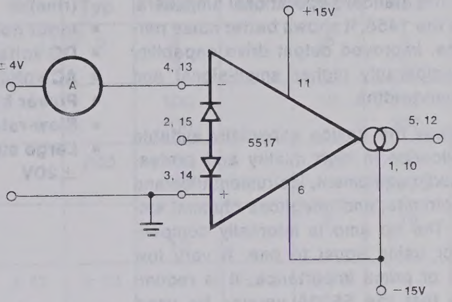

+15V
0.01μF
62K
INPUT
10K
3, 14
+
11
390pF
51Ω
2, 15
1, 16
7, 10
NE5517
5, 12
1.3K
4, 13
8, 9
OUTPUT
6
0.01μF
−15V
5K
10K
−15V
0.001μF

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

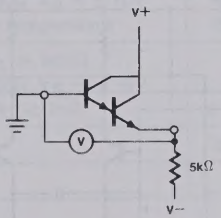
LEAKAGE CURRENT TEST CIRCUIT


+36V
A
4, 13
−
11
2, 15
NE5517
5, 12
7, 10
1, 15
8, 9
3, 14
+
6

DIFFERENTIAL INPUT CURRENT TEST CIRCUIT


+15V
± 4V
A
4, 13
11
2, 15
5517
5, 12
1, 10
3, 14
+
6
−15V

BUFFER V_{BE} TEST CIRCUIT



INTERNALLY COMPENSATED DUAL LOW NOISE OPERATIONAL AMPLIFIER

NE/SE5532/5532A

NE5532/5532A-FE,N, SE5532/5532A-FE

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

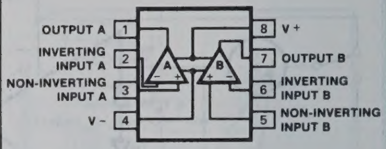
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms)**
- **Input noise voltage: 5nV/$\sqrt{\text{Hz}}$**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew-rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**

PIN CONFIGURATION

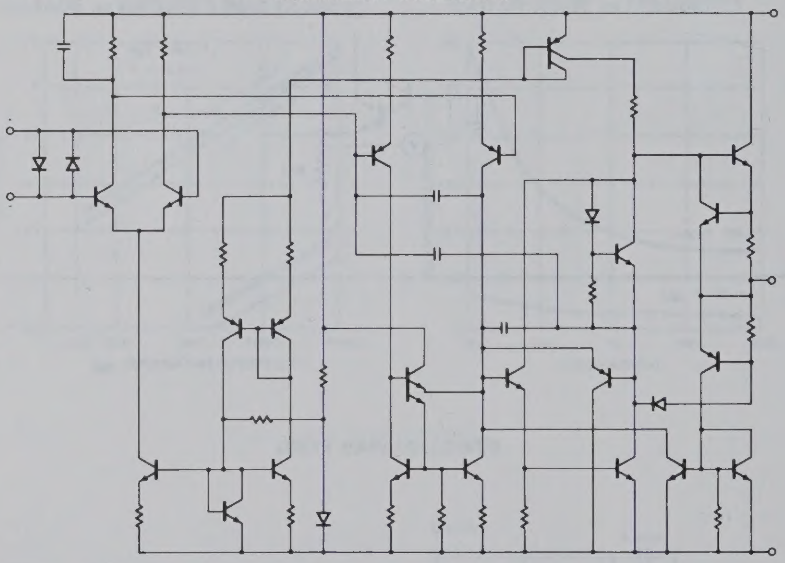
N, FE PACKAGE



ORDER PART NO.
NE5532FE,N, SE5532FE
NE5532AFE,N, SE5532AFE

EACH AMPLIFIER

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation		
	5532FE	1000	mW
	Lead temperature (soldering, 10 sec)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10mA.
2. Thermal resistance of the FE package is 125°C/W.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1, 2]

PARAMETER		TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			.5	2		.5	4	mV
		Over temperature			3			5	mV
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
I_{CC}	Supply current						8	16	mA
		Over temperature			13				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50			25	100		V/mV
		Over temperature	25			15			V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	40			15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$				±12	±13		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$				±15	±16		V
		$R_L \geq 2k\Omega$	±12	±13					V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5532, NE5532A, $T_{Min} = 0°C$, $T_{Max} = 70°C$.
2. For SE5532/5532A, $T_{Min} = -55°C$, $T_{Max} = +125°C$.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

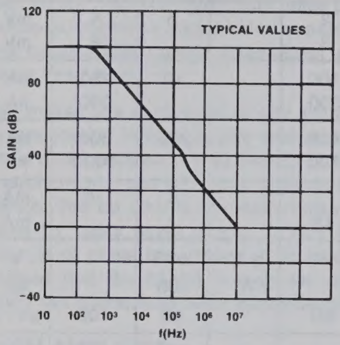
PARAMETER		TEST CONDITIONS	NE/SE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ Closed loop $f = 10kHz$, $R_L = 600\Omega$		0.3		Ω
	Overshoot	Voltage follower $V_{IN} = 100mV$ p-p $C_L = 100pF$ $R_L = 600\Omega$		10		%
	Gain	$f = 10kHz$		2.2		V/mV
	Gain bandwidth product	$C_L = 100pF$ $R_L = 600\Omega$		10		MHz
	Slew rate			9		V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$		140		kHz
		$V_{OUT} = \pm 14V$, $R_L = 600\Omega$, $V_{CC} = \pm 18V$		100		kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

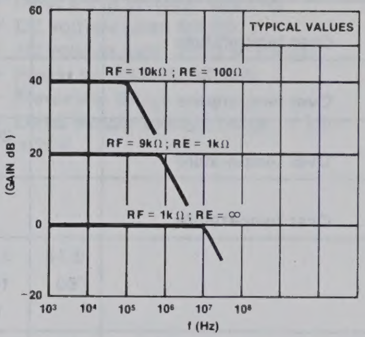
PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30Hz$		8			8	12	$nV/\sqrt{Hz}$
	$f_o = 1kHz$		5			5	6	$nV/\sqrt{Hz}$
Input noise current	$f_o = 30Hz$		2.7			2.7		$pA/\sqrt{Hz}$
	$f_o = 1kHz$		0.7			0.7		$pA/\sqrt{Hz}$
Channel separation	$f = 1kHz$, $RS = 5k\Omega$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

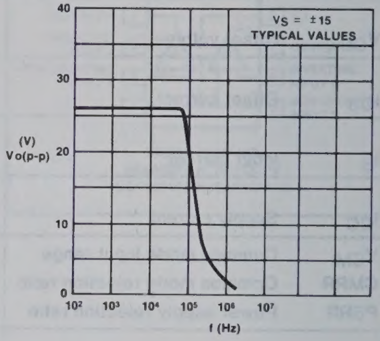
OPEN LOOP FREQUENCY RESPONSE



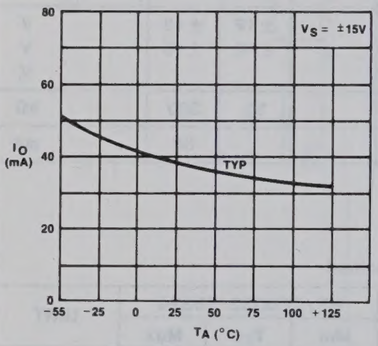
CLOSED LOOP FREQUENCY RESPONSE



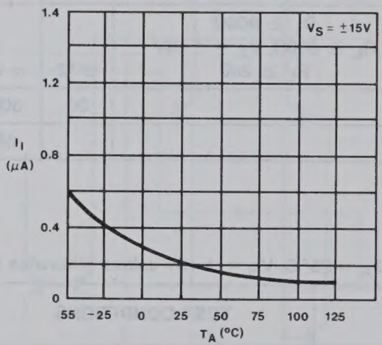
LARGE-SIGNAL FREQUENCY RESPONSE



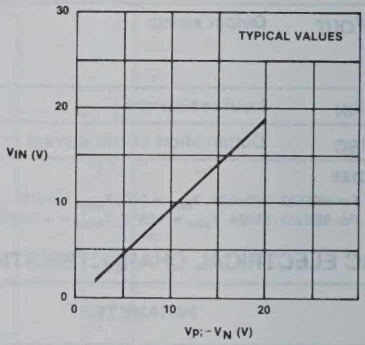
OUTPUT SHORT-CIRCUIT CURRENT



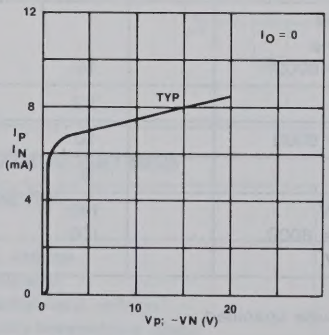
INPUT BIAS CURRENT



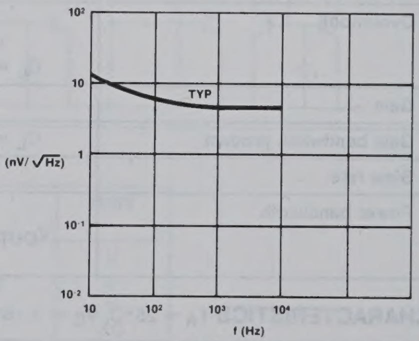
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT

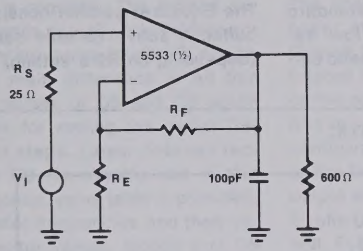


INPUT NOISE VOLTAGE DENSITY

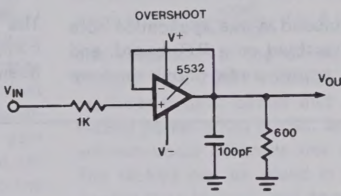


TEST CIRCUITS

CLOSED LOOP FREQUENCY RESPONSE


+
−
5533 (½)
RS
25 Ω
RF
VI
RE
100pF
600 Ω

VOLTAGE FOLLOWER


OVERSHOOT
V+
5532
VIN
1K
−
+
VOUT
600
100pF
V−

APPLICATIONS

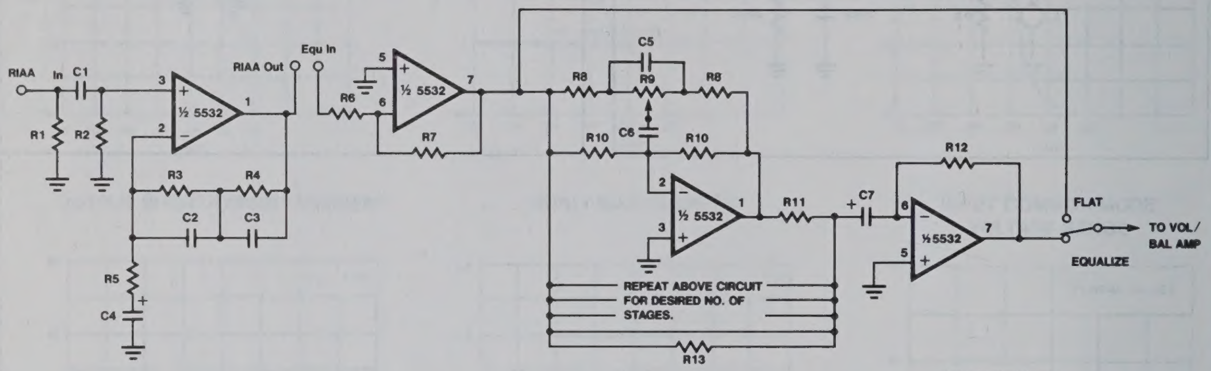
The Signetics 5532 High Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

The circuit included in this application note has been assembled on a P.C. board, and tested with actual audio input devices (Tuner and Turntable). It consists of an RIAA pre-amp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA pre-amp section is a standard compensation configuration with low frequency boost provided by the Magnetic cartridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an

RIAA—EQUALIZER SCHEMATIC



COMPONENT VALUES

R1	47k	C1	.22μF
R2	1meg	C2	750pF
R3	100k	C3	.0033μF
R4	1meg	C4	33μF
R5	1.1k	C5	SEE TABLE
R6	100k	C6	SEE TABLE
R7	100k	C7	2.2μF
R8	SEE TABLE		
R9	(pot) SEE TABLE		
R10	SEE TABLE		
R11	100K		
R12	100K		
R13	20K (5 STAGES)		

COMPONENT VALUE TABLES

R9 = 25k R8 = 2.4k R10 = 240k			R9 = 50 k R8 = 5.1k R10 = 510k			R9 = 100k R8 = 10k R10 = 1 meg		
fo	C5	C6	fo	C5	C6	fo	C5	C6
23 Hz	1μF	.1μF	25 Hz	.47μF	.047μF	12 Hz	.47μF	.047μF
50 Hz	.47μF	.047μF	36 Hz	.33μF	.033μF	18 Hz	.33μF	.033μF
72 Hz	.33μF	.033μF	54 Hz	.22μF	.022μF	27 Hz	.22μF	.022μF
108 Hz	.22μF	.022μF	79 Hz	.15μF	.015μF	39 Hz	.15μF	.015μF
158 Hz	.15μF	.015μF	119 Hz	.1μF	.01μF	59 Hz	.1μF	.01μF
238 Hz	.1μF	.01μF	145 Hz	.082μF	.0082μF	72 Hz	.082μF	.0082μF
290 Hz	.082μF	.0082μF	175 Hz	.068μF	.0068μF	87 Hz	.068μF	.0068μF
350 Hz	.068μF	.0068μF	212 Hz	.056μF	.0056μF	106 Hz	.056μF	.0056μF
425 Hz	.056μF	.0056μF	253 Hz	.047μF	.0047μF	126 Hz	.047μF	.0047μF
506 Hz	.047μF	.0047μF	360 Hz	.033μF	.0033μF	180 Hz	.033μF	.0033μF
721 Hz	.033μF	.0033μF	541 Hz	.022μF	.0022μF	270 Hz	.022μF	.0022μF
1082 Hz	.022μF	.0022μF	794 Hz	.015μF	.0015μF	397 Hz	.015μF	.0015μF
1588 Hz	.015μF	.0015μF	1191 Hz	.01μF	.001μF	595 Hz	.01μF	.001μF
2382 Hz	.01μF	.001μF	1452 Hz	.0082μF	820pF	726 Hz	.0082μF	820pF
2904 Hz	.0082μF	820pF	1751 Hz	.0068μF	680pF	875 Hz	.0068μF	680pF
3502 Hz	.0068μF	680pF	2126 Hz	.0056μF	560pF	1063 Hz	.0056μF	560pF
4253 Hz	.0056μF	560pF	2534 Hz	.0047μF	470pF	1267 Hz	.0047μF	470pF
5068 Hz	.0047μF	470pF	3609 Hz	.0033μF	330pF	1804 Hz	.0033μF	330pF
7218 Hz	.0033μF	330pF	5413 Hz	.0022μF	220pF	2706 Hz	.0022μF	220pF
10827 Hz	.0022μF	220pF	7940 Hz	.0015μF	150pF	3970 Hz	.0015μF	150pF
15880 Hz	.0015μF	150pF	11910 Hz	.001μF	100pF	5955 Hz	.001μF	100pF
23820 Hz	.001μF	100pF	14524 Hz	820pF	82pF	7262 Hz	820pF	82pF
			17514 Hz	680pF	68pF	8757 Hz	680pF	68pF
			21267 Hz	560pF	56pF	10633 Hz	560pF	56pF
						12670 Hz	470pF	47pF
						18045 Hz	330pF	33pF

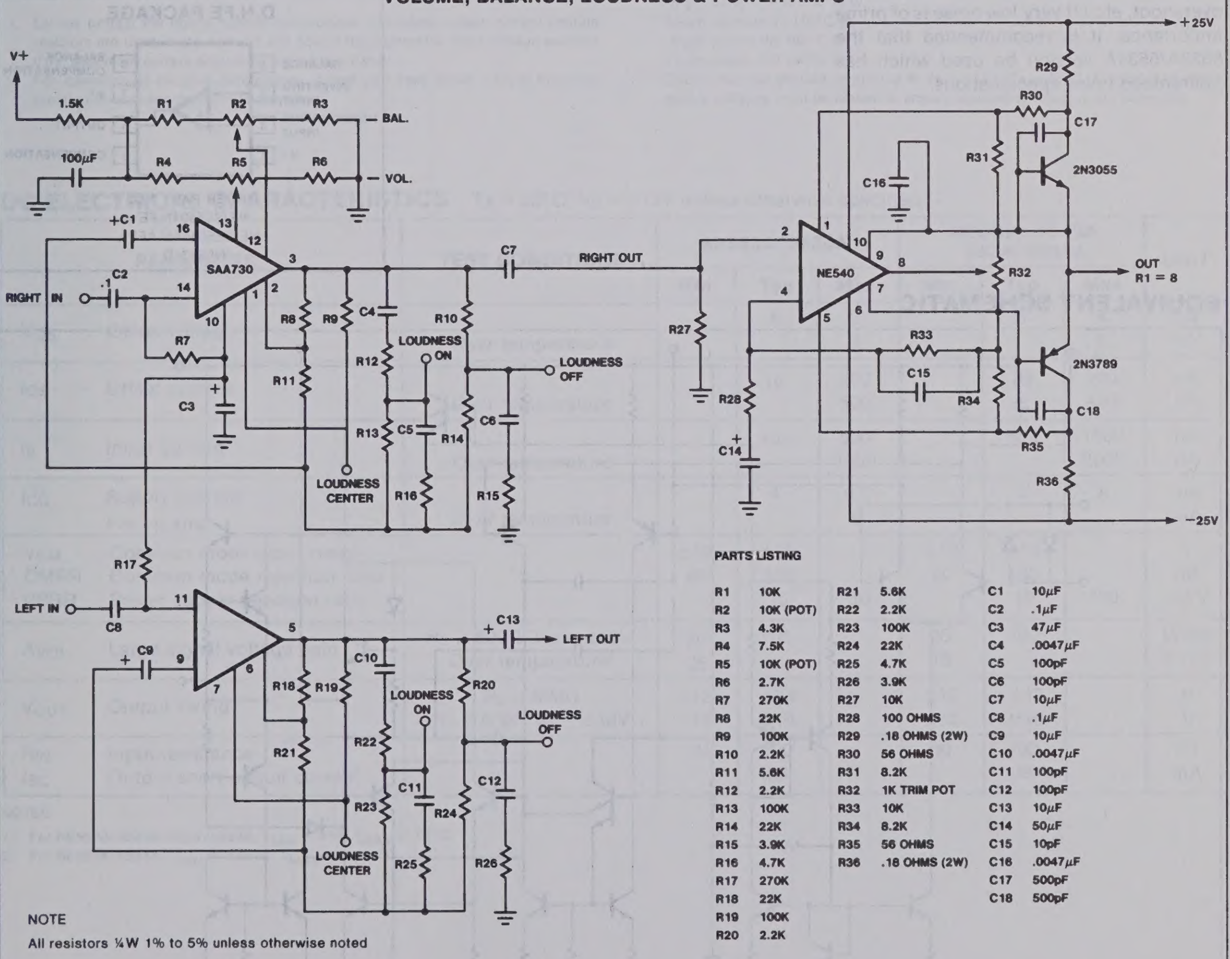
Figure 1

output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the pre amplifiers and the equalizer section. Because the 5532 is internally compensated, no external compensation is required. The 5-band active filter section is actually 5 individual active filters with the same feedback design for all 5. The main differance in all five stages is the values of C5 and C6 which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5 equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

The final stage is the summing amplifier/buffer stage, to sum the individual filters (Figure 2). Note the original signal is subtracted from the sum by a factor dependant on the number of filter stages. This subtraction is necessary to maintain a unity gain configuration at the output with all pots set to the flat position. If R13 were omitted the output with 1 volt at each stage would equal 5 volts (in this case) instead of the desired 1 volt. Full boost and cut using the table values is about ± 15dB. Although 5 bands were chosen for this application, the user may have as many bands as are required. Please note that the subtracting resistor R13, must be adjusted to meet the unity requirement using $R13 = \frac{100K}{\#\ \text{of stages}}$ i.e. 5 stages = 20k.

The remainder of the circuit employs the Philips TCA 730H volume, balance, and loudness-control circuit and the Signetics NE540 power driver circuit, which as shown will net about 35 watts per channel RMS. The NE540 can be found in the Signetics Analog Data Manual, and Applications Manual. Information on the TCA730A may be obtained from Signetics Analog Division.

VOLUME, BALANCE, LOUDNESS & POWER AMPS


V+
1.5K
R1
R2
R3
BAL.
100μF
R4
R5
R6
VOL.
+C1
16
13
12
C2
.1
14
SAA730
3
2
1
10
RIGHT IN
R7
R8
R9
C4
R10
LOUDNESS ON
R11
R12
C3
R13
C5
R14
C6
LOUDNESS OFF
LOUDNESS CENTER
R16
R15
C7
RIGHT OUT
R27
R28
C14
+25V
R29
R30
C17
R31
2N3055
C16
1
2
10
9
8
NE540
4
7
5
6
R32
OUT
R1 = 8
R33
C15
R34
2N3789
C18
R35
R36
−25V
R17
LEFT IN
11
C8
C9
9
5
6
7
C13
LEFT OUT
C10
R18
R19
R20
LOUDNESS ON
LOUDNESS OFF
R21
R22
C11
C12
R23
R24
LOUDNESS CENTER
R25
R26

PARTS LISTING

R1	10K	R21	5.6K	C1	10μF
R2	10K (POT)	R22	2.2K	C2	.1μF
R3	4.3K	R23	100K	C3	47μF
R4	7.5K	R24	22K	C4	.0047μF
R5	10K (POT)	R25	4.7K	C5	100pF
R6	2.7K	R26	3.9K	C6	100pF
R7	270K	R27	10K	C7	10μF
R8	22K	R28	100 OHMS	C8	.1μF
R9	100K	R29	.18 OHMS (2W)	C9	10μF
R10	2.2K	R30	56 OHMS	C10	.0047μF
R11	5.6K	R31	8.2K	C11	100pF
R12	2.2K	R32	1K TRIM POT	C12	100pF
R13	100K	R33	10K	C13	10μF
R14	22K	R34	8.2K	C14	50μF
R15	3.9K	R35	56 OHMS	C15	10pF
R16	4.7K	R36	.18 OHMS (2W)	C16	.0047μF
R17	270K			C17	500pF
R18	22K			C18	500pF
R19	100K				
R20	2.2K				

NOTE

All resistors ¼W 1% to 5% unless otherwise noted

For additional information on the NE540, refer to Signetics Analog Data and Applications Manuals.

For additional information on the SAA730, contact Signetics Analog Division, Philips Representative.

Figure 2

SINGLE AND DUAL LOW NOISE OPERATIONAL AMPLIFIER

NE5533/5533A
NE/SE5534/5534A

NE5533/5533A-N,F • NE/SE5534/5534A-N,FE
NE5534-D

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

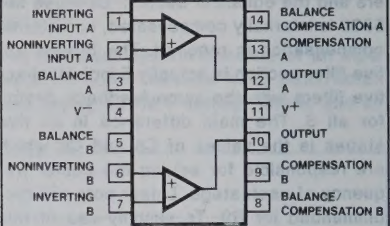
This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_S = \pm 18V$**
- **Input noise voltage: 4nV/$\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

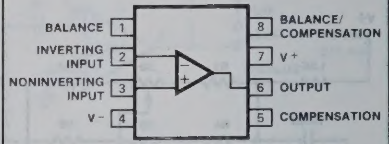
PIN CONFIGURATIONS

F,N PACKAGE


INVERTING INPUT A
1
NONINVERTING INPUT A
2
BALANCE A
3
V−
4
BALANCE B
5
NONINVERTING B
6
INVERTING B
7
14
BALANCE COMPENSATION A
13
COMPENSATION A
12
OUTPUT A
11
V+
10
OUTPUT B
9
COMPENSATION B
8
BALANCE/ COMPENSATION B
−
+

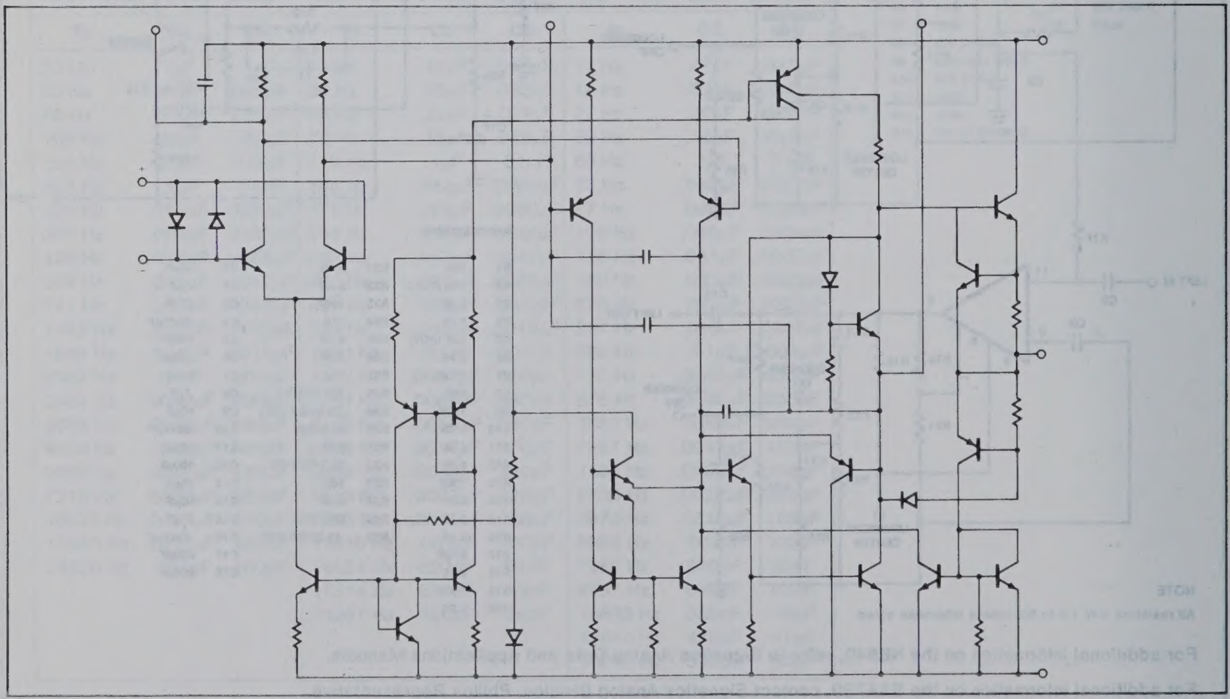
ORDER PART NO.
NE5533N,F
NE5533AN,AF

D,N,FE PACKAGE


BALANCE
1
INVERTING INPUT
2
NONINVERTING INPUT
3
V−
4
8
BALANCE/ COMPENSATION
7
V+
6
OUTPUT
5
COMPENSATION
−
+

ORDER PART NO.
NE/SE5534N,FE
NE/SE5534AN,AFE
NE5534D

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range		
	SE5534/5534A	-55 to +125	°C
	NE5533/5533A/5534/5534A	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533N, 5534N, 5534FE	800	mW
	5533F	1000	mW
	Output short circuit duration[3]	indefinite	
	Lead temperature (soldering 10 sec)	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistances:
   - 8-pin ceramic (FE) 140°C/W
   - 14-pin ceramic (F) 110°C/W
   - 8-pin plastic (N) 162°C/W
   - 14-pin plastic (N) 150°C/W
3. Output may be shorted to ground at $V_S = \pm15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			.5	2		.5	4	mV
		Over temperature			3			5	mV
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
I_{CC}	Supply current Per op amp			4	6.5		4	8	mA
		Over temperature			9				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		$R_L \geq 600\Omega$ $V_S = \pm18V$	±15	±16		±15	±16		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$
2. For SE5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$ unless otherwise specified.

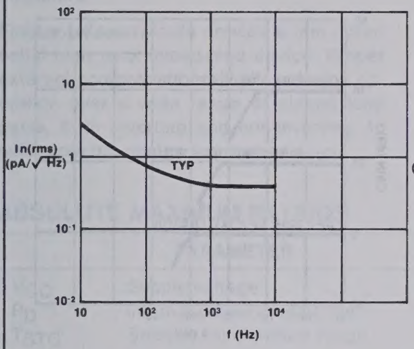
PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ closed loop $f = 10kHz$, $R_L = 600\Omega$, $C_C = 22pF$		0.3			0.3		Ω
Transient response		Voltage follower, $V_{IN} = 50mV$ $R_L = 600\Omega$, $C_C = 22pF$, $C_L = 100pF$							
T_R	Rise time			20			20		ns
	Overshoot			20			20		%
Transient response		$V_{IN} = 50mv$, $R_L = 600\Omega$ $C_C = 47pF$, $C_L = 500pF$							
T_R	Rise time			50			50		ns
	Overshoot			35			35		%
AC	Gain	$f = 10kHz$, $C_C = 0$ $f = 10kHz$, $C_C = 22pF$		6 2.2			6 2.2		V/mV V/mV
	Gain bandwidth product	$C_C = 22pF$, $C_L = 100pF$		10			10		mHz
	Slew rate	$C_C = 0$ $C_C = 22pF$		13 6			13 6		V/μS V/μS
	Power bandwidth	$V_{OUT} = ±10V$, $C_C = 0$ $V_{OUT} = ±10V$, $C_C = 22pF$ $V_{OUT} = ±14V$, $R_L = 600\Omega$ $C_C = 22pF$, $V_{CC} = ±18V$		200 95 70			200 95 70		kHz kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$ unless otherwise specified.

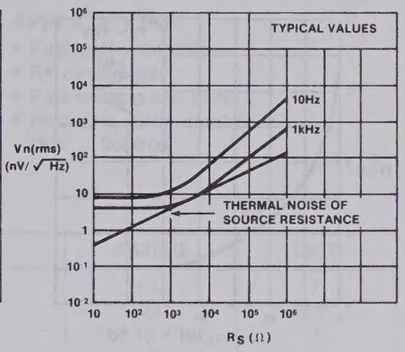
PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30Hz$ $f_o = 1kHz$		7 4			5.5 3.5	7 4.5	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Input noise current	$f_o = 30Hz$ $f_o = 1kHz$		2.5 0.6			1.5 0.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
Broadband noise figure	$f = 10Hz - 20kHz$, $R_S = 5k\Omega$					0.9		dB
Channel separation	$f = 1kHz$, $R_S = 5k\Omega$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

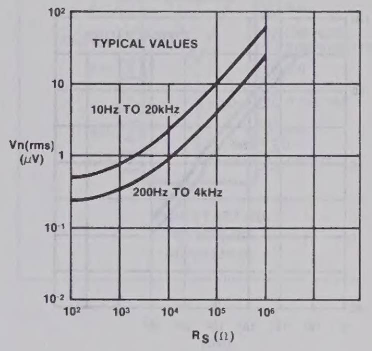
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

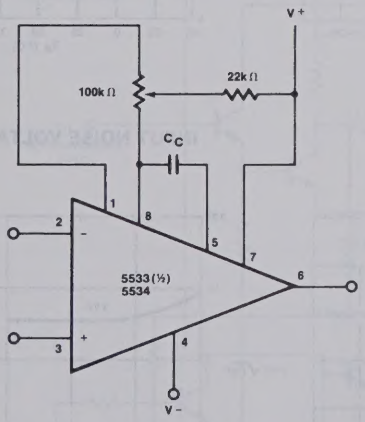


BROADBAND INPUT NOISE VOLTAGE

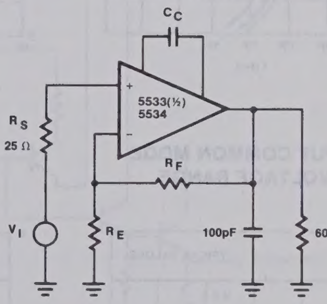


TEST LOAD CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT

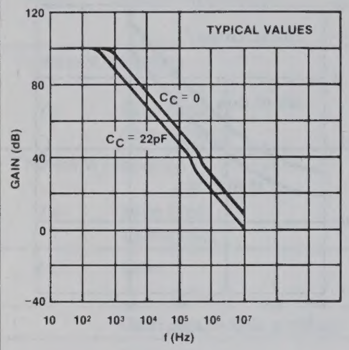

V+
100k Ω
22k Ω
CC
1
8
5
7
6
2
3
4
−
+
5533(½)
5534
V−

CLOSED LOOP FREQUENCY RESPONSE

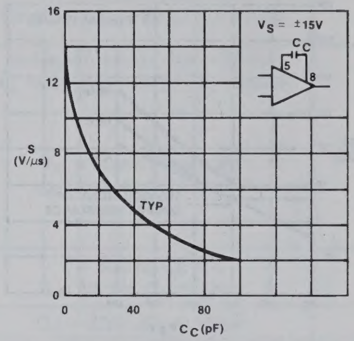

CC
+
−
5533(½)
5534
RS
25 Ω
RF
VI
RE
100pF
600 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

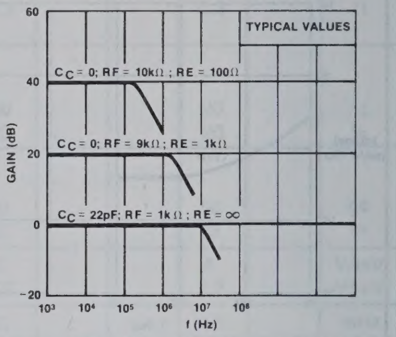
OPEN LOOP FREQUENCY RESPONSE



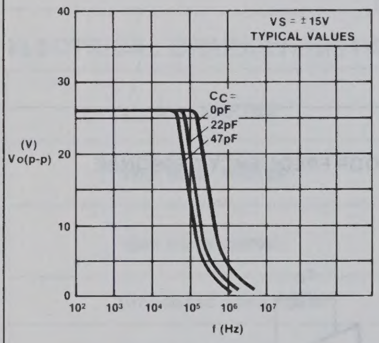
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



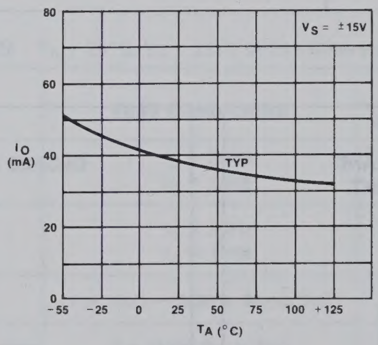
CLOSED LOOP FREQUENCY RESPONSE



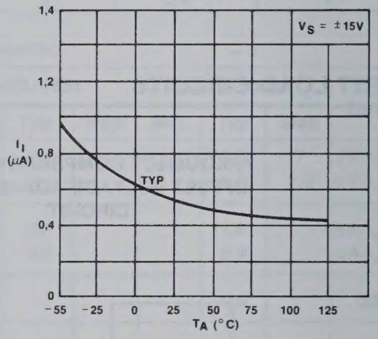
LARGE-SIGNAL FREQUENCY RESPONSE



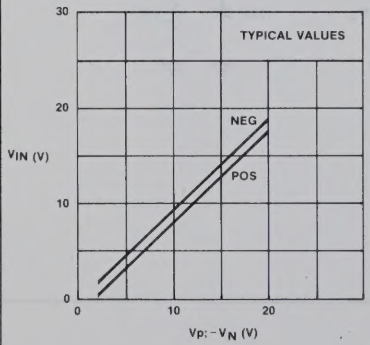
OUTPUT SHORT-CIRCUIT CURRENT



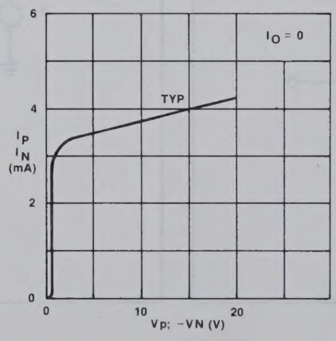
INPUT BIAS CURRENT



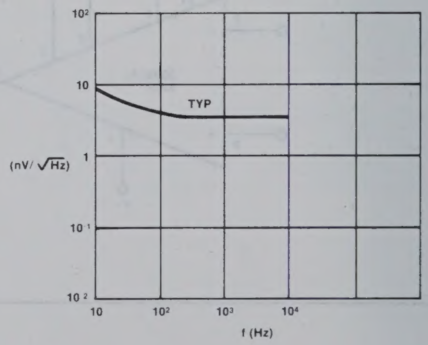
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT PER OP AMP



INPUT NOISE VOLTAGE DENSITY



ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER NE/SE5539

NE / SE5539-F,N

DESCRIPTION

The Signetics NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

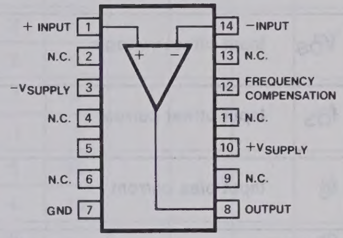
- **Gain bandwidth product: 1.2GHz**
- **Slew rate: 600V/μsec**
- **Full power response: 48MHz**
- **A_{VOL}: 50dB**

APPLICATIONS

- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

PIN CONFIGURATION

F,N PACKAGE



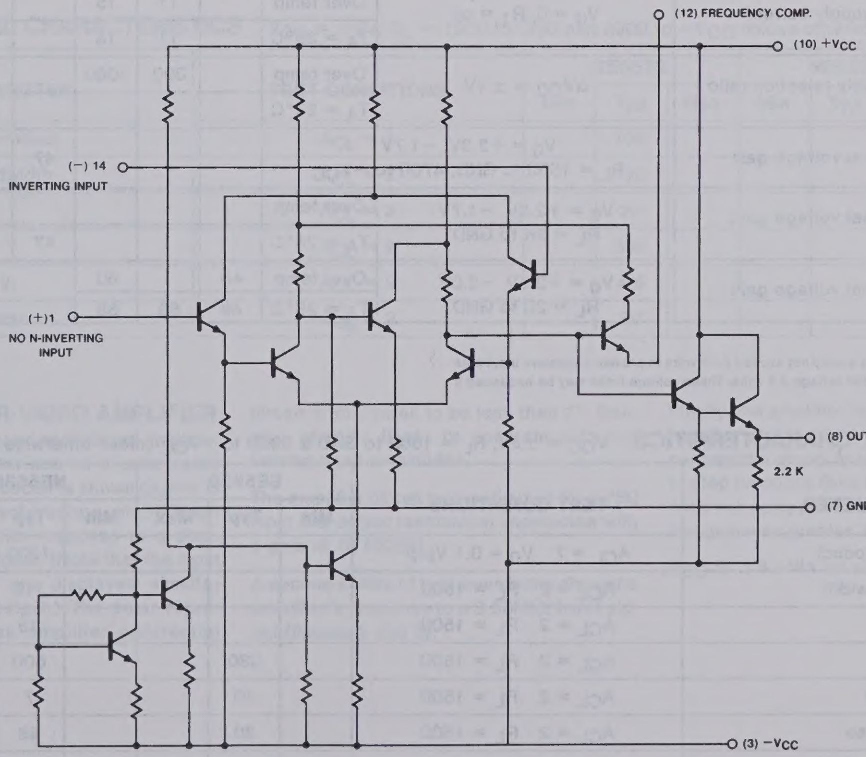
+ INPUT 1
N.C. 2
−V_SUPPLY 3
N.C. 4
5
N.C. 6
GND 7
14 −INPUT
13 N.C.
12 FREQUENCY COMPENSATION
11 N.C.
10 +V_SUPPLY
9 N.C.
8 OUTPUT
+
−

ORDER PART NO.
NE / SE5539F
NE / SE5539N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
	Lead temperature	300	°C

EQUIVALENT CIRCUIT



(12) FREQUENCY COMP.
(10) +V_CC
(−) 14
INVERTING INPUT
(+)1
NO N-INVERTING INPUT
(8) OUTPUT
2.2 K
(7) GND
(3) −V_CC

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS		SE5539 Min	SE5539 Typ	SE5539 Max	NE5539 Min	NE5539 Typ	NE5539 Max	UNIT
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
I_{OS}	Input offset current		Over temp		.1	3				μA
			$T_A = 25°C$		.1	1			2	
I_B	Input bias current		Over temp		6	25				μA
			$T_A = 25°C$		5	13		5	20	
CMRR	Common mode rejection ratio	F = 1 kHz, $R_S = 100\Omega$, $V_{CM} = 1.7V$		70	80		70	85		dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$	+Swing				+2.3	+2.7		V
			−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2\Omega$ to GND	Over temp +Swing	+2.3	+3.0					V
			Over temp −Swing	−1.5	−2.1					
			$T_A = 25°C$ +Swing	+2.5	+3.1					V
			$T_A = 25°C$ −Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$	Over temp		14	18				mA
			$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$	Over temp		11	15				mA
			$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$	Over temp		300	1000				μV/V
			$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2K$ to GND	Over temp							dB
			$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2\Omega$ to GND	Over temp	46		60				dB
			$T_A = 25°C$	48	53	58				

NOTE

1. Differential input voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 390Ω to $-V_{CC}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539 Min	SE5539 Typ	SE5539 Max	NE5539 Min	NE5539 Typ	NE5539 Max	UNIT
Gain bandwidth product	$A_{CL} = 7$ $V_O = 0.1$ Vp-p					1200		MHz
Small signal bandwidth	$A_{CL} = 2$ $R_L = 150\Omega$					110		MHz
Settling time	$A_{CL} = 2$ $R_L = 150\Omega$					15		nSec
Slew rate	$A_{CL} = 2$ $R_L = 150\Omega$		330			600		V/μSec
Propagation delay	$A_{CL} = 2$ $R_L = 150\Omega$		10			7		nSec
Full power response	$A_{CL} = 2$ $R_L = 150\Omega$		20			48		MHz
Full power response	$A_V = 7$, $R_L = 150\Omega$					20		MHz
Wide band noise (RMS)	$B_W = 5MHz$, $R_S = 50\Omega$					5		μV

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 6V$, $T_A = 25°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5				mV
				$T_A = 25°C$		2	3				
I_{OS}	Input offset current			Over temp		.1	3				μA
				$T_A = 25°C$		.1	1				
I_B	Input bias current			Over temp		5	20				μA
				$T_A = 25°C$		4	10				
CMRR	Common mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85					dB
$I_{CC}+$	Positive supply current			Over temp		11	14				mA
				$T_A = 25°C$		11	13				
$I_{CC}-$	Negative supply current			Over temp		8	11				mA
				$T_A = 25°C$		8	10				
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV / V
				$T_A = 25°C$							
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0					V
				−Swing	−1.1	−1.7					
			$T_A = 25°C$	+Swing	+1.5	+2.0					V
				−Swing	−1.4	−1.8					

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$		700					MHz
Small signal bandwidth	$A_{CL} = 2$		120					MHz
Settling time	$A_{CL} = 2$		23					nSec
Slew rate	$A_{CL} = 2$		330					V / μSec
Propagation delay	$A_{CL} = 2$		4.5					nSec
Full power response	$A_{CL} = 2$		20					MHz

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wide band operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown (figure 1) along with the Vectorscope photograph showing the amplifier response to a standard NTSC color signal. (Note that the input reference vectors are displayed simultaneously with the output.) The polar representation indicates amplifier differential phase error overall to be less than 2°. Gain also remains linear or constant with the varying input amplitudes.

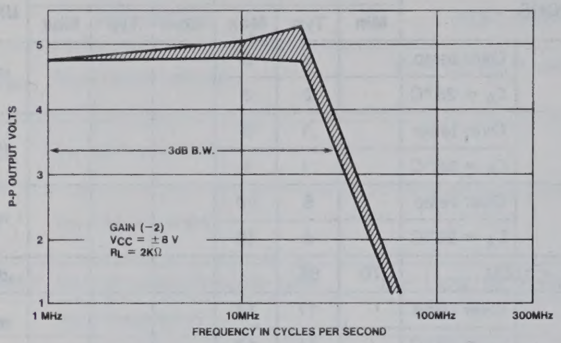
The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of 10 (20dB).

A second series of test waveforms show the amplifier's response to a 3.58MHz burst signal (figures 2 and 3).

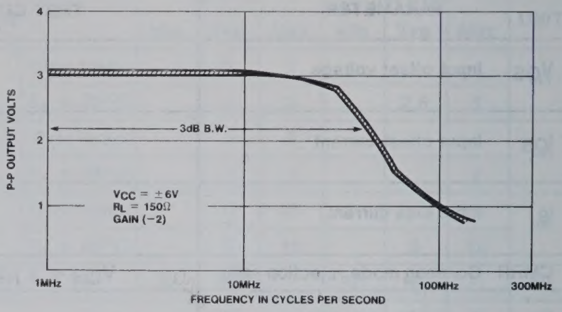
Finally, the amplifier response is shown as a function of time for the NTSC signal with no perceptible droop or overshoot in response to step functions (see figure 4). Note that no external compensation was required since the gain was greater than 7 (17dB).

V_{CC} is ±8 volts for all cases shown.

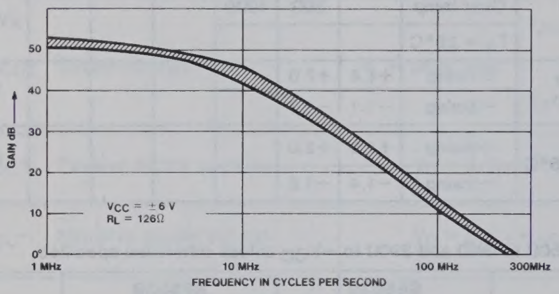
POWER BANDWIDTH (SE)



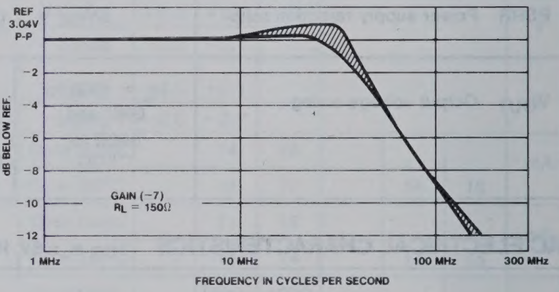
POWER BANDWIDTH (NE)



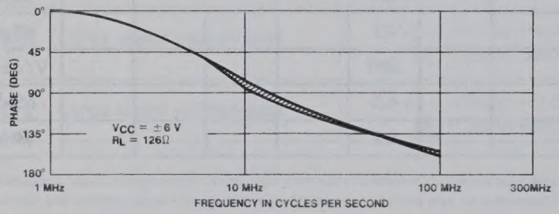
SE5539 OPEN LOOP GAIN vs FREQUENCY



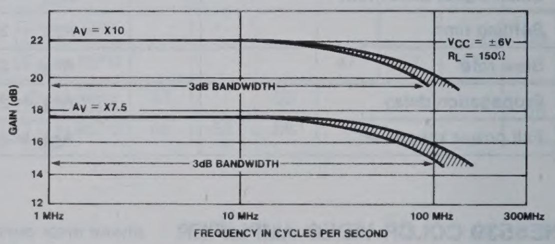
POWER BANDWIDTH



SE5539 OPEN LOOP PHASE vs FREQUENCY



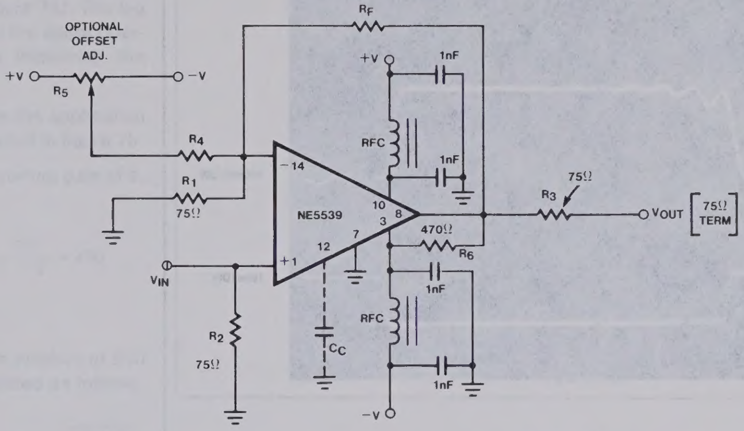
GAIN BANDWIDTH PRODUCT vs FREQUENCY



NOTE

▨ Indicates typical distribution $-55°C \leq T_A \leq 125°C$

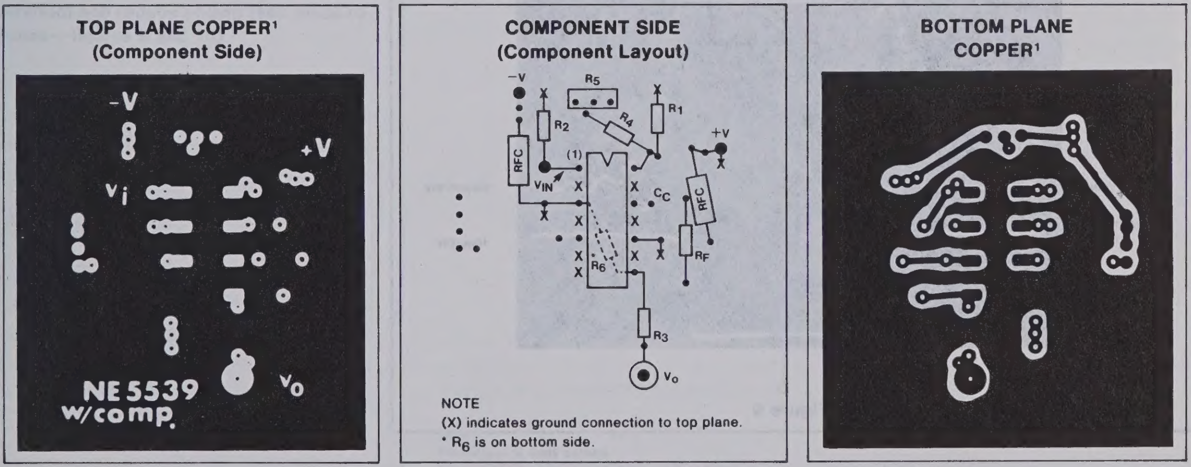
28dB NON-INVERTING AMP
SAMPLE P.C. LAYOUT


RF
OPTIONAL
OFFSET
ADJ.
+V
R5
−V
+V
1nF
RFC
1nF
R4
R1
75Ω
−14
NE5539
10
8
3
7
12
+1
VIN
R2
75Ω
CC
470Ω
R6
1nF
RFC
1nF
−V
75Ω
R3
VOUT
75Ω
TERM

R1 = 75Ω 5% CARBON
R2 = 75Ω 5% CARBON
R3 = 75Ω 5% CARBON
R4 = 36K 5% CARBON

R5 = 20K TRIMPOT (CERMET)
RF = 1.5K (28dB GAIN)
R6 = 470Ω 5% CARBON

RFC 3T # 26 BUSSWIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)


TOP PLANE COPPER[1] (Component Side)

COMPONENT SIDE (Component Layout)

BOTTOM PLANE COPPER[1]

−V
+V
Vi
NE 5539
w/comp.
Vo
−V
R5
R1
R4
R2
RFC
(1)
VIN
X
CC
+V
RFC
RF
R6
R3
Vo

NOTE
(X) indicates ground connection to top plane.
* R6 is on bottom side.

NOTE
[1] Bond edges of top and bottom ground plane copper.

Figure 10

SMALL SIGNAL RESPONSE

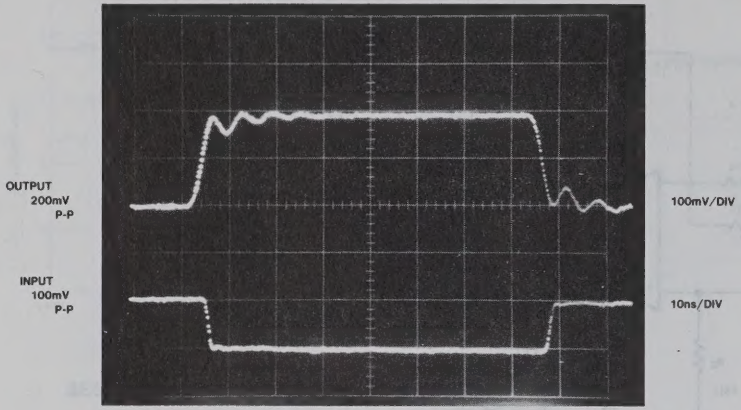


Figure 8

LARGE SIGNAL RESPONSE

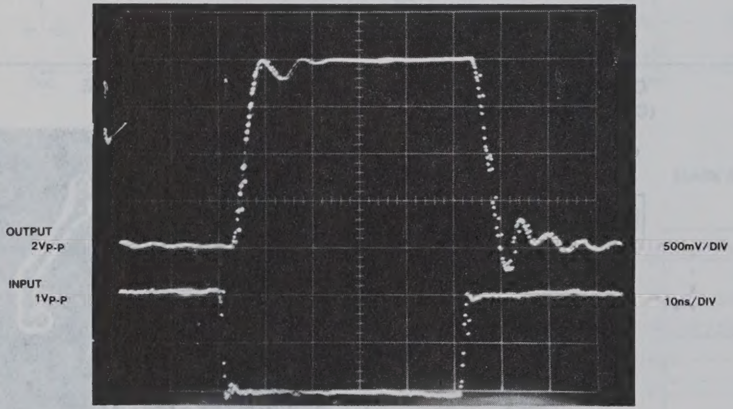


Figure 9

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The primary reasoning behind this procedure is to force the closed loop circuit to appear as a gain of X7 above the critical frequency where phase changes rapidly (approx. 70MHz; refer to figure 7a). The lag network raises the phase at the upper operating frequencies, greatly improving the phase margin.

The calculations below show the application of these principles to the circuit in figure 7b.

The circuit shown has an inverting gain of 2, therefore solving for R_2:

$$R_2 \leq \frac{R_f}{7 - |A_{CL}|} \leq \frac{2K}{7-2} = 400$$

Let $R_2 = 330\Omega$

Assuming a gain band width product of 350 MHz, C_G may now be calculated as follows:

$$\therefore C_G \simeq \frac{5}{\pi \bullet 330 \bullet 350 \bullet 10^6} \simeq \boxed{14\text{pF}}$$

In the circuit shown, a lead compensation capacitor of ≃ 1.6pF was used with a value of R_2 of 330Ω and C_G was a 2 — 20pF trimmer cap (JFD piston-type). Rise and fall times of 2.8 to 3ns were measured in the small signal mode with quite adequate range in the lag compensation trimmer to optimize overshoot and reduce ringing (see pulse response—figures 9 and 10).

INVERTING GAIN OF 7
GAIN-PHASE RESPONSE
(UNCOMPENSATED)

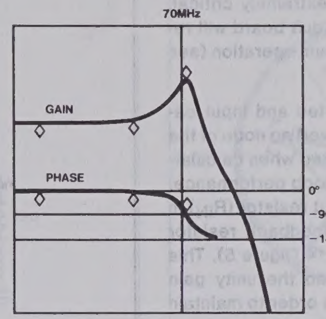
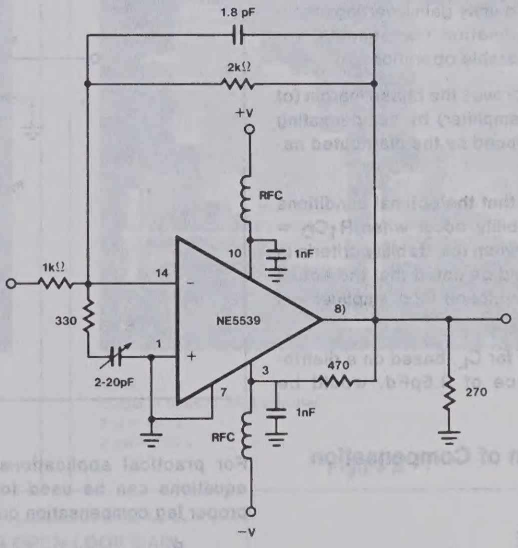


Figure 7a

NE5539
INVERTING GAIN OF 2 AMPLIFIER



Note
Resistors-¼ watt carbon.
RFC-3T #26 buss wire on Ferroxcube VK200 09/3B wideband threaded core.

Figure 7b

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CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. A double-sided printed circuit board will result in more favorable system operation (see figure 10).

The effect of the distributed and input capacitance added by the inverting node of the amplifier must be considered when calculating actual system closed loop performance. The RC product of the input resistor (R_{IN}) in parallel with C_{dist}. and feedback resistor (R_F) create a pole at pin 14 (figure 5). This frequency must fall beyond the unity gain frequency of the system in order to maintain stability and system performance.

CLOSED LOOP GAIN LESS THAN 7

The NE5539 is stable for all closed loop gains greater than seven (7). When operating at gains less than seven (7), the device can become unstable. The circuit in figure 7 is an example of a unity gain inverting amplifier. The compensation components are added to obtain stable operation.

Capacitor C_L improves the phase margin (of the operational amplifier) by compensating for the lag introduced by the distributed capacitor (C_D).

It can be shown that the optimal conditions for amplifier stability occur when $R_1C_D = R_FC_L$; however, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed loop amplifier will be reduced.

The actual value for C_L, based on a distributed capacitance of 3.5pFd, would be $\simeq$ 2pF.

NON-INVERTING BLOCK DIAGRAM

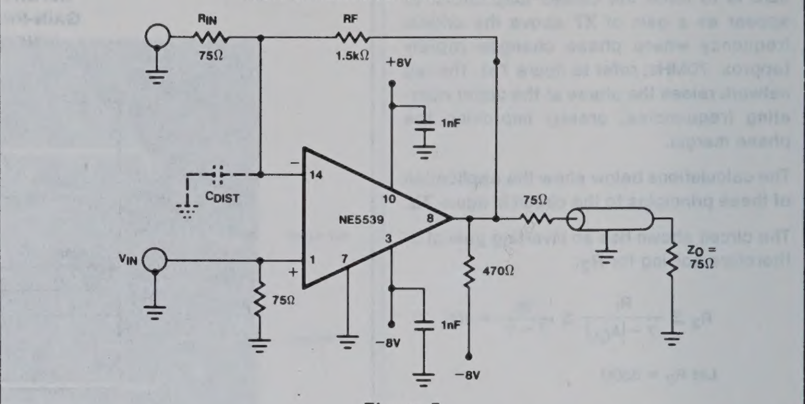

Figure 5

WIDE BAND UNITY GAIN INVERTING AMPLIFIER CIRCUIT IN A 75Ω SYSTEM

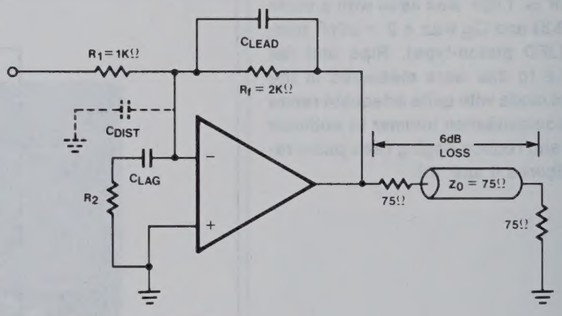

Figure 6

Determination of Compensation Capacitance:

$$C_{lead} = \frac{C_{dist}}{A_{CL}}$$

The above equation defines the relationship between the distributed capacitance, closed loop gain (A_{CL}), and the compensation capacitor (C_L). For closed loop stability and gains less than 5, C_{lead} becomes a practical consideration. When bandwidth is of primary concern, the simple lead compensation will usually be adequate. However, if transient response is also a factor in the design, then a lag compensation network (C_G, R_2) may be necessary.

For practical applications, the following equations can be used to determine the proper lag compensation components:

$$\frac{R_f}{R_1 \| R_2} \geq 7 \qquad \text{(Equation 1)}$$

$$\therefore R_2 \leq \frac{R_f}{7 - A_{CL}} \qquad \text{(Equation 2)}$$

(Using Equation 1 to insure a closed loop gain of X7 above the network break frequency allows you to solve for R_2, the lag network resistor.)

C_{lag} may be approximated by the following equations. First set the lag network break frequency in relation to the amplifier total gain product (open loop).

$$\text{Set } \omega_{lag} \simeq \frac{2\pi \cdot GBW}{10} \text{ rad/sec}$$

$$\simeq \frac{\pi \cdot GBW}{5} \text{ rad/sec,}$$

$$\text{then } \omega_{lag} = \frac{1}{R_2C_{lag}}$$

and C_{lag} may now be determined.

$$\therefore C_{lag} \simeq \frac{5}{\pi \cdot R_2 \cdot GBW}$$

< Assume GBW = 350MHz > (Equation 3)

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NE5539 VIDEO AMPLIFIER

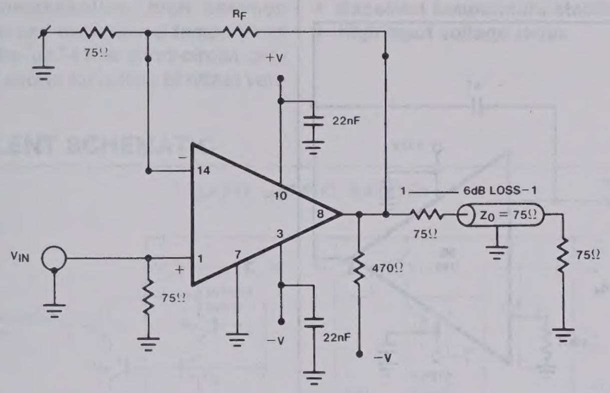

RF
75Ω
+V
22nF
14
10
8
3
1
7
−
+
VIN
75Ω
−V
22nF
−V
470Ω
1 — 6dB LOSS − 1
75Ω
Z0 = 75Ω
75Ω

Figure 1

NE5539 NTSC VECTOR POLAR GRAPH

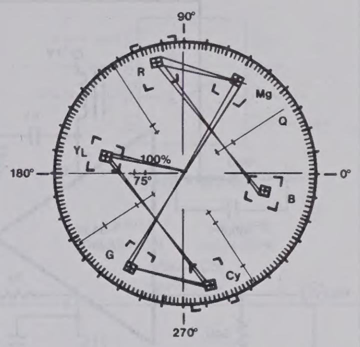
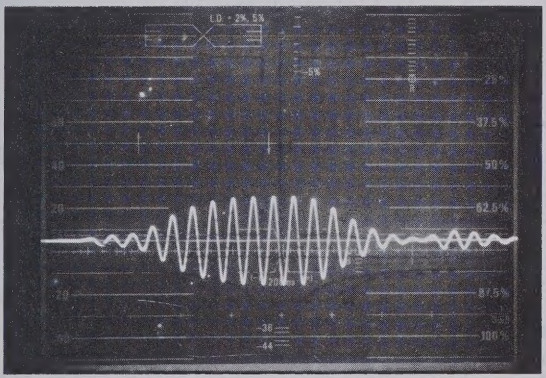


Figure 2

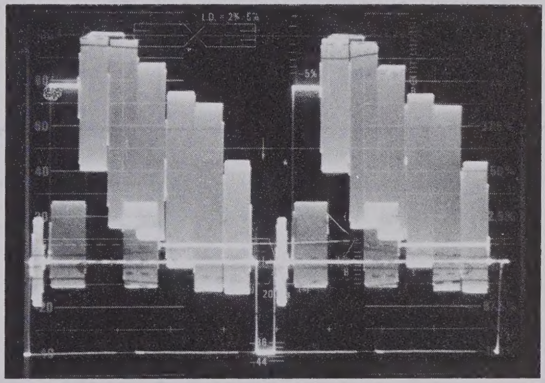
3.58MHz BURST SIGNAL



NOTE
3.58MHz burst through a 5539 20dB amplifier.

Figure 3

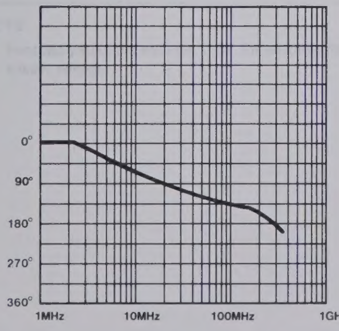
NTSC OUTPUT SIGNAL



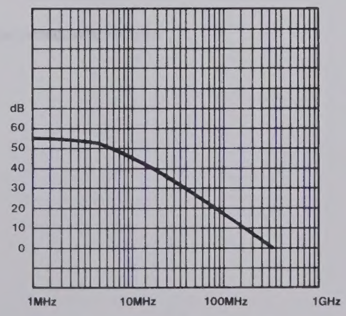
NOTE
Output of NE5539 20dB amplifier.
Z in = 75Ω's
Z out = 75Ω's

Figure 4

NE5539 OPEN LOOP PHASE



NE5539 OPEN LOOP GAIN



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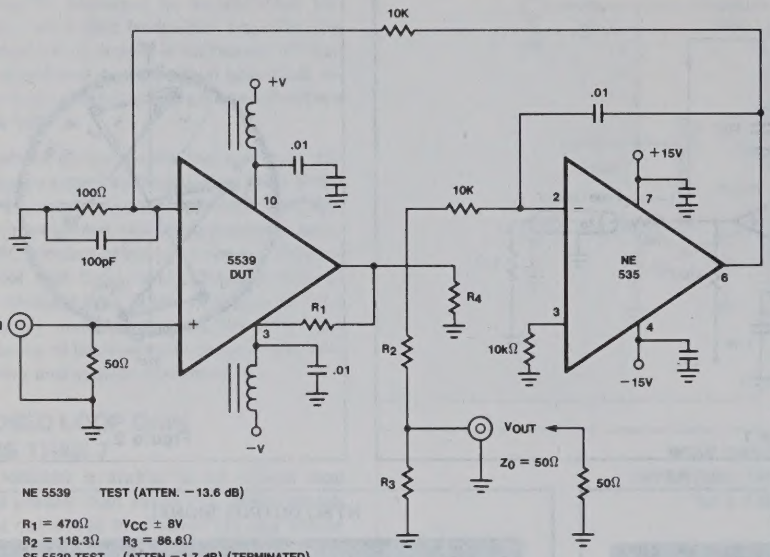
OPEN LOOP GAIN/PHASE TEST CIRCUIT


10K
+V
.01
.01
100Ω
100pF
10
−
5539
DUT
+
VIN
50Ω
R1
3
.01
−V
R4
10K
2
−
3
NE
535
6
7
+15V
4
−15V
10kΩ
R2
R3
VOUT
Z0 = 50Ω
50Ω

NE 5539 TEST (ATTEN. −13.6 dB)

$R_1 = 470\Omega$ $V_{CC} \pm 8V$
$R_2 = 118.3\Omega$ $R_3 = 86.6\Omega$
SE 5539 TEST (ATTEN −1.7 dB) (TERMINATED)
$R_1 = 390\Omega$ $V_{CC} \pm 6V$
$R_2 = 140\Omega$
$R_3 = 75\Omega$ $R_4 = 470\Omega$

GENERAL PURPOSE OPERATIONAL AMPLIFIER μA741/μA741C/SA741C

μA741/741C-N,FE
SA741C-N
μA741C-D

DESCRIPTION

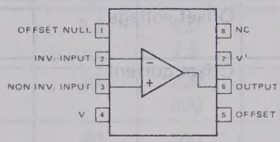
The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**

PIN CONFIGURATION

D,N,FE PACKAGE


OFFSET NULL 1
INV. INPUT 2
NON INV. INPUT 3
V⁻ 4
8 NC
7 V⁺
6 OUTPUT
5 OFFSET NULL
−
+

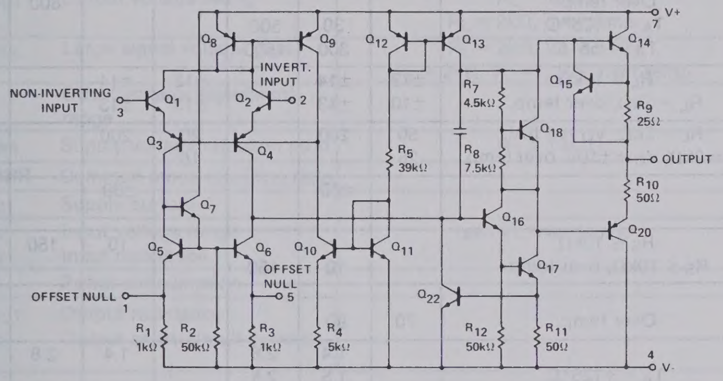
ORDER PART NO.

μA741N	μA741FE
μA741CN	μA741CFE

SA741CN
μA741CD

EQUIVALENT SCHEMATIC

μA741, μA741C, SA741C


V+ 7
Q8
Q9
Q12
Q13
Q14
INVERT. INPUT
NON-INVERTING INPUT 3
Q1
Q2
2
R7 4.5kΩ
Q15
R9 25Ω
Q3
Q4
Q18
R5 39kΩ
R8 7.5kΩ
OUTPUT
R10 50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
OFFSET NULL 5
Q17
OFFSET NULL 1
Q22
R1 1kΩ
R2 50kΩ
R3 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
4 V-

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA741C	±18	V
μA741	±22	V
Internal power dissipation		
N package	500	mW
FE package	1000	mW
Differential input voltage	±30	V
Input voltage[1]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μA741C	0 to +70	°C
SA741C	-40 to +85	°C
μA741	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTE
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

μA741/741C-N,FE
SA741C-N
μA741C-D

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.		1.0	6.0			7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		20	500				nA
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
		$R_L = 2k\Omega$, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	50	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, over temp.	25			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp.		10	150				μV/V
CMRR	Common mode rejection ratio								dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		$T_A = +125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		MΩ
P_d	Power consumption			50	85		50	85	mW
		$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		45	100				mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current			25			25		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

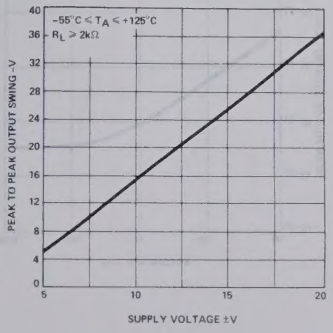
PARAMETER		TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10kΩ$ $R_S = 10kΩ$, over temp.		2.0	6.0 7.5	mV mV
I_{OS}	Offset current	 Over temp.		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 1500	nA nA
V_{OUT}	Output voltage swing	$R_L = 10kΩ$ $R_L = 2kΩ$, over temp.	±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2kΩ$, $V_O = ±10V$ $R_L = 2kΩ$, $V_O = ±10V$, over temp.	20 15	200		V/mV V/mV
	Offset voltage adjustment range			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10kΩ$		10	150	µV/V
CMRR	Common mode rejection ratio					dB
I_{CC}	Supply current			1.4	2.8	mA
V_{IN}	Input voltage range	(µA741, over temp.)	±12	±13		V
R_{IN}	Input resistance		0.3	2.0		MΩ
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$, unless otherwise specified.

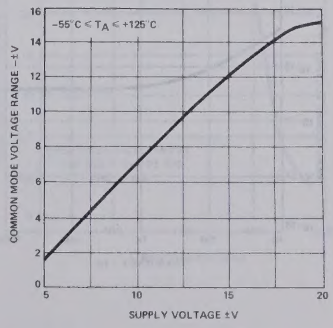
PARAMETER	TEST CONDITIONS	µA741, µA741C			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz				MΩ
Parallel input capacitance	Open loop, f = 20Hz		1.4		pF
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2kΩ$, $C_L \leq 100pf$				
Rise time			0.3		µs
Overshoot			5.0		%
Slew rate	$C \leq 100pf$, $R_L \geq 2k$, $V_{IN} = ±10V$		0.5		V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

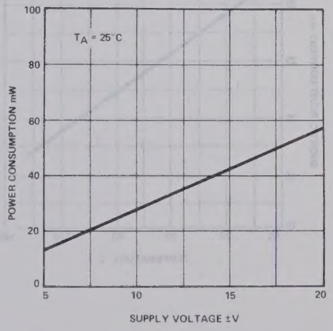
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

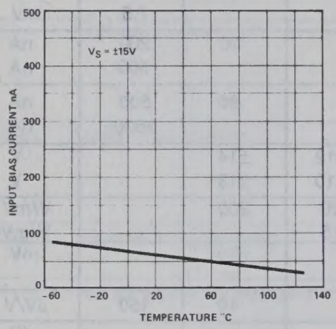


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

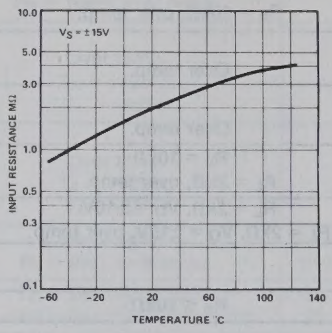


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

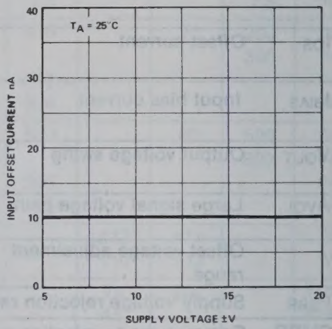
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



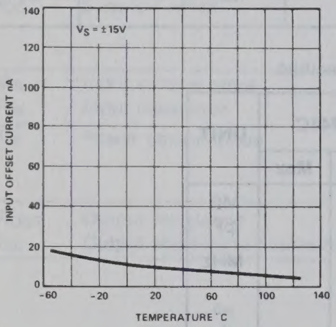
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



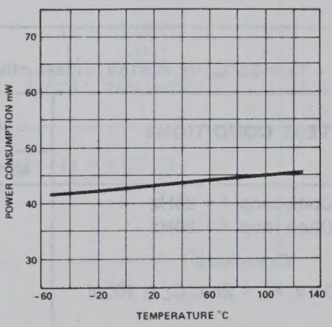
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



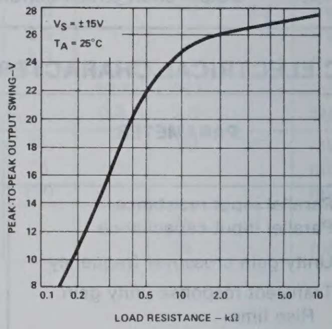
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



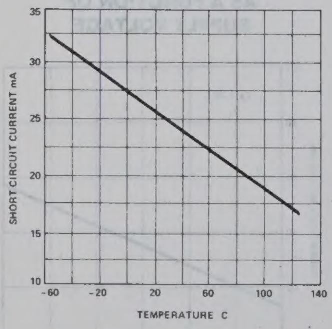
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



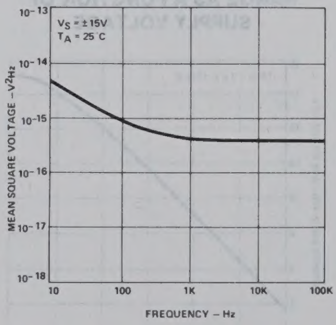
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



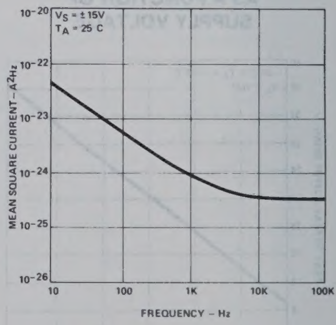
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

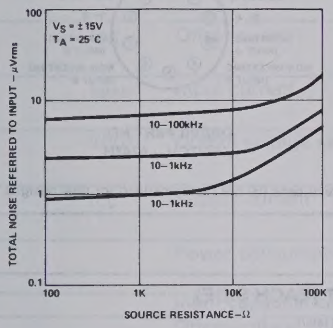


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

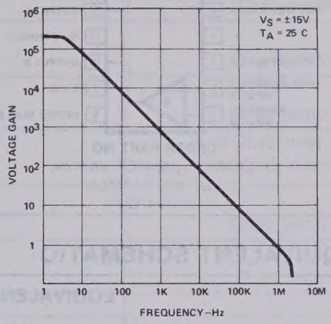


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

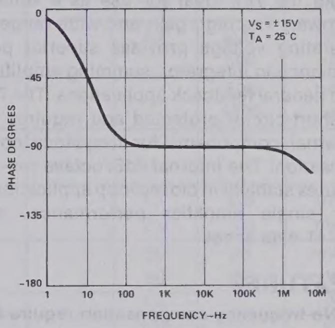
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



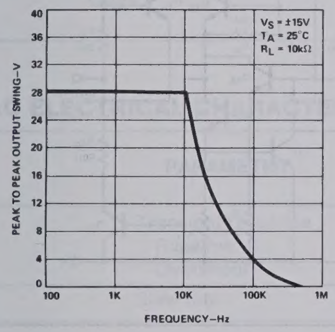
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



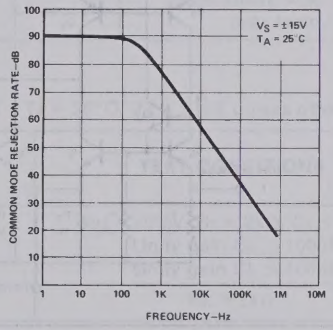
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



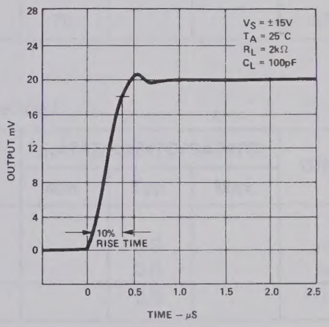
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



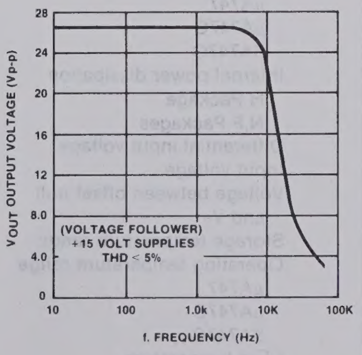
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



DUAL OPERATIONAL AMPLIFIER μA747/747C/SA747C

μA747/747C-F,H,N
SA747C-N
μA747C-D

DESCRIPTION

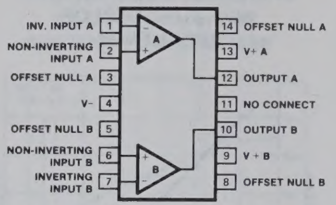
The 747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. High common mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

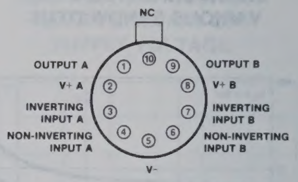
PIN CONFIGURATIONS

D,F,N PACKAGE


INV. INPUT A
1
NON-INVERTING INPUT A
2
OFFSET NULL A
3
V-
4
OFFSET NULL B
5
NON-INVERTING INPUT B
6
INVERTING INPUT B
7
A
B
14
OFFSET NULL A
13
V+ A
12
OUTPUT A
11
NO CONNECT
10
OUTPUT B
9
V + B
8
OFFSET NULL B

ORDER PART NO.
μA747CN, μA747CF, μA747N,
μA747F, SA747CN
μA747CD

H PACKAGE*

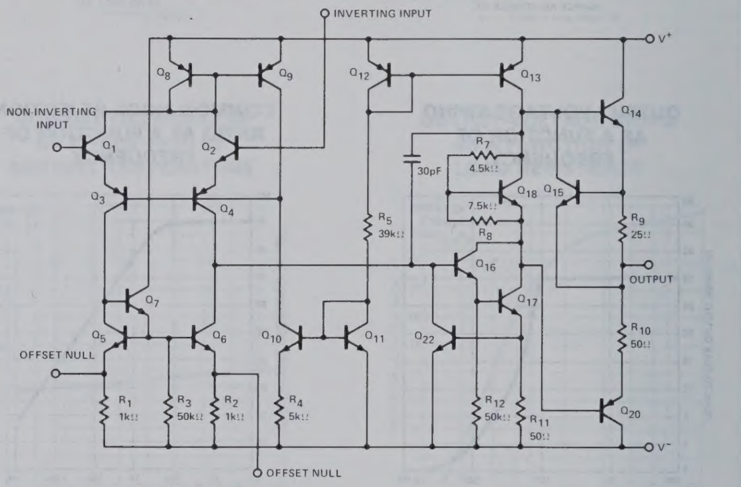

NC
OUTPUT A
V+ A
INVERTING INPUT A
NON-INVERTING INPUT A
V-
OUTPUT B
V+ B
INVERTING INPUT B
NON-INVERTING INPUT B
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩

ORDER PART NO.
μA747CH, μA747H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC

EQUIVALENT CIRCUIT (EACH SIDE)


INVERTING INPUT
V+
NON-INVERTING INPUT
OFFSET NULL
OFFSET NULL
OUTPUT
V-
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q20
Q22
30pF
R7 4.5kΩ
7.5kΩ R8
R5 39kΩ
R9 25Ω
R10 50Ω
R1 1kΩ
R3 50kΩ
R2 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA747	±22	V
μA747C	±18	V
SA747C	±18	V
Internal power dissipation		
H Package	500	mW
N,F Packages	670	mW
Differential input voltage	±30	V
Input voltage	±15	V
Voltage between offset null and V-	±0.5	V
Storage temperature range	-65 to +155	°C
Operating temperature range		
μA747	-55 to +125	°C
μA747C	0 to +70	°C
SA747C	-40 to +85	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short-circuit duration	indefinite	

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA747C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \le 10k\Omega$		2.0	6.0	mV
		$R_S \le 10k\Omega$, over temp		3.0	7.5	mV
I_{OS}	Offset current			20	200	nA
		Over temp			500	nA
I_{BIAS}	Input current				500	nA
		Over temp			1500	nA
V_{OUT}	Output voltage swing	$R_L \ge 2k\Omega$, over temp	±10	±13		V
		$R_L \ge 10k\Omega$, over temp	±12	±14		V
I_{CC}	Supply current			1.7	2.8	mA
		Over temp		2.0	3.3	mA
	Power consumption			50	85	mW
		Over temp		60	100	mW
	Input capacitance			1.4		pF
	Offset voltage adjustment range			±15		V
	Output resistance			75		Ω
	Channel separation			120		dB
P_{SRR}	Supply voltage rejection ratio	$R_S \le 10k\Omega$, over temp		30	150	μV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \ge 2k\Omega$ $V_{OUT} = \pm10V$	25,000			V/V
C_{MRR}		$R_S \le 10K\Omega$, V_{CM} ±12V over temp	70			dB

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	μA747/μA747C/SA747C			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = 20mV$, $R_1 = 2k\Omega$, $C_1 < 100pf$				
Risetime	Unity gain CL ≤ 100pf		0.3		μs
Overshoot	Unity gain CL ≤ 100pf		5.0		%
Slew rate	RL > 2kΩ		0.5		V/μs

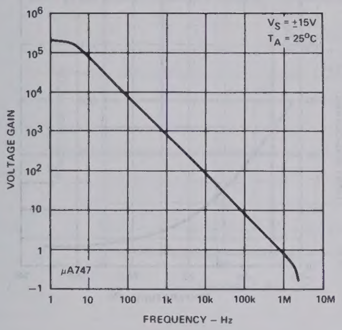
µA747/747C-F,H,N
SA747C-N
µA747C-D

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

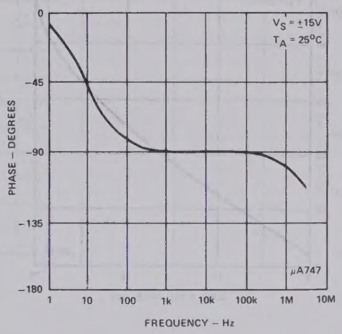
	PARAMETER	TEST CONDITIONS	µA747			µA747C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp		3.0	6.0		3.0	7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		85	500				nA
		Over temp					7.0	300	nA
I_{BIAS}	Input current			80	500		80	500	nA
		$T_A = 125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
		Over temp					30	800	nA
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp	±10	±13		±10	±13		V
		$R_L \geq 10k\Omega$, over temp	±12	±14		±12	±14		V
I_{CC}	Supply current each side			1.7	2.8		1.7	2.8	mA
		$T_A = 125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
		Over temp					2.0	3.3	mA
	Power consumption			50	85		50	85	mW
		$T_A = 125°C$		45	75				mW
		$T_A = -55°C$		60	100				mW
		Over temp					60	100	mW
	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		V
	Output resistance			75			75		Ω
	Channel separation			120			120		dB
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp		30	150		30	150	µV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \geq 2k\Omega$ $V_{OUT} = \pm10V$	50,000			25,000			V/V
		Over temp	25,000			15,000			V/V
C_{MRR}		$R_S \leq 10K\Omega$, V_{CM} ±12V over temp	70			70			dB

TYPICAL PERFORMANCE CHARACTERISTICS

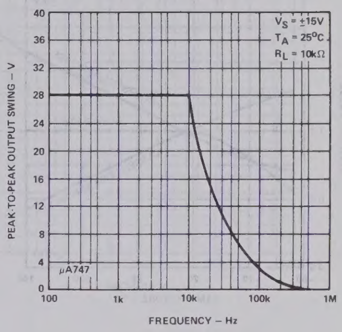
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



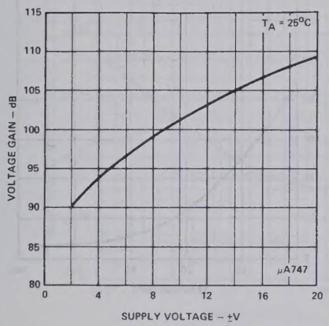
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



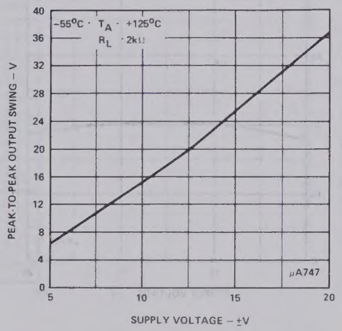
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



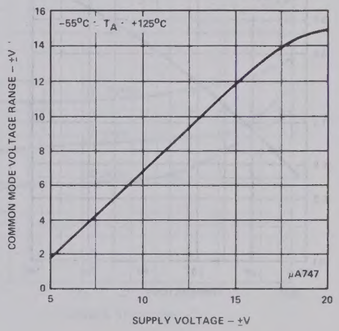
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



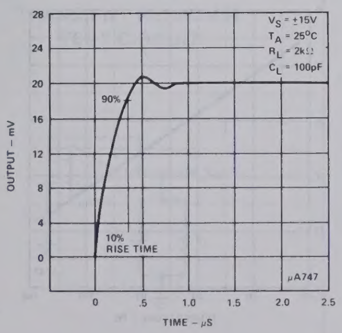
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



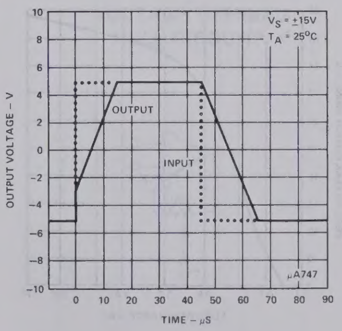
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



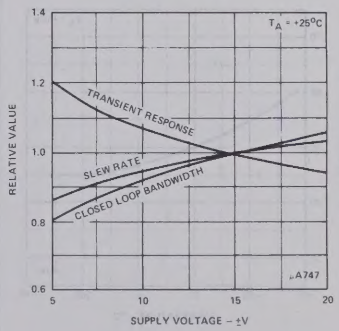
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



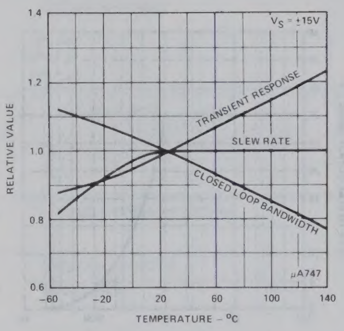
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



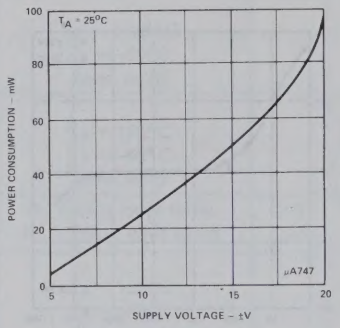
µA747/747C-F,H,N
SA747C-N
µA747C-D

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

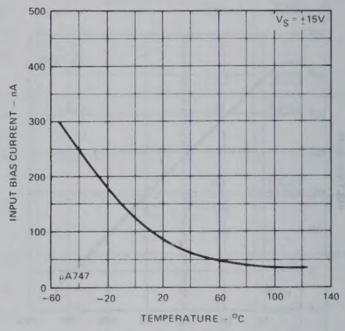
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



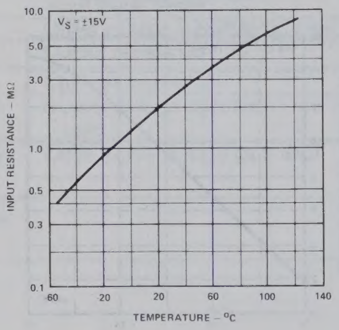
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



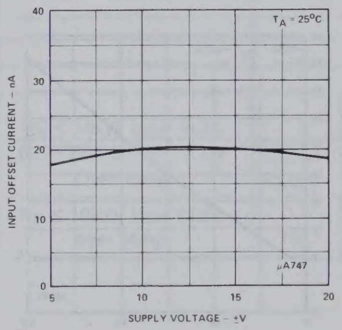
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



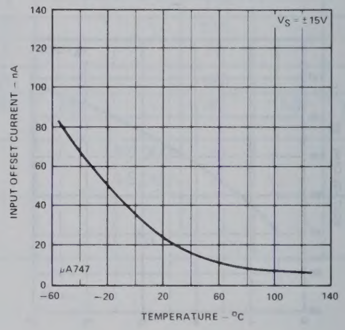
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



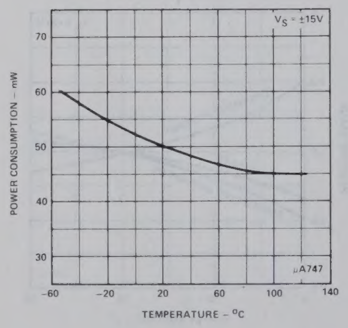
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



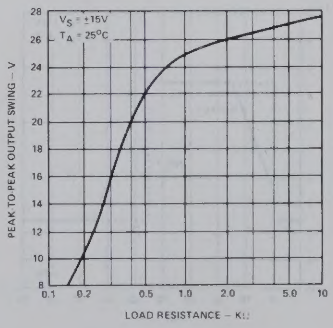
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



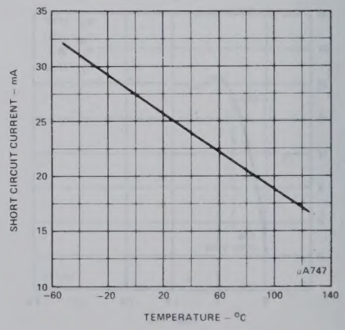
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

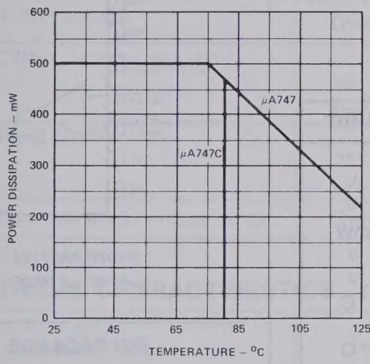


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

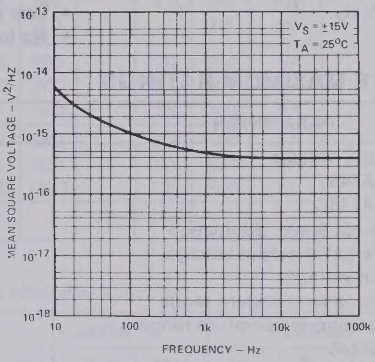


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

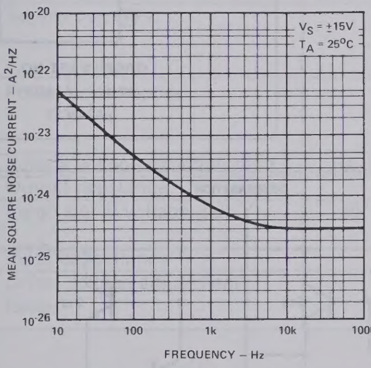
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



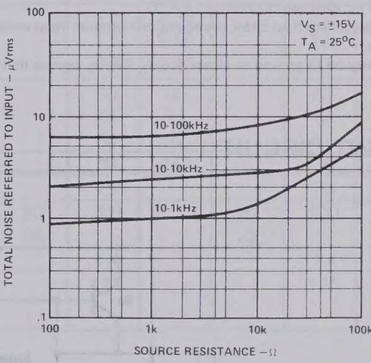
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

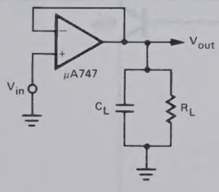


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

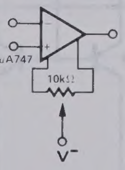


TEST CIRCUITS

TRANSIENT RESPONSE TEST CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



μA748/748C-F,N
μA748C-D

DESCRIPTION

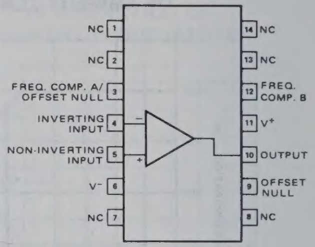
The 748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

FEATURES

- **Short circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**

PIN CONFIGURATIONS

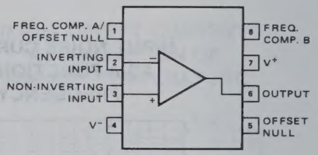
F PACKAGE


NC 1
NC 2
FREQ. COMP. A/ OFFSET NULL 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
V⁻ 6
NC 7
14 NC
13 NC
12 FREQ. COMP. B
11 V⁺
10 OUTPUT
9 OFFSET NULL
8 NC
−
+

ORDER PART NO.

μA748F, μA748CF,

D,N PACKAGE


FREQ. COMP. A/ OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V⁻ 4
8 FREQ. COMP. B
7 V⁺
6 OUTPUT
5 OFFSET NULL
−
+

ORDER PART NO.

μA748N, μA748CN
μA748CD

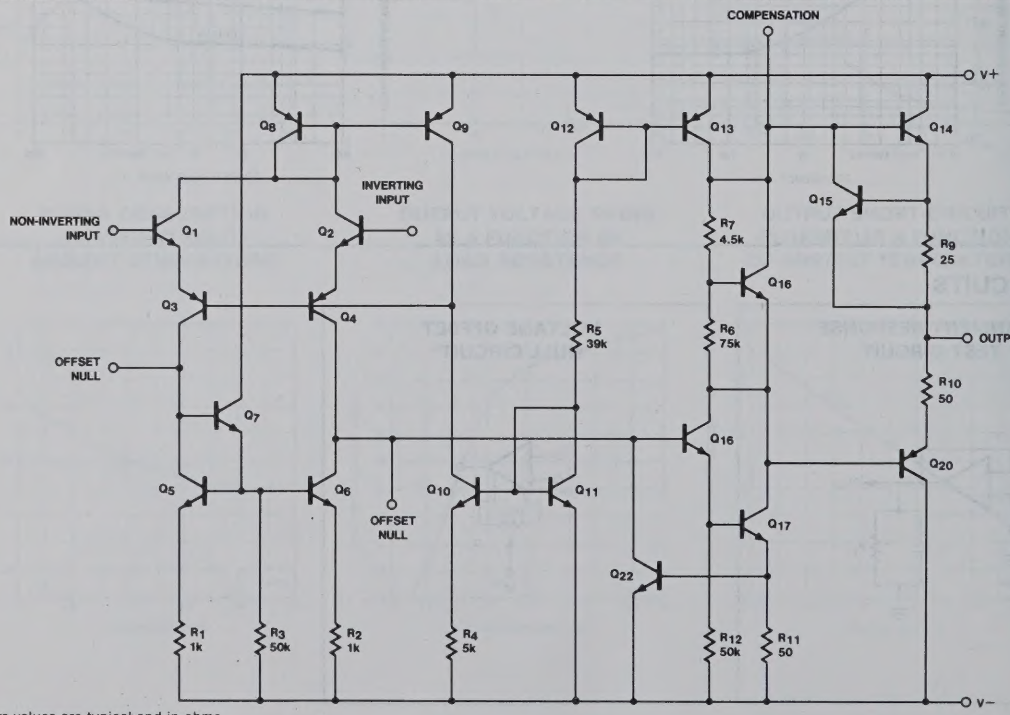
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA748	±22	V
μA748C	±18	V
Internal power dissipation[1]	500	mW
Differential output voltage	±30	V
Input voltage[2]	±15	V
Storage temperature range	-65 to +150	°C
Operating temperature range		
μA748	-55 to +125	°C
μA748C	0 to +70	°C
Lead temperature	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperatures to +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

EQUIVALENT CIRCUIT


COMPENSATION
V+
V−
OUTPUT
NON-INVERTING INPUT
INVERTING INPUT
OFFSET NULL
OFFSET NULL
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q16
Q17
Q20
Q22
R1 1k
R2 1k
R3 50k
R4 5k
R5 39k
R6 75k
R7 4.5k
R9 25
R10 50
R11 50
R12 50k

NOTE
All resistors values are typical and in ohms.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	μA748			μA748C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \le 10k\Omega$, $T_A = 25°C$		1.0	5.0		2.0	6.0	mV
		Over temperature			6.0			7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
		$25° \le T_A \le T_{max}$		7.0	200		9.0	300	nA
		$T_{min} \le T_A \le 25°C$		85	500		35	300	nA
I_{BIAS}	Input current			80	500		80	500	nA
		$25° \le T_A \le T_{max}$		30	500		40	800	nA
		$T_{min} \le T_A \le 25°C$		300	1500		130	800	nA
V_{CM}	Common mode voltage range	Over temperature	±12	±13		±12	±13		V

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

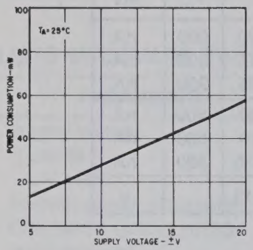
	PARAMETER	TEST CONDITIONS	μA748			μA748C			UNIT
			Min	Typ	Max	Min	Typ	Max	
C_{MRR}	Common mode rejection ratio	$R_S \le \pm10k\Omega$, over temperature	70	90		70	90		dB
R_{IN}	Input resistance		0.3	2.0		.30	2.0		MΩ
V_{OUT}	Output voltage swing	$R_L \ge 2k\Omega$, over temperature	±10	±13		±10	±13		V
		$R_L \ge 10k\Omega$, over temperature	±12	±14		±12	±14		V
I_{CC}	Supply current			1.7	2.83		1.7	2.83	mA
		$25° \le T_A \le T_{max}$		1.5	2.50		1.6	3.33	mA
		$T_{min} \le T_A \le 25°C$		2.0	3.33		1.8	3.33	mA
P_d	Power consumption	$T_A = 25°C$		50	85		50	85	mW
		$25° \le T_A \le T_{max}$		45	75		48	100	mW
		$T_{min} \le T_A \le 25°C$		60	100		54	100	mW
P_{SRR}	Supply voltage rejection ratio	$R_S \le 10k\Omega$, over temperature		30	150		30	150	μV/V
	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$R_L \ge 2k\Omega$ V_{OUT} ±10V ±15V	50	200		50	200		V/mV
		Over temperature	25			25			V/mV
	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		mV

AC ELECTRICAL CHARACTERISTICS

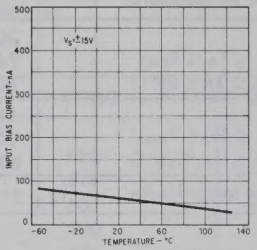
PARAMETER	TEST CONDITIONS	μA748			μA748C/SA748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response (unity gain)	$V_{IN} = 20mV$, $R_L = 2k\Omega$ $C_L \le 100pF$							
Rise time	$C_1 = 30pF$		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew rate	$R_L \ge 2k\Omega$ $C_1 = 30pF$		0.5			0.5		V/μs

TYPICAL CHARACTERISTIC CURVES

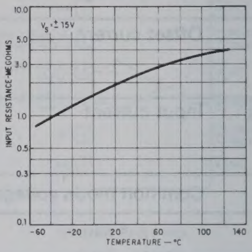
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



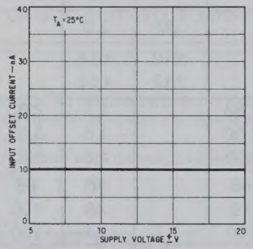
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



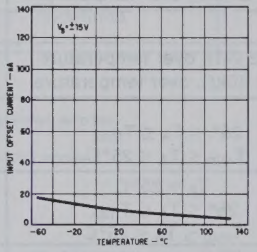
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



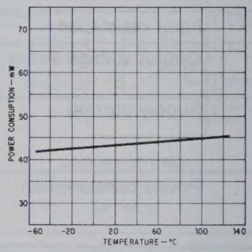
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



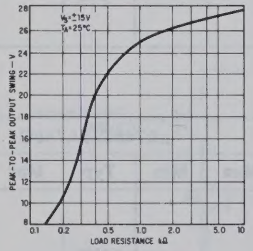
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



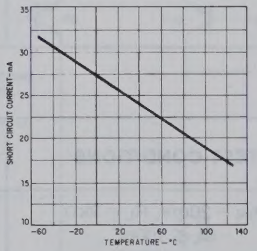
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



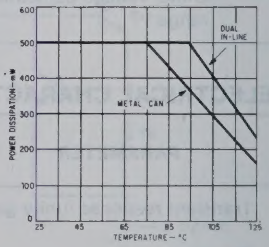
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



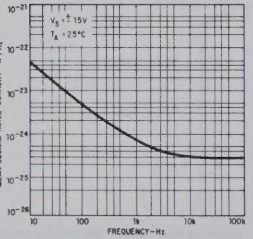
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



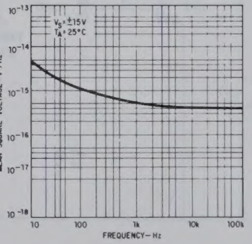
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



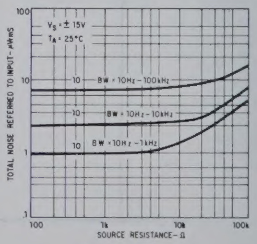
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

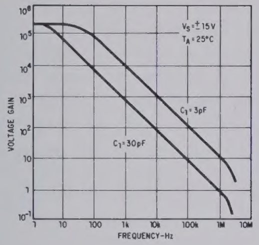


BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE

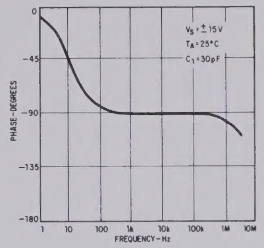


TYPICAL CHARACTERISTIC CURVES (Cont'd)

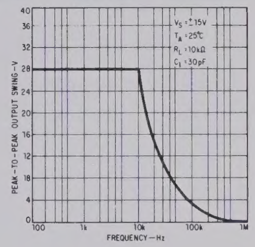
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



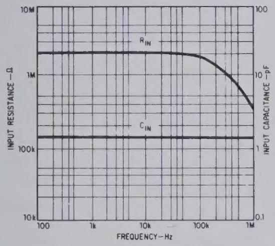
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



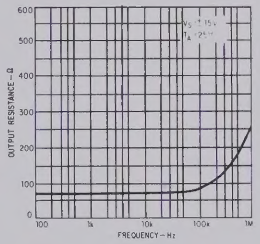
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



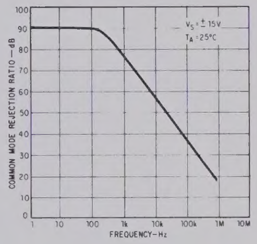
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



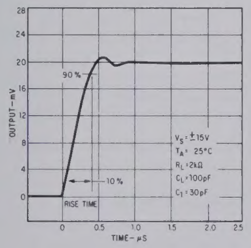
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



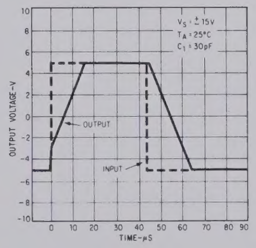
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



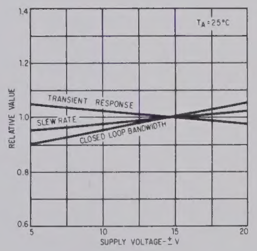
TRANSIENT RESPONSE



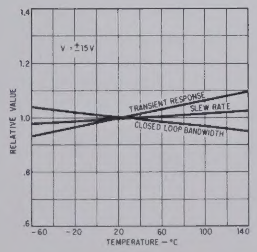
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



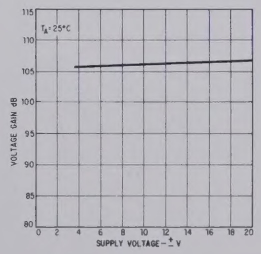
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



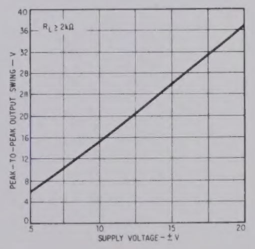
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



SECTION 2
VIDEO AMPLIFIERS

Section 2—VIDEO AMPLIFIERS

NE/SE592 Video Amplifier 137
μA733/733C Differential Video Amplifier 143

NE592-D,F,H,N
SE592-F,H

DESCRIPTION

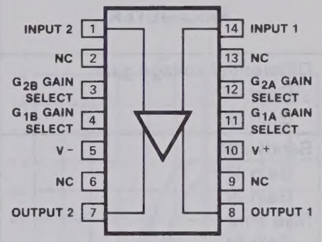
The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The 592 is a pin-for-pin replacement for the μA733.

FEATURES

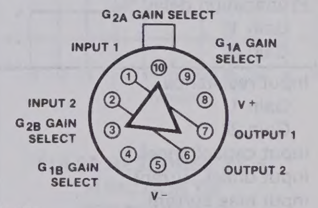
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

PIN CONFIGURATION

D,F,N PACKAGE

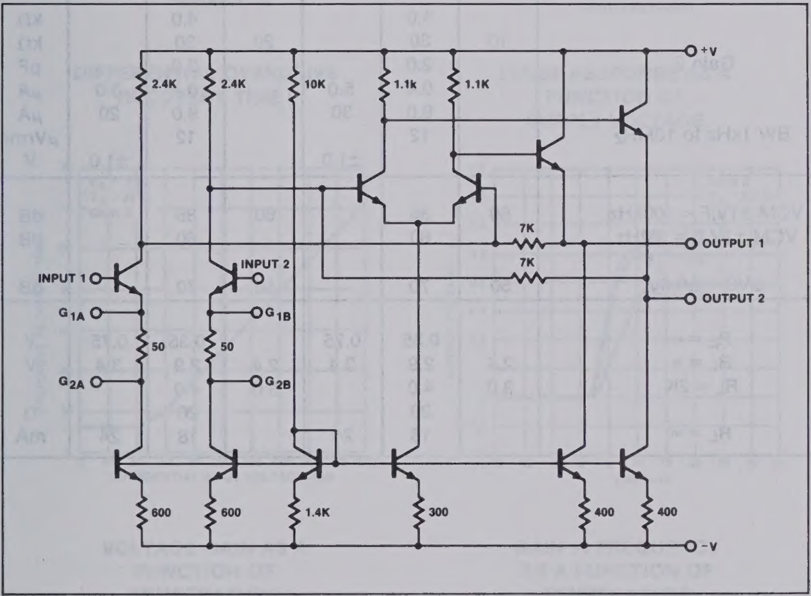

INPUT 2 1
NC 2
G_{2B} GAIN SELECT 3
G_{1B} GAIN SELECT 4
V − 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G_{2A} GAIN SELECT
11 G_{1A} GAIN SELECT
10 V +
9 NC
8 OUTPUT 1

H PACKAGE*


G_{2A} GAIN SELECT
INPUT 1
G_{1A} GAIN SELECT
INPUT 2
G_{2B} GAIN SELECT
G_{1B} GAIN SELECT
V +
OUTPUT 1
OUTPUT 2
V −
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩

NOTE
Pin 5 connected to case.
*Metal cans (H) not recommended for new designs.

EQUIVALENT CIRCUIT


+V
2.4K
2.4K
10K
1.1k
1.1K
7K
7K
OUTPUT 1
OUTPUT 2
INPUT 1
INPUT 2
G_{1A}
G_{1B}
50
50
G_{2A}
G_{2B}
600
600
1.4K
300
400
400
−V

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode Input voltage	±6	V
Output current	10	mA
Operating temperature range		
SE592K	-55 to +125	°C
NE592K	0 to +70	°C
Storage temperature range	-65 to +150	°C
Power dissipation	500	mW

NE592-D,F,H,N
SE592-F,H

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$ unless otherwise specified
Recommend operating supply voltages $V_S = \pm 6.0V$

PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1^1	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	250	400	600	300	400	500	V/V
Gain 2^2		80	100	120	90	100	110	V/V
Bandwidth								
Gain 1^1			40			40		MHz
Gain 2^2			90			90		MHz
Rise time								
Gain 1^1	$V_{OUT} = 1V$ p-p		10.5			10.5		ns
Gain 2^2			4.5	12		4.5	10	ns
Propagation delay								
Gain 1^1	$V_{OUT} = 1V$ p-p		7.5			7.5		ns
Gain 2^2			6.0	10		6.0	10	ns
Input resistance								
Gain 1^1			4.0			4.0		kΩ
Gain 2^2		10	30		20	30		kΩ
Input capacitance^2	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW 1kHz to 10MHz		12			12		μVrms
Input voltage range				±1.0			±1.0	V
Common mode rejection ratio								
Gain 2	VCM ±1V,F < 100kHz	60	86		60	86		dB
Gain 2	VCM ±1V,F = 5MHz		60			60		dB
Supply voltage rejection ratio								
Gain 2	ΔVS = ±0.5V	50	70		50	70		dB
Output offset voltage								
Gain 2^2	$R_L = \infty$		0.35	0.75		0.35	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Out put voltage swing differential	$R_L = 2K$	3.0	4.0		3.0	4.0		
Output resistance			20			20		Ω
Power supply current	$R_L = \infty$		18	24		18	24	mA

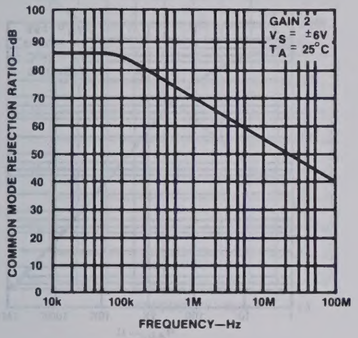
NOTES

1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

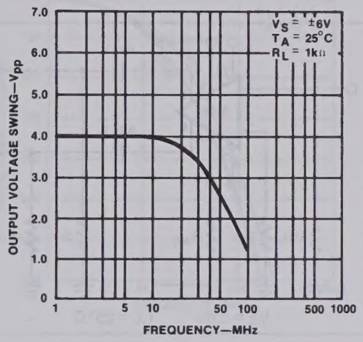
NE592-D,F,H,N
SE592-F,H

TYPICAL PERFORMANCE CHARACTERISTICS

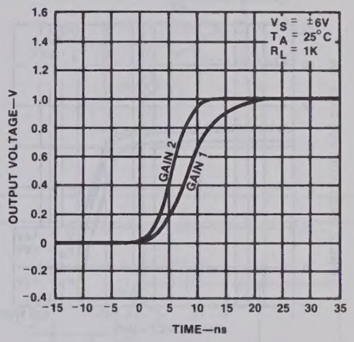
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



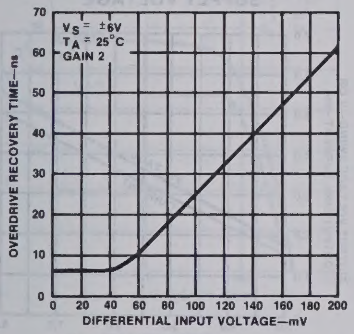
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



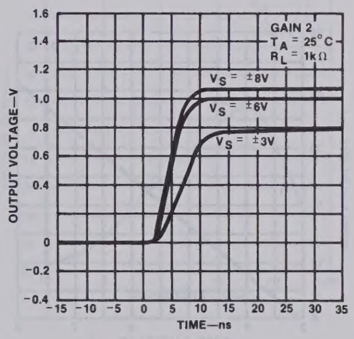
PULSE RESPONSE



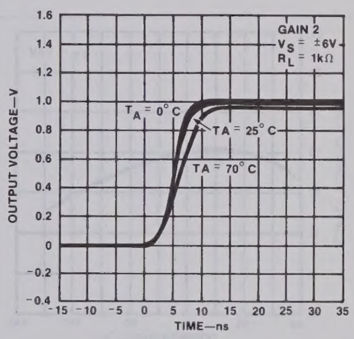
DIFFERENTIAL OVERDRIVE RECOVERY TIME



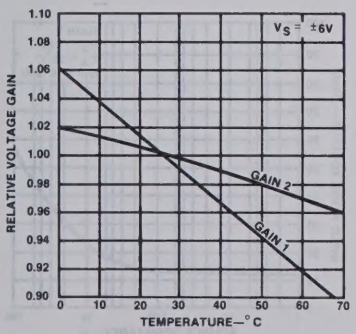
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



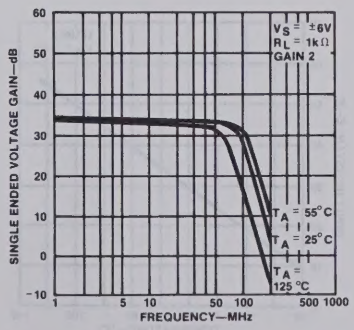
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



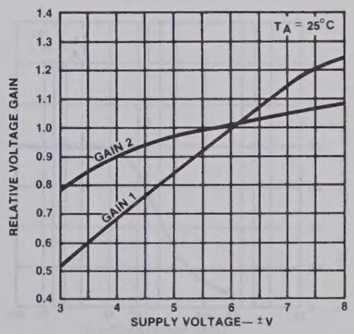
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE

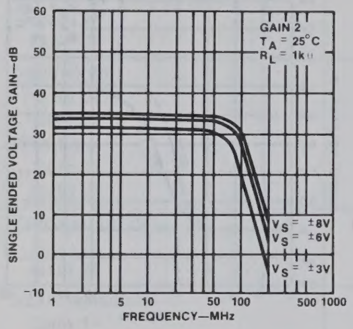


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

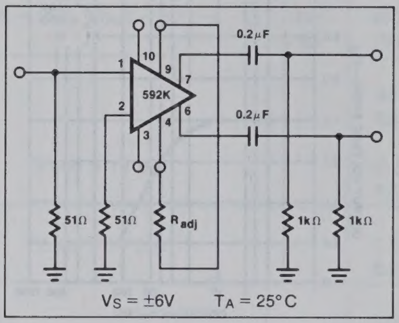


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

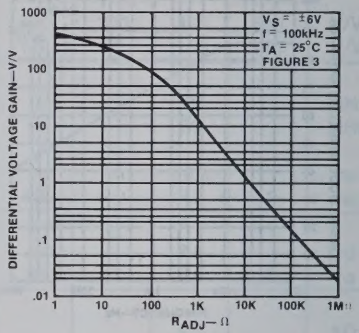
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



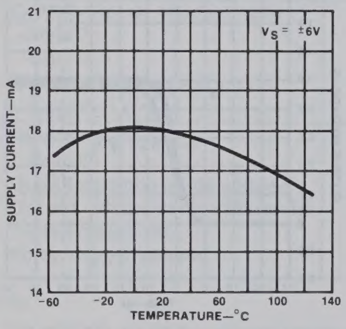
VOLTAGE GAIN ADJUST CIRCUIT



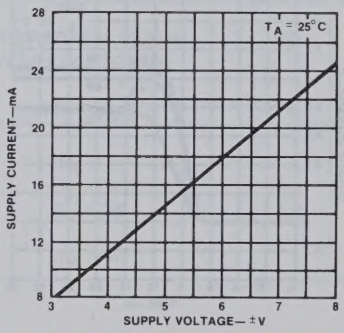
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



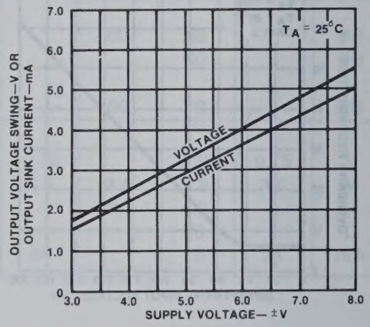
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



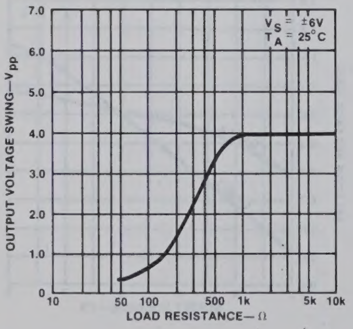
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



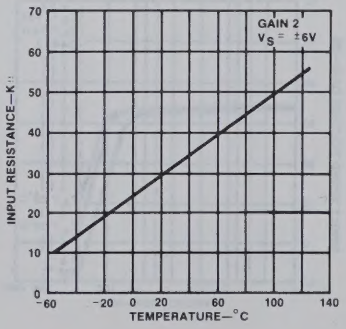
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



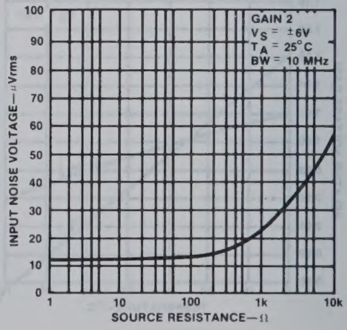
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

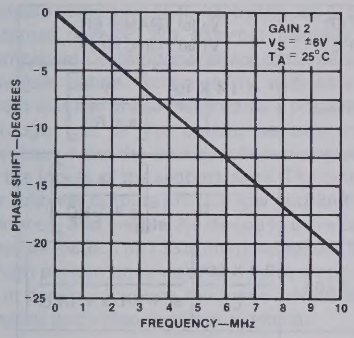


INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

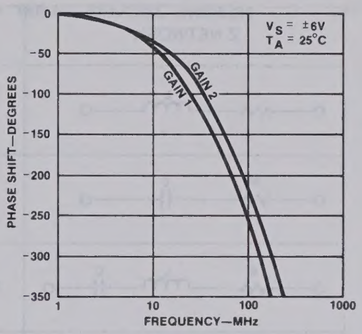


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

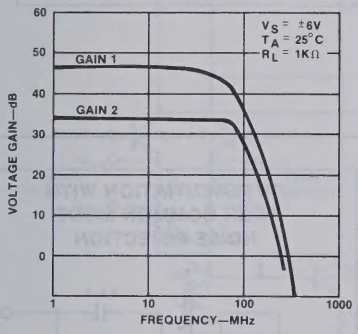
PHASE SHIFT AS A FUNCTION OF FREQUENCY



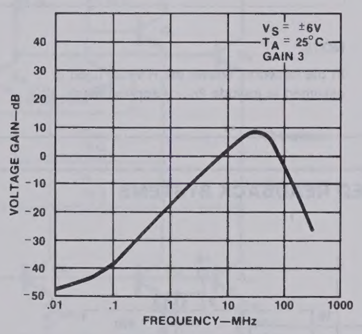
PHASE SHIFT AS A FUNCTION OF FREQUENCY



VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

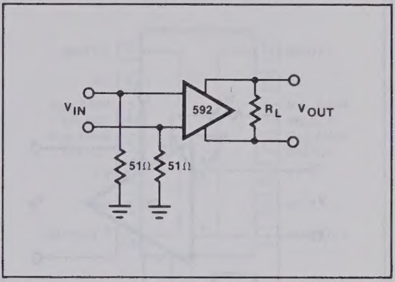


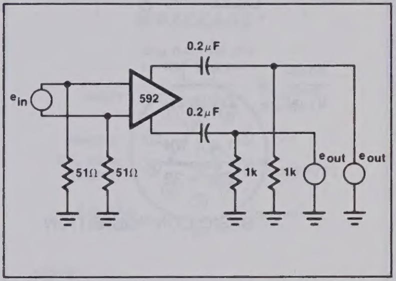
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



TEST CIRCUITS

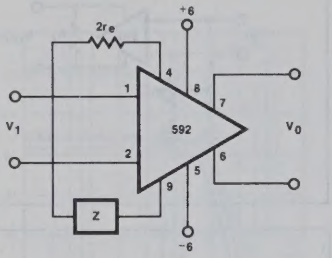
T_A = 25°C unless otherwise specified


V_{IN}
592
R_L
V_{OUT}
51Ω
51Ω


0.2µF
e_{in}
592
0.2µF
51Ω
51Ω
1k
1k
e_{out}
e_{out}

TYPICAL APPLICATIONS

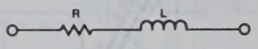
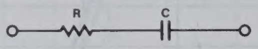
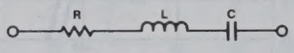
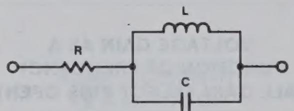
FILTER NETWORKS


+6
2re
4
8
1
7
V1
592
V0
2
6
5
9
Z
-6

$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

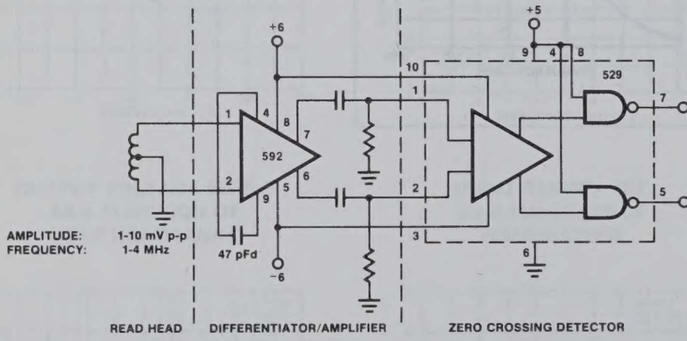
$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

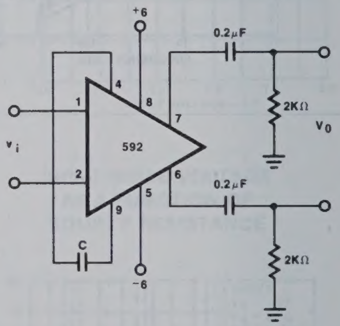
Z NETWORK	FILTER TYPE	$\frac{V_0(s)}{V_1(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS


+6
+5
9
4
8
10
529
1
7
Q
592
8
7
4
1
2
6
5
9
2
3
5
Q̄
6
AMPLITUDE: 1-10 mV p-p
FREQUENCY: 1-4 MHz
47 pFd
-6
READ HEAD
DIFFERENTIATOR/AMPLIFIER
ZERO CROSSING DETECTOR

DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION


+6
0.2μF
4
8
1
7
2KΩ
vi
592
V0
2
6
5
0.2μF
9
C
-6
2KΩ

FOR FREQUENCY $F_1 << 1/2\,\pi\,(32)\,C$
$V_0 \cong 1.4 \times 10^4 C \frac{dV_i}{dT}$

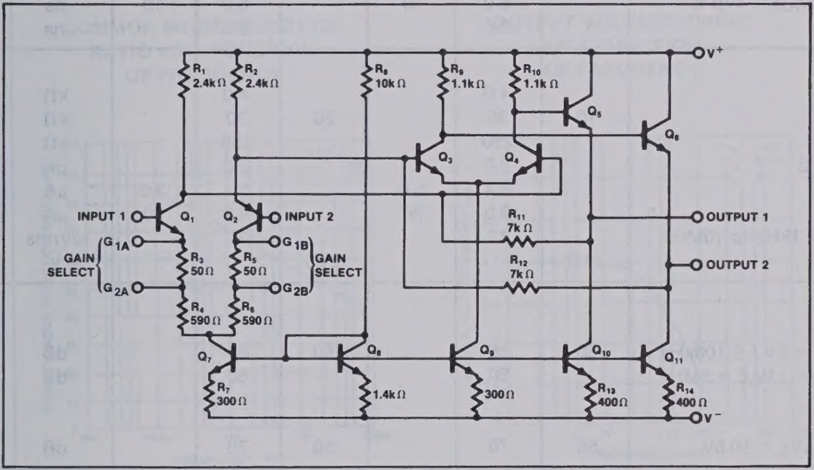
DIFFERENTIAL VIDEO AMPLIFIER μA733/733C

μA733/733C-F,H,N

DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

CIRCUIT SCHEMATIC



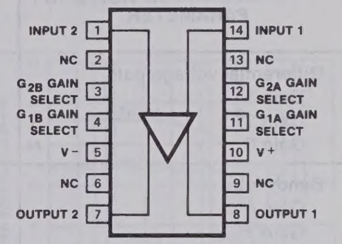
R1 2.4kΩ
R2 2.4kΩ
R8 10kΩ
R9 1.1kΩ
R10 1.1kΩ
V+
Q5
Q6
Q3
Q4
INPUT 1
Q1
Q2
INPUT 2
R11 7kΩ
R12 7kΩ
OUTPUT 1
OUTPUT 2
G1A
GAIN SELECT
G2A
R3 50Ω
R5 50Ω
G1B
G2B
GAIN SELECT
R4 590Ω
R6 590Ω
Q7
Q8
Q9
Q10
Q11
R7 300Ω
1.4kΩ
300Ω
R13 400Ω
R14 400Ω
V−

FEATURES

- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10,100 and 400**
- **No frequency compensation required**
- **Mil std 883A,B,C available**

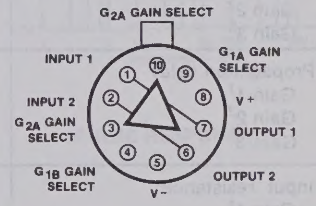
PIN CONFIGURATION

F,N PACKAGE



INPUT 2 1
NC 2
G2B GAIN SELECT 3
G1B GAIN SELECT 4
V− 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G2A GAIN SELECT
11 G1A GAIN SELECT
10 V+
9 NC
8 OUTPUT 1

H PACKAGE*



G2A GAIN SELECT
INPUT 1
G1A GAIN SELECT
INPUT 2
V+
G2A GAIN SELECT
OUTPUT 1
G1B GAIN SELECT
OUTPUT 2
V−
1
2
3
4
5
6
7
8
9
10

NOTE

Pin 5 connected to case.

*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Differential input Voltage	±5	V
Common mode input Voltage	±6	V
Vcc	±8	V
Ouput current	10	mA
Junction temperature	+150	°C
Storage temperature range	-65 to +150	°C
Operation temperature range		
μA733C	0 to +75	°C
μA733	-55 to +125	°C
P_D Power dissipation		
K package	500	mW
N, F package	670	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_S = \pm V$, VCM = 0 unless otherwise specified.
Recommended operating supply voltages $V_S = \pm 6.0V$.

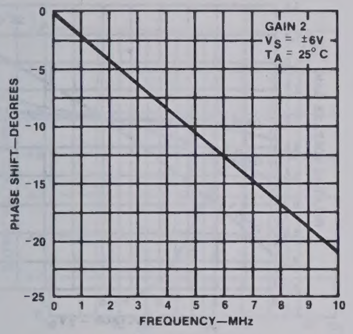
PARAMETER	TEST CONDITIONS	μA733C Min	μA733C Typ	μA733C Max	μA733 Min	μA733 Typ	μA733 Max	UNITS
Differential voltage gain								
Gain 1^1		250	400	600	300	400	500	V/V
Gain 2^2	$R_I = 2k\Omega$, $V_{OUT} = 3Vp\text{-}p$	80	100	120	90	100	110	V/V
Gain 3^3		8.0	10	12	9.0	10	11	V/V
Bandwidth								
Gain 1^1			40			40		MHz
Gain 2^2			90			90		MHz
Gain 3^3			120			120		MHz
Rise time								
Gain 1^1			10.5			10.5		ns
Gain 2^2	$V_{OUT} = 1Vp\text{-}p$		4.5	12		4.5	10	ns
Gain 3^3			2.5			2.5		ns
Propagation delay								
Gain 1^1			7.5			7.5		ns
Gain 2^2	$V_{OUT} = 1Vp\text{-}p$		6.0	10		6.0	10	ns
Gain 3^3			3.6			3.6		ns
Input resistance								
Gain 1^1			4.0			4.0		kΩ
Gain 2^2		10	30		20	30		kΩ
Gain 3^3			250			250		kΩ
Input capacitance^2	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW = 1kHz to 10MHz		12			12		μVrms
Input voltage range		±1.0			±1.0			V
Common mode								
Rejection ratio								
Gain 2	VCM = ±V, f ≤ 100kHz	60	86		60	86		dB
Gain 2	VCM = ±1V, F = 5MHz		60			60		dB
Supply voltage								
Rejection ratio								
Gain 2	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
Output offset voltage								
Gain 1^1	$R_L = \infty$		0.6	1.5		0.6	1.5	V
Gain 2 and $3^{2,3}$			0.35	1.5		0.35	1.0	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing, differential	$R_L = 2k$	3.0	4.0		3.0	4.0		
Output sink current		2.5	3.6		2.5	3.6		mA
Output resistance			20			20		Ω
Power supply current	$R_L \pm \infty$		18	24		18	24	mA

NOTES

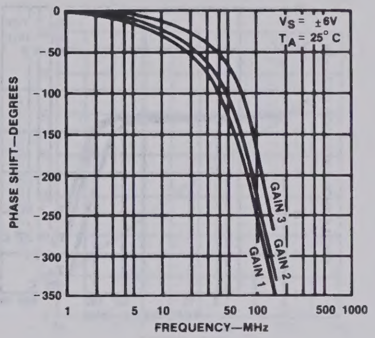
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

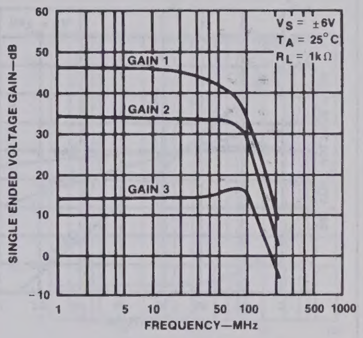
PHASE SHIFT AS A FUNCTION OF FREQUENCY



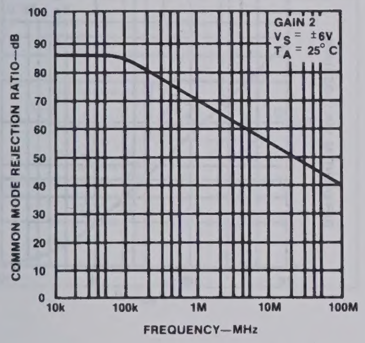
PHASE SHIFT AS A FUNCTION OF FREQUENCY



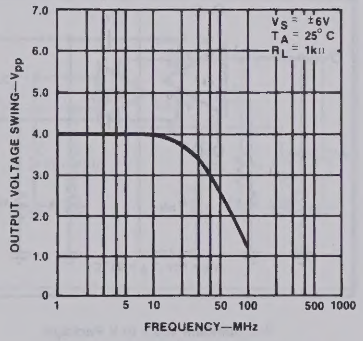
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



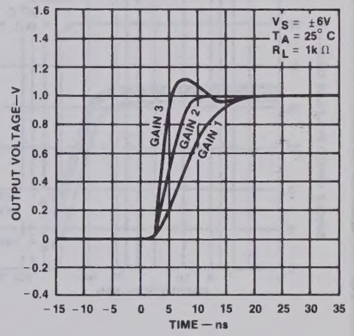
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



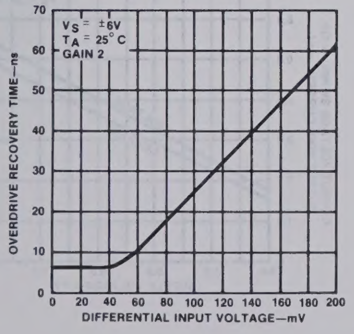
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



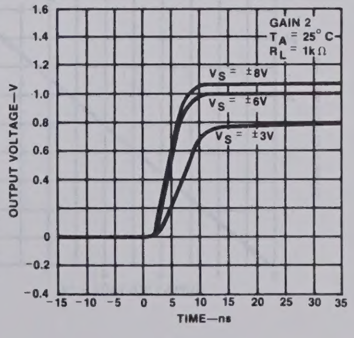
PULSE RESPONSE



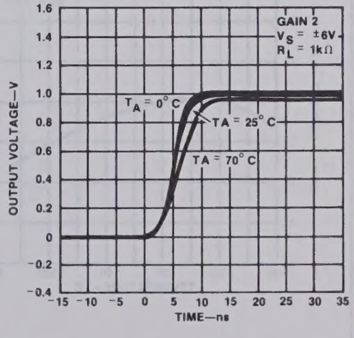
DIFFERENTIAL OVERDRIVE RECOVERY TIME



PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE

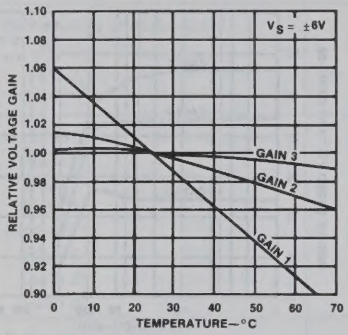


PULSE RESPONSE AS A FUNCTION OF TEMPERATURE

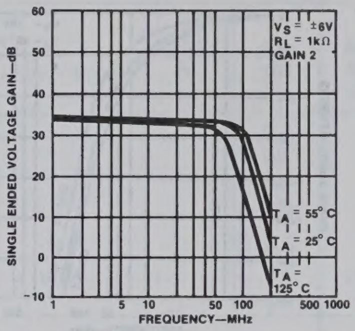


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

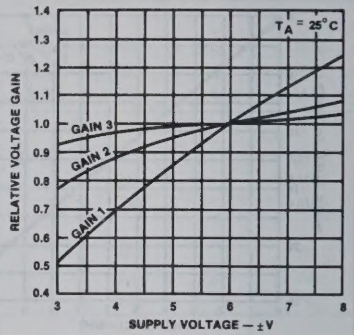
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



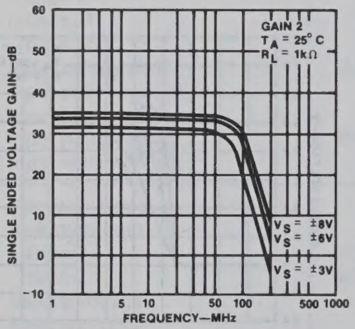
GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE



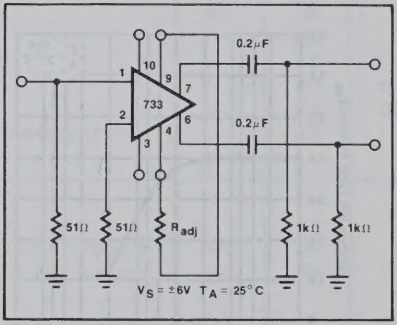
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

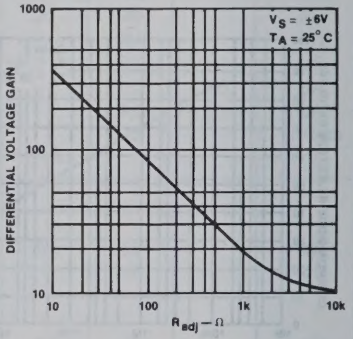


VOLTAGE GAIN ADJUST CIRCUIT

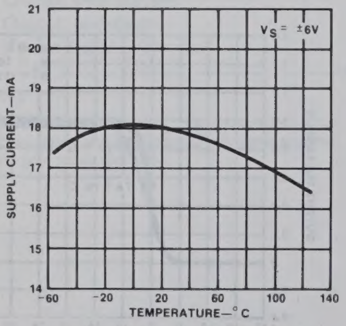


(Pin numbers apply to K Package)

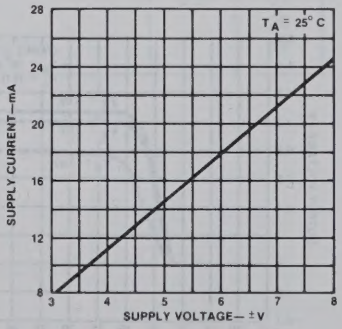
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



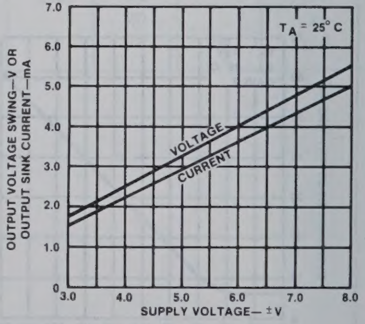
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

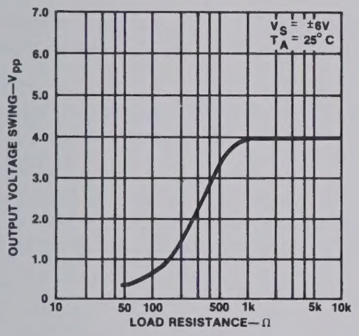


OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE

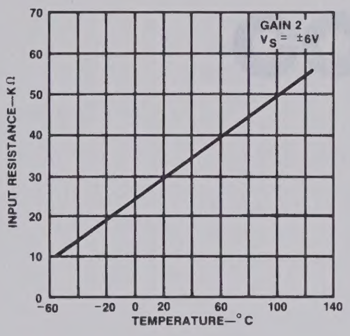


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

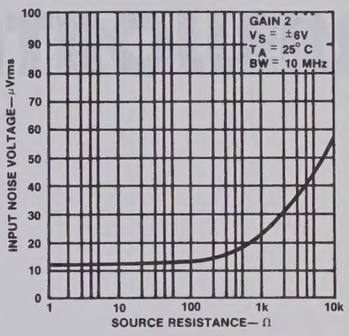
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

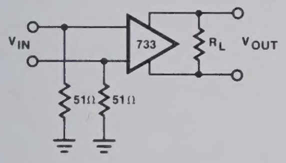


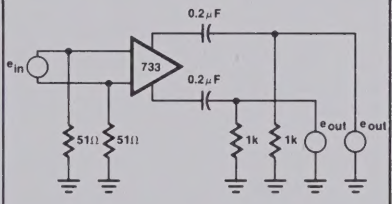
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



TEST CIRCUITS

$T_A = 25°C$ unless otherwise specified.


V_IN
733
R_L
V_OUT
51Ω
51Ω


0.2μF
e_in
733
0.2μF
51Ω
51Ω
1k
1k
e_out
e_out

SECTION 3
POWER CONTROLLERS

Section 3—POWER CONTROLLERS

NE/SE5553/5554	Dual Polarity Regulator	153
NE/SE5560	Switched-Mode Power Supply Control Circuit	157
SG1524/2524/3524	Regulating Pulse Width Modulator	161
μA723/723C/SA723C	Precision Voltage Regulator	169

VOLTAGE REGULATOR DEFINITIONS

T_A
Ambient temperature range. Range of the surrounding environment of the operating device.

T_J
Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}
Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}
Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)
Supply Voltage. The range of power supply voltage over which the device will operate safely.

Line Regulation

Sometimes referred to as "static regulation". This term refers to the changes in the output as the input is varied slowly from its rated minimum value to its rated maximum value (from 105 VAC_{RMS} to 125 VAC_{RMS}). Measured in mv/V.

Load Regulation

Sometimes referred to as "dynamic regulation". This term refers to the changes in the output when load conditions are suddenly changed (from no load to full load). Measured in mv/V.

Thermal Regulation

Referred to as changes due to ambient variations or thermal drift. Also referred to as temperature coefficient, measured in ppm/°C or mv/°C.

Transient Response

The ability of a regulator to respond to rapid changes in line variations, load variations, or intermittent transient input conditions. (Transient Response is often referred to as "recovery time"). Measured in milliseconds (ms).

Voltage Limiting

The ability of the regulator to "shut down" in the event that the internal reference sources fail to function properly. Measured in Volts.

Current Limiting

The ability of the amplified segment to limit the output current of the device when safe operating limits are exceeded. Measured in amperes (pre-determined).

Thermal Shutdown

The ability of the regulator to shut itself down when the maximum die temperature is exceeded. Measured in degrees Celsius (C).

Power Dissipation

The ability of the regulator to tolerate excessively high levels of input power while maintaining its operation within the safe operating area of its active devices. Measured in watts.

Efficiency

Regarding a regulator, the ratio of the total power input to the usable power output. Expressed as a percentage. (For example, if a regulator has a 50 watt input and a 40 watt output, its efficiency is 80 percent).

EMI/RFI

("Electromagnetic Interference/Radio Frequency Interference") regarding regulators, magnetic field disturbance and radio frequency interference signals generated especially by SMPS devices. Measurement is generally unspecified.

Safe Operating Area Restriction (SOAR)

Limits the output current of the amplifier to maintain safe (no thermal runaway) operating conditions. (Accomplished through internal sensor amplifiers).

NOTE
Refer to Section 4 of Analog Applications Manual for an in-depth explanation of Voltage Regulators

DUAL TRACKING VOLTAGE REGULATOR

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
NATIONAL MOTOROLA RAYTHEON		Line Regulator	1 %	SE / NE 555X	Yes		I_{OUT} 400mA
LM125, −6, −7	0.1 %	Line Regulator	0.25 %				
Raytheon 4194	±.05 to ±40	V_{OUT}	± 5 to ±20 Volts	SE / NE 5553 / 4	Yes		
Motorola 1568	100 mA	I_{OUT}	±400 mA	SE / NE 5553 / 4			
		Package Power Dissipation	8 Watts	SE NE } 5553 / 4 Series in SIL-9 package			

NE/SE5553/5554-F,H,N,U

DESCRIPTION

The NE/SE5553,4 are dual polarity tracking regulators designed to produce balanced or unbalanced output voltages from 5 to 20 volts with up to 300 mA output current. Similar in specifications to the 78MXX and 79MXX fixed regulators, the 5553/4 series can be continuously adjusted, balanced or unbalanced. The fixed voltage on the 5553 is ±12V, and on the 5554 is ±15V. Employing current limiting and thermal shutdown protection, these dual polarity regulators are ideal for local on-card regulation.

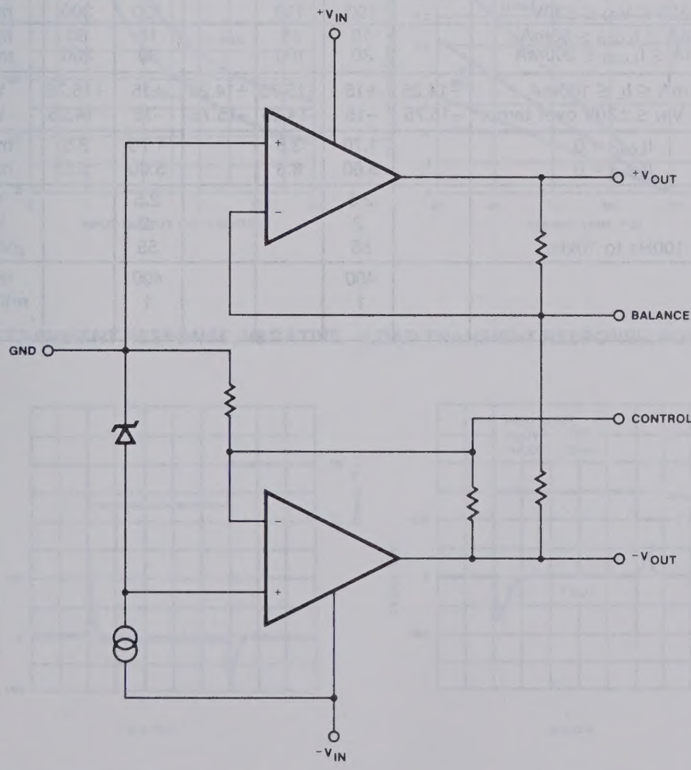
FEATURES

- **Output current to 300mA**
- **Internally current limited**
- **Thermal overload protected**
- **Input voltage to ±32V**
- **Output balance 1% typ.**
- **External balance control**
- **Continuously adjustable from 5 to 20 volts, balanced or unbalanced**
- **No external components required**
- **Short circuit current 400mA**
- **Maximum power capability can be achieved with proper heat sinking**

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{IN}	Input voltage	±32	V
T_{SG}	Storage temperature	-65 to +150	°C
T_J	Operating junction temperature		
	NE5553/5554	0 to +125	°C
	SE5553/5554	-55 to +150	°C
	Lead temperature 10 sec.	300	°C

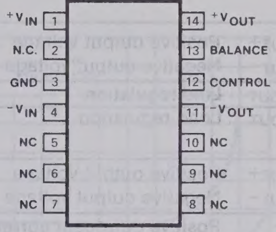
BLOCK DIAGRAM



$^+V_{IN}$
+
−
$^+V_{OUT}$
BALANCE
GND
CONTROL
−
+
$^-V_{OUT}$
$^-V_{IN}$

PIN CONFIGURATIONS

F,N PACKAGE

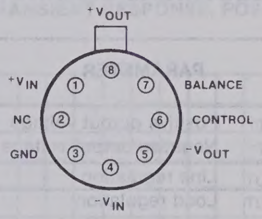


$^+V_{IN}$ 1
N.C. 2
GND 3
$^-V_{IN}$ 4
NC 5
NC 6
NC 7
14 $^+V_{OUT}$
13 BALANCE
12 CONTROL
11 $^-V_{OUT}$
10 NC
9 NC
8 NC

ORDER PART NO.

VOLTAGE	PART NO.
±12V	NE/SE5553F,N
±15V	NE/SE5554F,N

H PACKAGE*



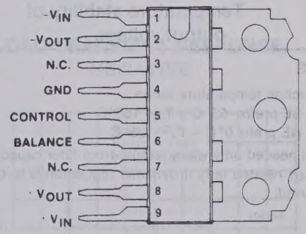
$^+V_{OUT}$
$^+V_{IN}$ ①
⑧
⑦ BALANCE
NC ②
⑥ CONTROL
GND ③
⑤ $^-V_{OUT}$
④
$^-V_{IN}$

ORDER PART NO.

VOLTAGE	PART NO.
±12V	NE/SE5553H
±15V	NE/SE5554H

*Metal cans (H) not recommended for new designs

U PACKAGE



$^-V_{IN}$ 1
$^-V_{OUT}$ 2
N.C. 3
GND 4
CONTROL 5
BALANCE 6
N.C. 7
$^+V_{OUT}$ 8
$^+V_{IN}$ 9

ORDER PART NO.

VOLTAGE	PART NO.
±12V	NE/SE5553U
±15V	NE/SE5554U

THERMAL RESISTANCE

H Package: Θ_{JC} = 20°C/W Θ_{JA} = 150°C/W
N Package: Θ_{JC} = 33°C/W Θ_{JA} = 95°C/W
U Package: Θ_{JC} = 30°C/W Θ_{JA} = 62°C/W
F Package: Θ_{JC} = 30°C/W Θ_{JA} = 110°C/W

DC ELECTRICAL CHARACTERISTICS $V_{IN} = \pm 20V$, $I_L = 100mA$, $T_J = 25°C$, $C_{IN} = C_{OUT} = 0.1\mu F$ unless otherwise specified.[2]

PARAMETER		TEST CONDITIONS	SE5553			NE5553			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{OUT}+$	Positive output voltage		+11.5	+12	+12.5	+11.5	+12	+12.5	
$V_{OUT}-$	Negative output voltage		-12.5	-12	-11.5	-12.5	-12	-11.5	V
ΔV_{OUT}	Line regulation	$\pm 20 \le V_{IN} \le \pm 30V$		100	150		100	300	mV
ΔV_{OUT}	Load regulation	$1mA \le I_{Load} \le 50mA$		10	25		10	50	mV
		$1mA \le I_{Load} \le 200mA$		30	100		30	200	mV
$V_{OUT}+$	Positive output voltage	$1mA \le I_L \le 100mA$	+11.4	+12	+12.6	+11.4	+12	+12.6	V
$V_{OUT}-$	Negative output voltage	$\pm 20V \le V_{IN} \le \pm 30V$ over temp.[1]	-12.6	-12	-11.4	-12.6	-12	-11.4	V
I_Q+	Positive quiescent current	$I_{Load} = 0$		1.70	3.5		1.70	3.5	mA
I_Q-	Negative quiescent current	$I_{Load} = 0$		5.60	8.5		5.60	8.5	mA
	Input/output differential voltage			2.5			2.5		V
V_{BAL}	Output voltage balance			.2			.2		V
	Output noise voltage	100Hz to 10kHz		55			55		μVrms
I_{Peak}	Peak output current			400			400		mA
	Temperature stability of output voltage			1			1		mV/°C

DC ELECTRICAL CHARACTERISTICS $V_{IN} = \pm 20V$, $I_L = 100mA$, $T_J = 25°C$, $C_{IN} = C_{OUT} = 0.1\mu F$ unless otherwise specified.[2]

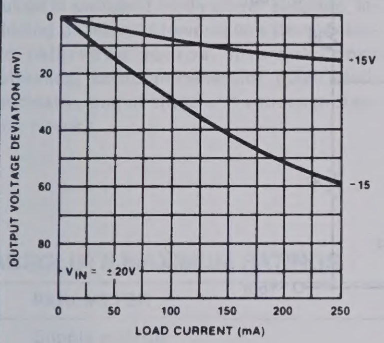
PARAMETER		TEST CONDITIONS	SE5554			NE5554			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{OUT}+$	Positive output voltage		+14.4	+15	+15.6	+14.4	+15	+15.6	
$V_{OUT}-$	Negative output voltage		-15.6	-15	-14.4	-15.6	-15	-14.4	V
ΔV_{OUT}	Line regulation	$\pm 20 \le V_{IN} \le \pm 30V$		100	150		100	300	mV
ΔV_{OUT}	Load regulation	$1mA \le I_{Load} \le 50mA$		10	25		10	50	mV
		$1mA \le I_{Load} \le 200mA$		30	100		30	200	mV
$V_{OUT}+$	Positive output voltage	$1mA \le I_L \le 100mA$	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$V_{OUT}-$	Negative output voltage	$\pm 20V \le V_{IN} \le \pm 30V$ over temp.[1]	-15.75	-15	-14.25	-15.75	-15	-14.25	V
I_Q+	Positive quiescent current	$I_{Load} = 0$		1.70	3.5		1.70	3.5	mA
I_Q-	Negative quiescent current	$I_{Load} = 0$		5.60	8.5		5.60	8.5	mA
	Input/output differential voltage			2.5			2.5		V
V_{BAL}	Output voltage balance			.2			.2		V
	Output noise voltage	100Hz to 10kHz		55			55		μVrms
I_{Peak}	Peak output current			400			400		mA
	Temperature stability of output voltage			1			1		mV/°C

NOTES

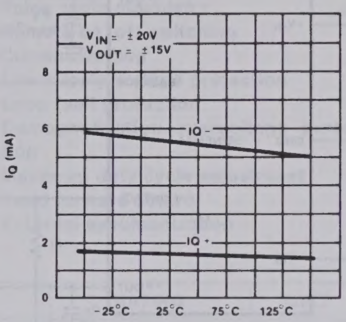
1. Junction temperature range
   SE prefix $-55°C < T_J < 150°C$
   NE prefix $0°C < T_J < 125°C$
2. C_{IN} needed only when remote from filter capacitors
   C_{OUT} needed only if dynamic regulation is to be improved.

TYPICAL PERFORMANCE CHARACTERISTICS

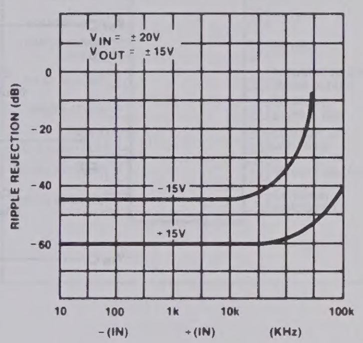
LOAD REGULATION



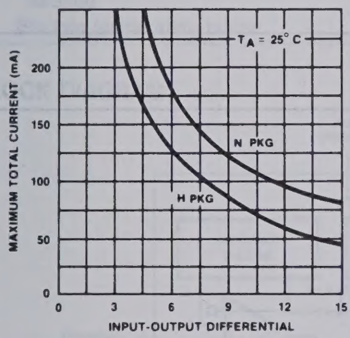
IQ +, IQ −



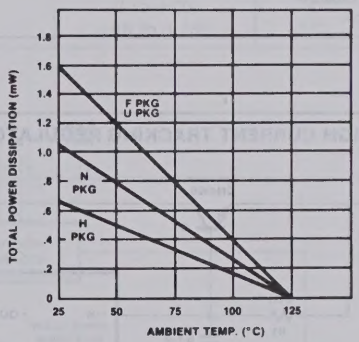
RIPPLE REJECTION



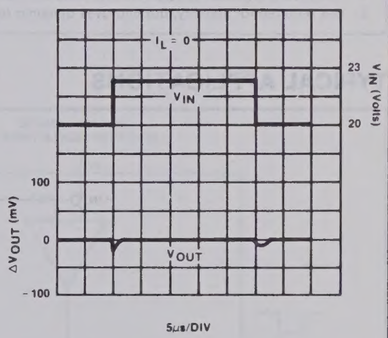
MAXIMUM CURRENT CAPABILITY



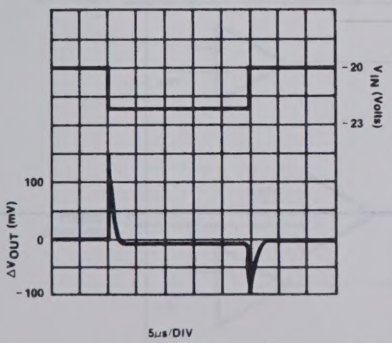
MAXIMUM FREE AIR POWER DISSIPATION



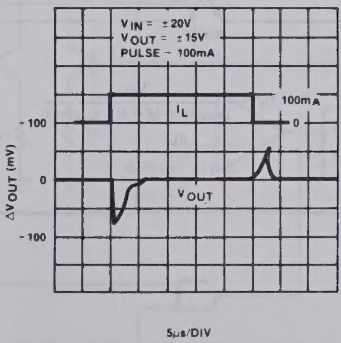
LINE TRANSIENT RESPONSE, POSITIVE



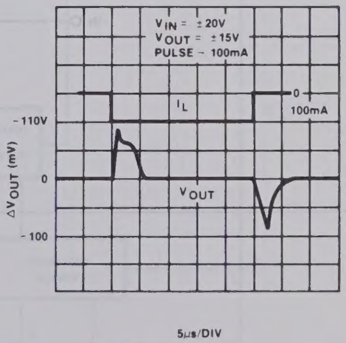
LINE TRANSIENT RESPONSE, NEGATIVE



LOAD TRANSIENT RESPONSE, POSITIVE



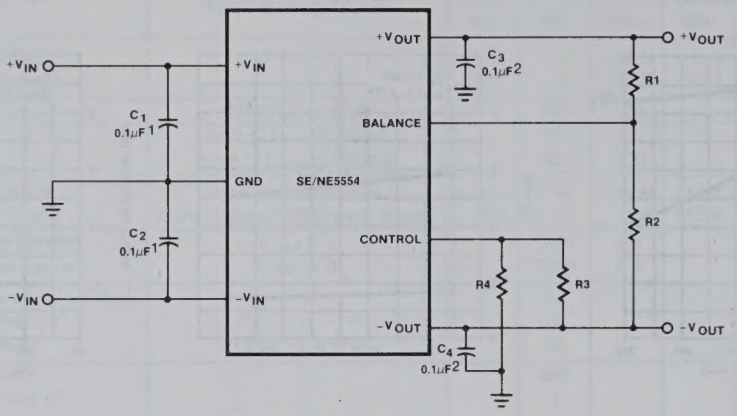
LOAD TRANSIENT RESPONSE, NEGATIVE



4. Device capability in free air.

BLOCK DIAGRAM

TYPICAL CONNECTION


+VOUT
+VIN
C3
0.1µF 2
+VOUT
R1
+VIN
C1
0.1µF 1
BALANCE
GND
SE/NE5554
R2
C2
0.1µF 1
CONTROL
R4
R3
-VIN
-VIN
-VOUT
-VOUT
C4
0.1µF 2

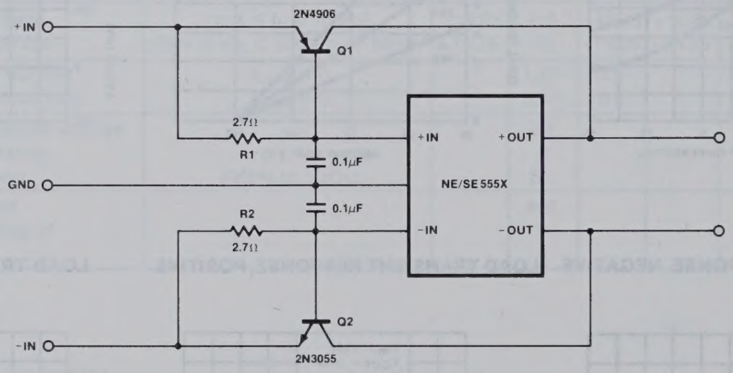
R1 and R2 adjust $+V_{OUT}$
with respect to $-V_{OUT}$
R3 and R4 adjust $-V_{OUT}$
From -5V to -20V

NOTES

1. Required if regulator is operated any distance from filter capacitor.
2. Not required for stability, but improves dynamic regulation.

TYPICAL APPLICATIONS

HIGH CURRENT TRACKING REGULATOR


2N4906
+IN
Q1
2.7Ω
R1
+IN
+OUT
0.1µF
GND
NE/SE 555X
0.1µF
R2
2.7Ω
-IN
-OUT
Q2
-IN
2N3055

$$R1 = R2 = \frac{V_{BE}}{I_{REG}(\max)\,(\beta + 1) - I_{out}(\max)}$$

For

$$\beta_{(Q)} \geq \frac{I_{out\ (max)}}{I_{reg\ (max)}}$$

NE/SE5560-F,N

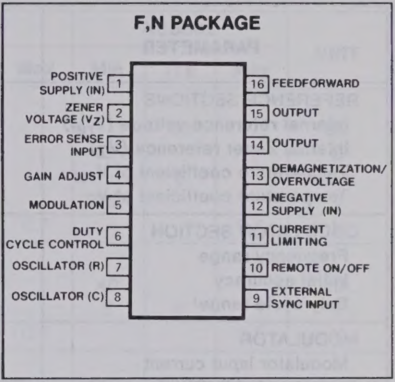
DESCRIPTION

The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- Stabilized power supply
- Temperature compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/overvoltage protection
- Maximum duty cycle adjustment
- Feed forward control
- External synchronization

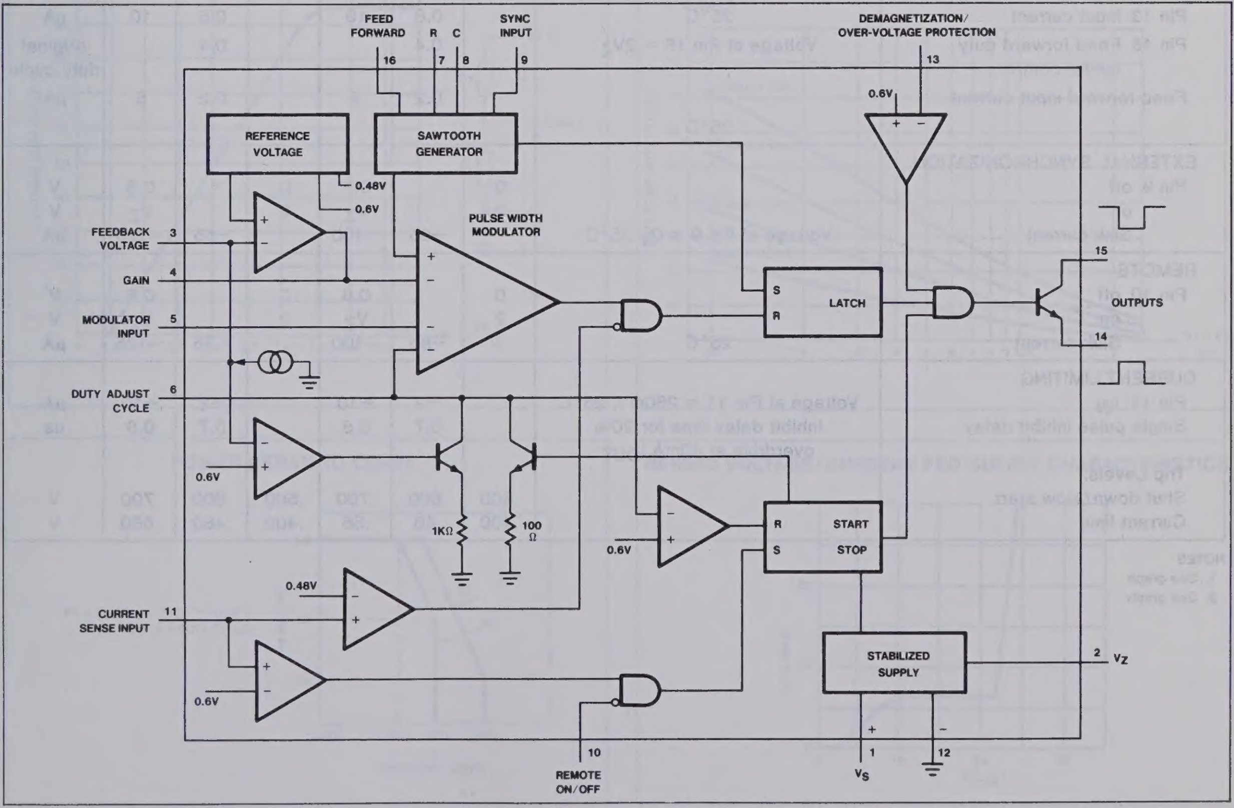
PIN CONFIGURATION


F,N PACKAGE
POSITIVE SUPPLY (IN) 1
ZENER VOLTAGE (VZ) 2
ERROR SENSE INPUT 3
GAIN ADJUST 4
MODULATION 5
DUTY CYCLE CONTROL 6
OSCILLATOR (R) 7
OSCILLATOR (C) 8
16 FEEDFORWARD
15 OUTPUT
14 OUTPUT
13 DEMAGNETIZATION/OVERVOLTAGE
12 NEGATIVE SUPPLY (IN)
11 CURRENT LIMITING
10 REMOTE ON/OFF
9 EXTERNAL SYNC INPUT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage (Voltage sourced)	+18	V
Supply current (Current sourced)	30	mA
Output current	40	mA
Operating temperature range (ambient)		
SE5560	−55 to +125	°C
NE5560	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM


FEED FORWARD
R
C
SYNC INPUT
16
7
8
9
DEMAGNETIZATION/ OVER-VOLTAGE PROTECTION
13
0.6V
REFERENCE VOLTAGE
SAWTOOTH GENERATOR
0.48V
0.6V
PULSE WIDTH MODULATOR
FEEDBACK VOLTAGE 3
GAIN 4
MODULATOR INPUT 5
DUTY ADJUST CYCLE 6
S
R
LATCH
15
OUTPUTS
14
0.6V
1KΩ
100 Ω
0.6V
R START
S STOP
0.48V
CURRENT SENSE INPUT 11
0.6V
STABILIZED SUPPLY
2 VZ
10 REMOTE ON/OFF
+ 1 VS
− 12

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 12V unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTIONS								
Internal reference voltage (V_{ref})	25°C	3.69	3.76	3.84	3.57	3.76	3.96	V
Internal Zener reference (V_Z)	I_L = 7mA	7.8	8.4	9.0	7.8	8.4	9.0	V
Temperature coefficient of V_{ref}				±100		±100		ppm/°C
Temperature coefficient of V_Z				±150		±150		ppm/°C
OSCILLATOR SECTION								
Frequency range		50		100K	50		100K	Hz
Initial accuracy	R = 5K		5			5		%
Duty cycle range[1]	fo = 20kHz	0		98	0		98	%
MODULATOR								
Modulator input current	Voltage at Pin 5 = 1V		0.2	20		0.2	20	µA
HOUSEKEEPING FUNCTION								
Pin 6 Duty cycle limit control	(For 50% Maximum duty cycle) 15kHz to 50kHz	38	40	42	37	40	43	% of V_Z
Pin 6 Input current			.2	20		0.2	20	µA
Pin 1 Low supply voltage protection thresholds		8.5	9.1	10.5	8.5	9.1	10.5	V
Pin 3 Feedback loop protection trip on threshold		400	500	720	400	500	720	mV
Pin 3 Pull up current			−15	−35		−15	−35	µA
Pin 13 Demagnetization/over voltage protection trip on threshold		470	600	720	470	600	720	mV
Pin 13 Input current	25°C		0.6	10		0.6	10	µA
Pin 16 Feed forward duty cycle[2] control	Voltage at Pin 16 = $2V_Z$		0.4			0.4		original duty cycle
Feed forward input current			0.2	5		0.2	5	µA
	25°C							
EXTERNAL SYNCHRONIZATION								
Pin 9 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
Sink current	Voltage at Pin 9 = 0_V 25°C		−65	−100		−65	−125	µA
REMOTE								
Pin 10 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
Sink current	25°C		−85	−100		−75	−125	µA
CURRENT LIMITING								
Pin 11; I_{IN}	Voltage at Pin 11 = 250mV, 25°C		−2	−10		−2	−10	µA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	µs
Trip Levels:								
Shut down/slow start		.500	.600	.700	.500	.600	.700	V
Current limit		.400	.48	.56	.400	.480	.560	V

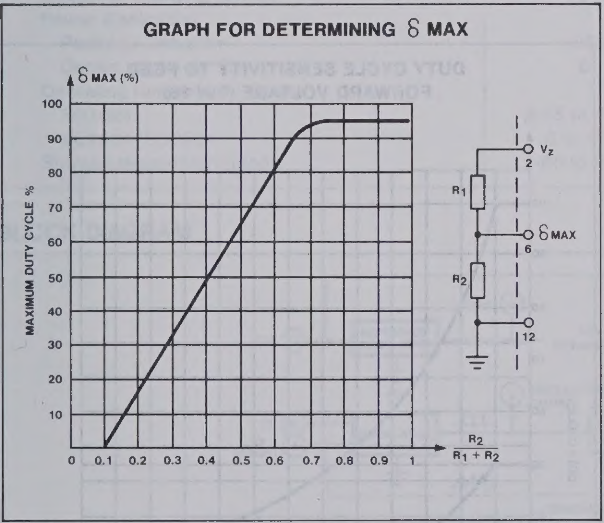
NOTES
1. See graph
2. See graph

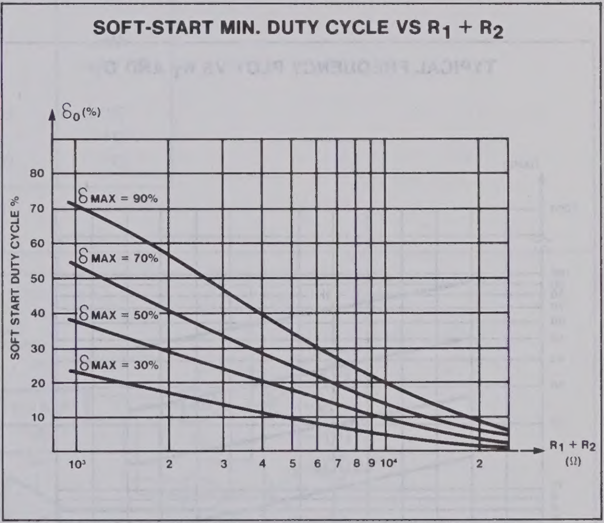
DC ELECTRICAL CHARACTERISTICS (Con't) $T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified

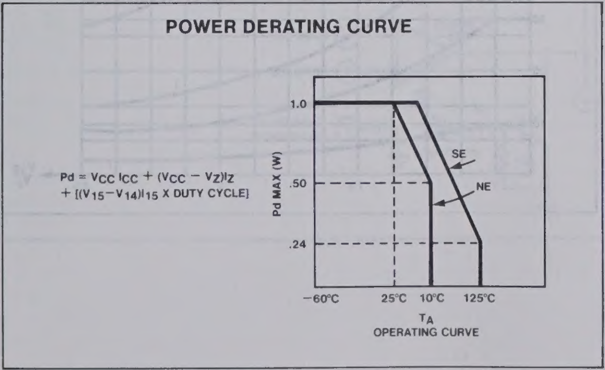
PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER								
Open loop gain			60			60		dB
Feedback resistor		10K			10K			Ω
Small signal bandwith			3			3		MHz
Output voltage swing (positive)		6.2			6.2			V
Output voltage swing (negative)				0.7			0.6	V
OUTPUT STAGE								
Output Current (Pin 15)		40			40			mA
Max emitter voltage (Pin 14)		5	6		5	6		V
$V_{CE}(SAT)$ $I_C = 40mA$				0.5			0.5	V
SUPPLY VOLTAGE/CURRENT								
I_{CC}	$I_Z=0$, Voltage fed, $V_{CC}=12V$, 25°C			10			10	mA
V_{CC}	$I_{CC} = 10$ mA, Current fed	20		23	19		24	V
V_{CC}	$I_{CC} = 30$ mA, Current fed	20		30	20		30	V

NOTES
1. See graph
2. See graph

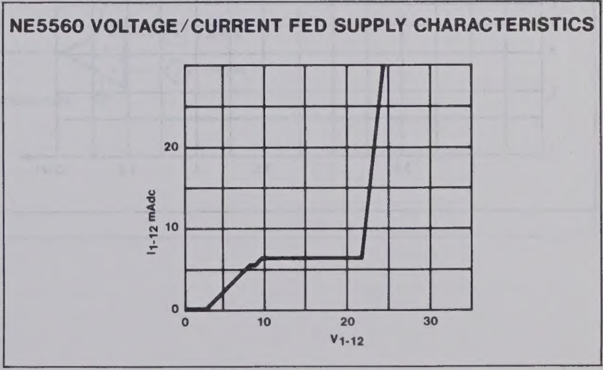
TYPICAL PERFORMANCE CHARACTERISTICS


GRAPH FOR DETERMINING δ MAX


SOFT-START MIN. DUTY CYCLE VS $R_1 + R_2$

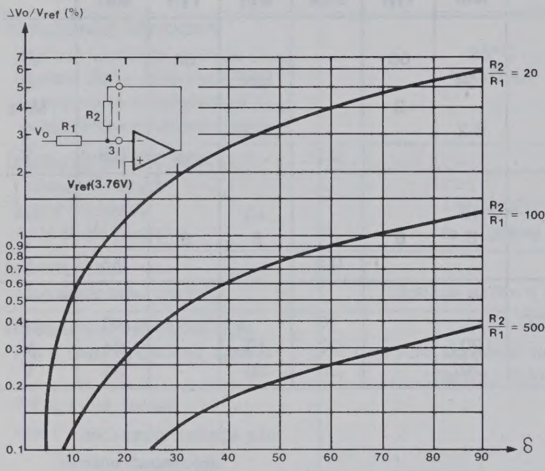

POWER DERATING CURVE

$P_d = V_{CC} I_{CC} + (V_{CC} - V_Z) I_Z + [(V_{15} - V_{14}) I_{15} \times \text{DUTY CYCLE}]$

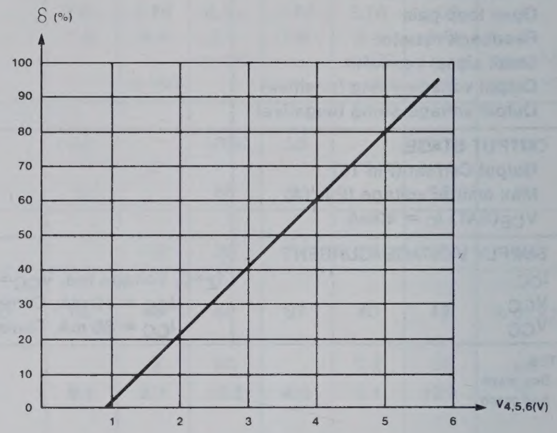

NE5560 VOLTAGE/CURRENT FED SUPPLY CHARACTERISTICS

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

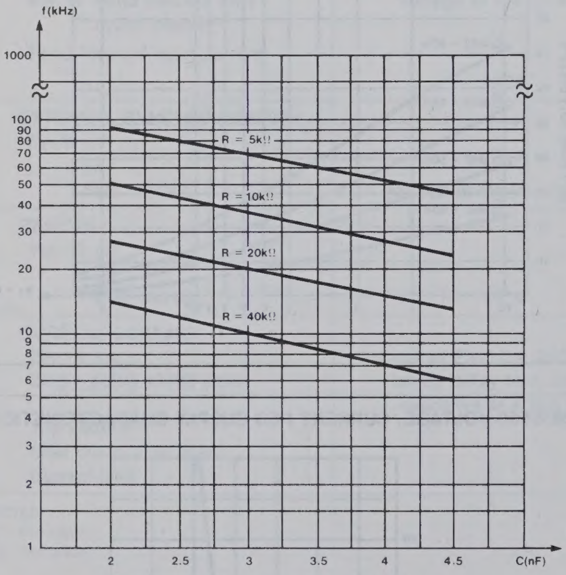
REGULATION VS ERROR AMP CLOSED LOOP GAIN



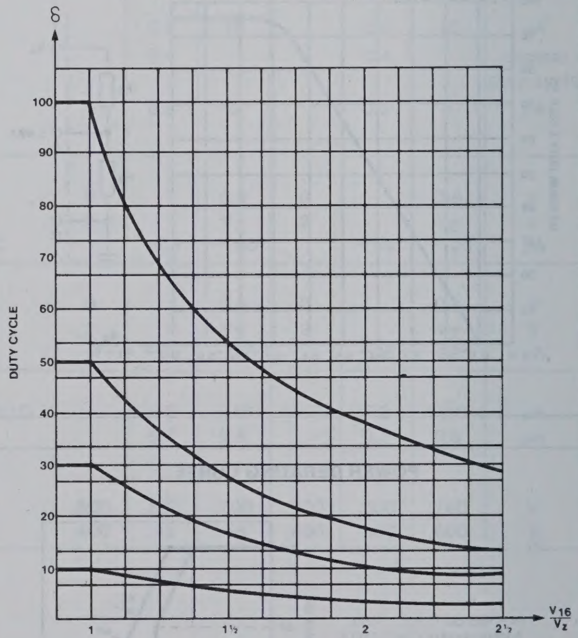
TRANSFER CURVE OF PULSE WIDTH MODULATOR DUTY CYCLE VS INPUT VOLTAGE



TYPICAL FREQUENCY PLOT VS R_T AND C_T



DUTY CYCLE SENSITIVITY TO FEED FORWARD VOLTAGE (PIN 16)



SG1524/SG2524/SG3524-F,N

DESCRIPTION

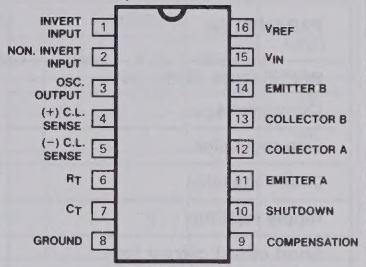
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of −55°C to +125°C, while the SG2524 and SG3524 are designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

CONNECTION DIAGRAM
F,N PACKAGE


INVERT INPUT 1
NON. INVERT INPUT 2
OSC. OUTPUT 3
(+) C.L. SENSE 4
(−) C.L. SENSE 5
R_T 6
C_T 7
GROUND 8
16 V_{REF}
15 V_{IN}
14 EMITTER B
13 COLLECTOR B
12 COLLECTOR A
11 EMITTER A
10 SHUTDOWN
9 COMPENSATION

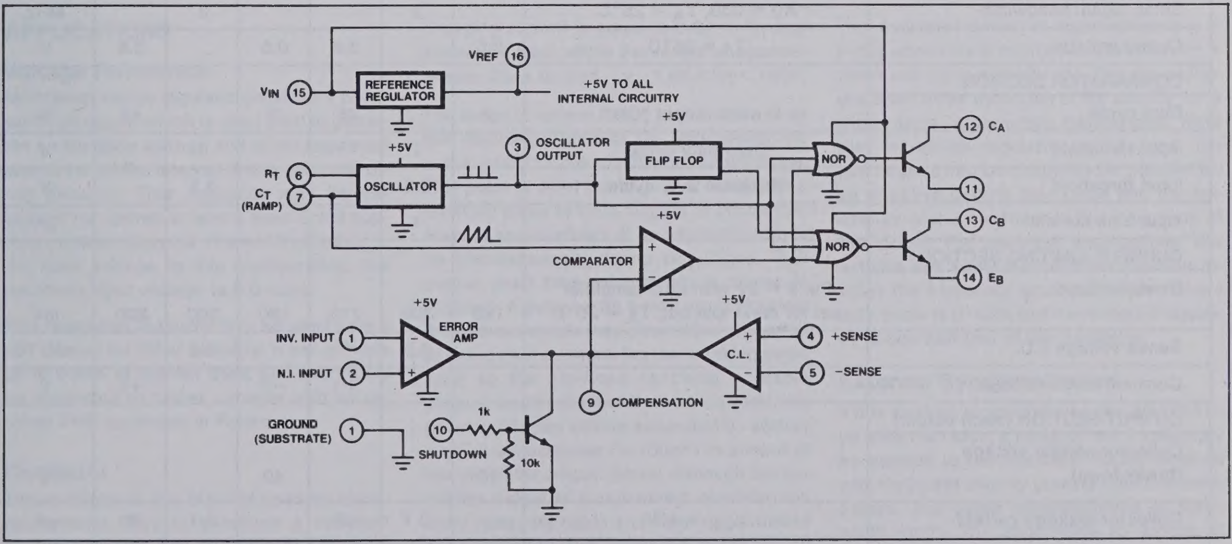
TOP VIEW

ORDER PART NO.
SG1524F, SG2524F
SG2524N, SG3524F
SG3524N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/°C
Operating temperature range		
SG1524	−55 to +125	°C
SG2524/SG3524	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM


V_{REF} 16
V_{IN} 15
REFERENCE REGULATOR
+5V TO ALL INTERNAL CIRCUITRY
+5V
+5V
3 OSCILLATOR OUTPUT
FLIP FLOP
R_T 6
C_T (RAMP) 7
OSCILLATOR
+5V
COMPARATOR
NOR
NOR
12 C_A
11
13 C_B
14 E_B
+5V
ERROR AMP
INV. INPUT 1
N.I. INPUT 2
+5V
C.L.
4 +SENSE
5 −SENSE
9 COMPENSATION
GROUND (SUBSTRATE) 1
10 SHUTDOWN
1k
10k

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, $V_{IN} = 20V$, and f = 20kHz)

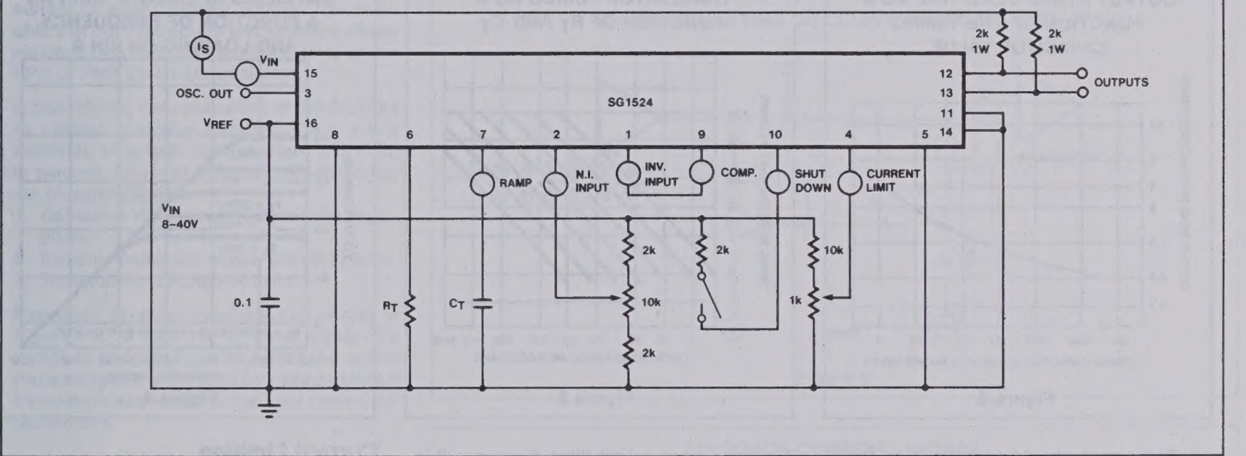
PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	$V_{IN} = 8$ to 40V		10	20		10	30	mV
Load regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
Ripple rejection	f = 120Hz, $T_A = 25°C$		66			66		dB
Short circuit current limit	$V_{REF} = 0$, $T_A = 25°C$		100			100		mA
Temperature stability	Over operating temperature range		0.3	1		0.3	1	%
Long term stability	$T_A = 25°C$		20			20		mV/kHr
OSCILLATOR SECTION								
Maximum frequency	$C_T = .001$ mfd, $R_T = 2k\Omega$		300			300		kHz
Initial accuracy	R_T and C_T constant		5			5		%
Voltage stability	$V_{IN} = 8$ to 40V, $T_A = 25°C$			1			1	%
Temperature stability	Over operating temperature range						2	%
Output amplitude	Pin 3, $T_A = 25°C$		3.5			3.5		V_P
Output pulse width	$C_T = .01$ mfd, $T_A = 25°C$		0.5			0.5		μs
ERROR AMPLIFIER SECTION								
Input offset voltage	$V_{CM} = 2.5V$		0.5	5		2	10	mV
Input bias current	$V_{CM} = 2.5V$		2	10		2	10	μA
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	$T_A = 25°C$	1.8		3.4	1.8		3.4	V
Common mode rejection ratio	$T_A = 25°C$		70			70		dB
Small signal bandwidth	$A_V = 0dB$, $T_A = 25°C$		3			3		MHz
Output voltage	$T_A = 25°C$	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION								
Duty cycle	% each output "ON"	0		45	0		45	%
Input threshold	Zero duty cycle		1			1		V
Input threshold	Maximum duty cycle		3.5			3.5		V
Input bias current			1			1		μA
CURRENT LIMITING SECTION								
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25°C$	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		mV/°C
Common mode voltage		−1		+1	−1		+1	V
OUTPUT SECTION (each output)								
Collector-emitter voltage (breakdown)		40			40			V
Collector-leakage current	$V_{CE} = 40V$		0.1	50		0.1	50	μA
Saturation voltage	$I_C = 50mA$		1	2		1	2	V
Emitter output voltage	$V_{IN} = 20V$	17	18		17	18		V

DC ELECTRICAL CHARACTERISTICS (Cont'd)

(Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, $V_{IN} = 20V$, and f = 20kHz)

PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
Rise time	R_C = 2K ohm, T_A = 25°C		0.2			0.2		μs
Fall time	R_C = 2K ohm, T_A = 25°C		0.1			0.1		μs
TOTAL STANDBY CURRENT (excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V		8	10		8	10	mA

OPEN LOOP TEST CIRCUIT



APPLICATIONS

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

Oscillator

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V \div R_T$ and should be kept within the range of approximately 30μA to 2mA, i.e., $1.8K < R_T < 100K$.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (≈100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately t = R_TC_T where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG1524 to an external clock, a pulse of ≈+3 volts may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more SG1524's must be synchronized together, one must be designated as master with its R_TC_T set for the correct peri-

TYPICAL APPLICATION

EXPANDED REFERENCE CURRENT CAPABILITY

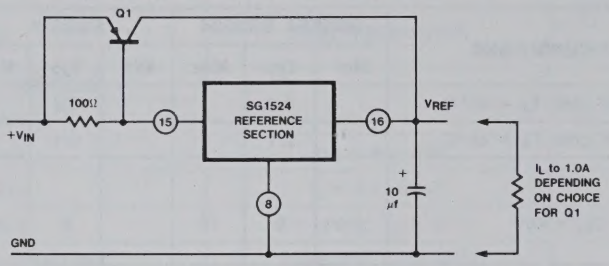


Figure 1

OUTPUT STAGE DEAD TIME AS A FUNCTION OF THE TIMING CAPACITOR VALUE

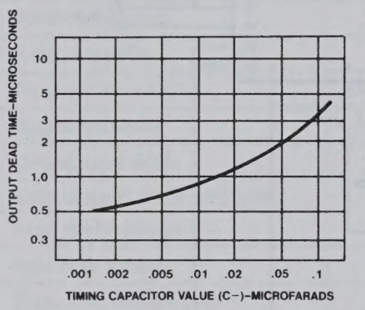


Figure 2

OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

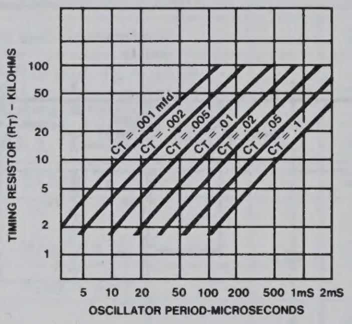


Figure 3

AMPLIFIES OPEN-LOOP GAIN AS A FUNCTION OF FREQUENCY AND LOADING ON PIN 9

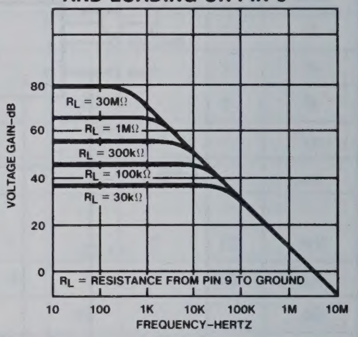


Figure 4

od. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node ($R_L \approx 5M\Omega$). The gain is

$$A_V = g_m R_L = \frac{8\, I_C\, R_L}{2kT} \approx .002\, R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200µA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the SG1524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1,

$$\text{Threshold} = V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)$$
$$= I_1R_2 \approx 200\text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ± 1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 14). Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

Output Circuits

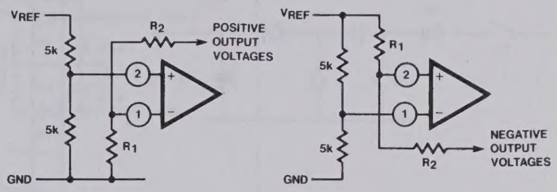
The outputs of the SG1524 are two identical NPN transistors with both collectors and emitters uncommitted. This circuitry is very similar to that used in the SG111 comparator in that each output transistor has antisaturation circuitry for fast response, and current limiting set for a maximum output current of approximately 100mA. The availability of both collectors and emitters allows maximum versatility to enable driving either NPN or PNP external transistors.

In considering the application of the SG1524 to voltage regulator circuitry, there are a multitude of output configurations possible. In general, however, they fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

Examples of each category are shown in Figures 8, 9 and 10. In each case, the switches indicated can be either the output transistors in the SG1524 or added external transistors according to the load current requirements.

ERROR AMPLIFIER BIASING CIRCUITS



$$V_O = \frac{2.5V\,(R + R_2)}{R_1} \qquad \frac{R_1\ R_2}{R_2 + R_2} = 2.5k\Omega$$

Note change in input connections for opposite polarity outputs.

Figure 5

CURRENT LIMITING CIRCUITRY OF THE SG 1524

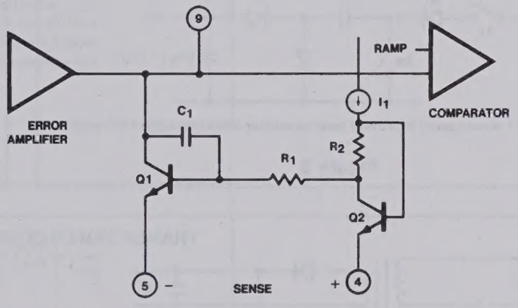


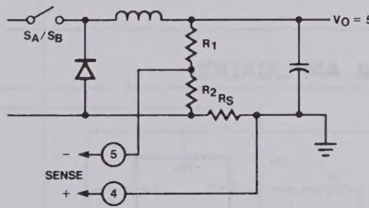
Figure 6

FOLDBACK CURRENT LIMITING

$$I_{MAX} = \frac{1}{R_S}\left(V_{TH} + \frac{V_O\ R_2}{R_1 + R_2}\right)$$

$$I_{SC} = \frac{V_{TH}}{R_S} \quad \text{WHERE}$$

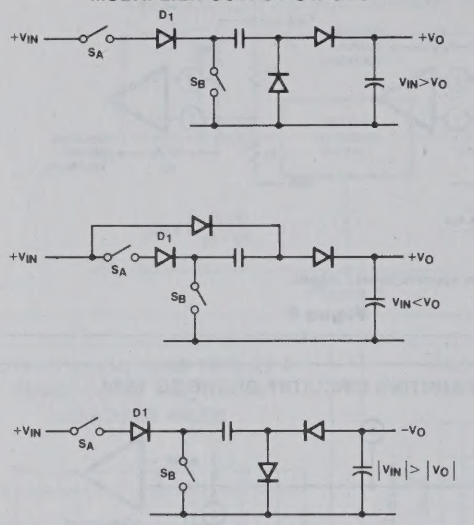
$$V_{TH} = 200\ \text{mV}$$



Foldback current limiting can be used to reduce power dissipation under shorted output conditions.

Figure 7

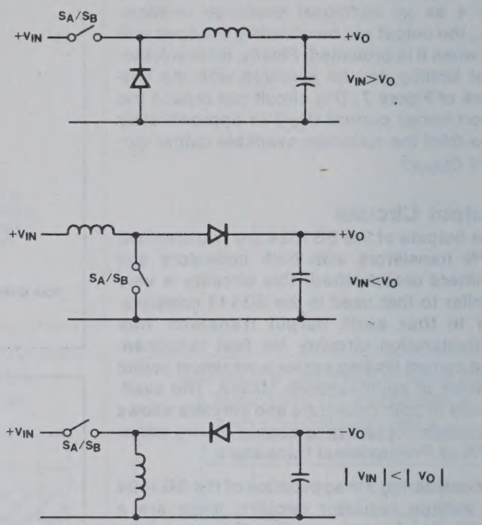
CAPACITOR-DIODE COUPLED VOLTAGE MULTIPLIER OUTPUT STAGES


+VIN
SA
D1
SB
+VO
VIN>VO
+VIN
D1
SA
SB
+VO
VIN<VO
+VIN
D1
SA
SB
−VO
|VIN|>|VO|

Note: Diode D1 is necessary to prevent reverse emitter-base breakdown to transistor switch S_A.

Figure 8

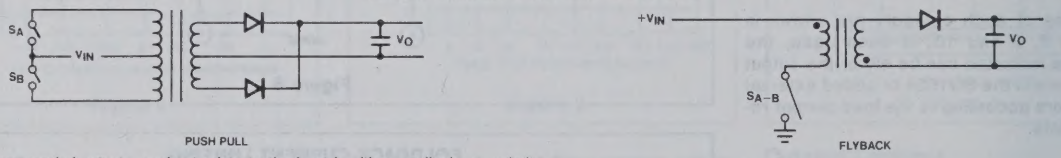
SINGLE-ENDED INDUCTOR CIRCUITS


SA/SB
+VIN
+VO
VIN>VO
+VIN
+VO
SA/SB
VIN<VO
+VIN
SA/SB
−VO
|VIN|<|VO|

Single-ended inductor circuits where the two outputs of the SG1524 are connected in parallel.

Figure 9

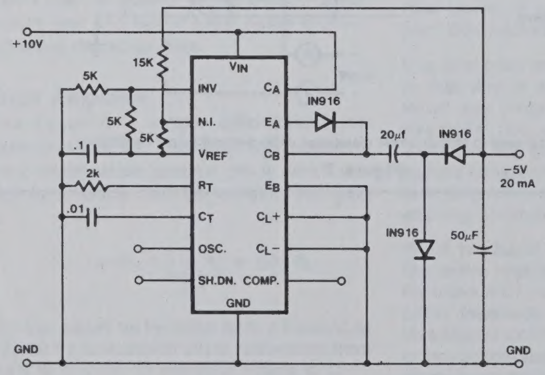
TRANSFORMER-COUPLED OUTPUTS


SA
VIN
SB
VO
PUSH PULL
+VIN
VO
SA−B
FLYBACK

Transformer-coupled outputs need not relate to the input in either amplitude or polarity.

Figure 10

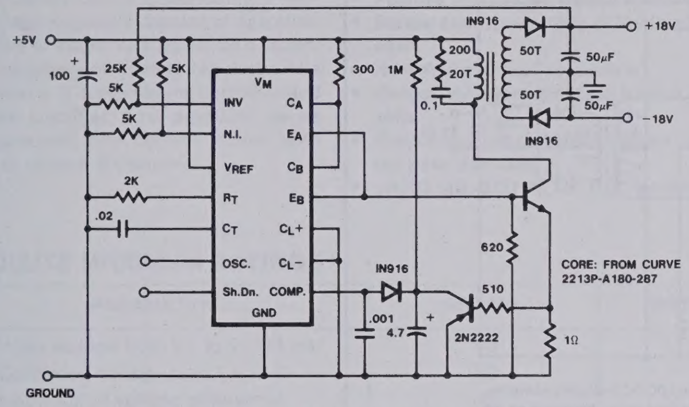
TYPICAL APPLICATION


+10V
15K
VIN
5K
INV
CA
5K
N.I.
EA
5K
IN916
.1
VREF
CB
20μf
IN916
2k
RT
EB
−5V
20 mA
.01
CT
CL+
OSC.
CL−
IN916
50μF
SH.DN. COMP.
GND
GND
GND

The capacitor-diode output circuit is used here as a polarity converter to generate a −5 volt supply from +15 volts. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Figure 11

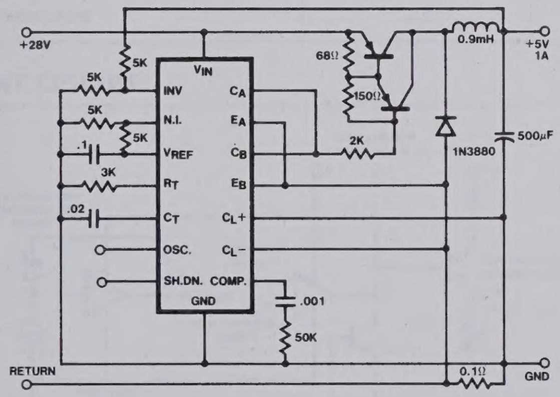
TYPICAL APPLICATION


+5V
100
25K
5K
5K
5K
VM
INV
CA
N.I.
EA
VREF
CB
2K
RT
EB
.02
CT
CL+
OSC.
CL−
Sh.Dn.
COMP.
GND
GROUND
300
1M
200
20T
0.1
IN916
50T
50µF
+18V
50T
50µF
−18V
IN916
620
CORE: FROM CURVE 2213P-A180-287
IN916
510
.001
4.7
2N2222
1Ω

Another low-current supply is the flyback converter used here to generate ±15 volts at 20mA from a +5 volt regulated line. The reference generator in the SG1524 is unused with the input voltage providing the reference. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

Figure 12

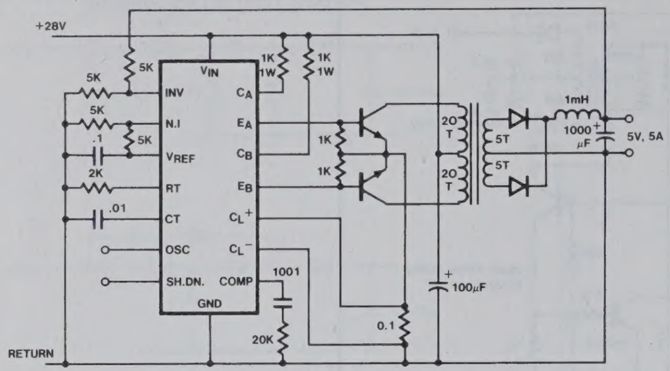
TYPICAL APPLICATION


+28V
5K
5K
5K
5K
.1
3K
.02
VIN
INV
CA
N.I.
EA
VREF
CB
RT
EB
CT
CL+
OSC.
CL−
SH.DN.
COMP.
GND
.001
50K
RETURN
68Ω
150Ω
2K
0.9mH
+5V 1A
1N3880
500µF
0.1Ω
GND

In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective .0-90% duty-cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.

Figure 13

TYPICAL APPLICATION


+28V
5K
5K
5K
.1
5K
2K
.01
V_{IN}
INV
N.I
V_{REF}
RT
CT
OSC
SH.DN.
GND
C_A
E_A
C_B
E_B
C_L^+
C_L^-
COMP
1K 1W
1K 1W
1K
1K
20 T
20 T
5T
5T
1mH
1000 μF
5V, 5A
100μF
1001
20K
0.1
RETURN

Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

Figure 14

PRECISION VOLTAGE REGULATOR

μA723/723C/SA723C

μA723/723C-F,H,N
SA723C-N
μA723C-D

DESCRIPTION

The μA723/SA723C is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The 723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

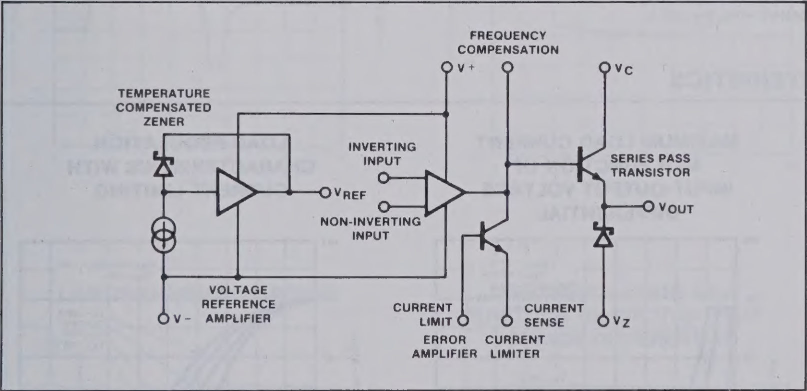
FEATURES

- **Positive or negative supply operation**
- **Series, shunt, switching or floating operation**
- **.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts**
- **Output current to 150mA without external pass transistor**
- **μA723 MIL STD 88 3A, B, C available**

ABSOLUTE MAXIMUM RATINGS

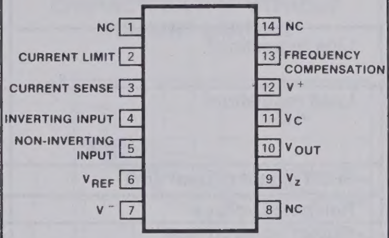
PARAMETER	RATING	UNIT
Pulse voltage from V+ to V- (50 ms)	50	V
Continous voltage from V+ to V-	40	V
Input-output voltage differential	40	V
Maximum output current	150	mA
Current from V_{REF}	15	mA
Current from V_Z	25	mA
Internal power dissipation[1]	800	mw
Operating temperature range		
μA723	-55 to +125	°C
μA723C	0 to 70	°C
SA723C	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature	300	°C

EQUIVALENT CIRCUIT


FREQUENCY COMPENSATION
V+
VC
TEMPERATURE COMPENSATED ZENER
INVERTING INPUT
SERIES PASS TRANSISTOR
VREF
VOUT
NON-INVERTING INPUT
VOLTAGE REFERENCE AMPLIFIER
V-
CURRENT LIMIT
CURRENT SENSE
VZ
ERROR AMPLIFIER
CURRENT LIMITER

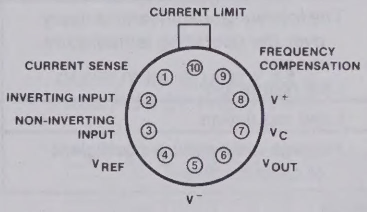
PIN CONFIGURATIONS

D,F,N PACKAGE


NC 1
CURRENT LIMIT 2
CURRENT SENSE 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
VREF 6
V- 7
14 NC
13 FREQUENCY COMPENSATION
12 V+
11 VC
10 VOUT
9 VZ
8 NC

ORDER PART NO.
μA723F,N
μA723CF,CN
SA723CN
μA723CD

H PACKAGE*


CURRENT LIMIT
CURRENT SENSE
FREQUENCY COMPENSATION
INVERTING INPUT
V+
NON-INVERTING INPUT
VC
VREF
VOUT
V-
1
2
3
4
5
6
7
8
9
10

ORDER PART NO.
μA723H
μA723CH

*Metal cans (H) not recommended for new designs

µA723/723C-F,H,N
SA723C-N
µA723C-D

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1]

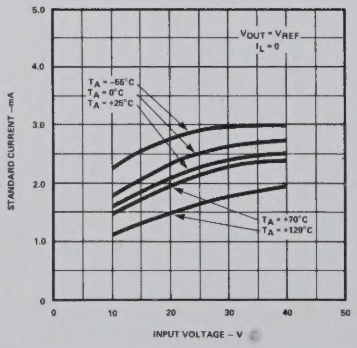
PARAMETER	TEST CONDITIONS	µA723			µA723C/SA723C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Line regulation[2]	$V_{IN} = 12V$ to $V_{IN} = 15V$		0.01	0.1		0.01	0.1	$\%V_{OUT}$
	$V_{IN} = 12V$ to $V_{IN} = 40V$		0.02	0.2		0.1	0.5	$\%V_{OUT}$
Load regulation[2]	$I_L = 1mA$ to $I_L = 50mA$		0.03	0.15		0.03	0.2	$\%V_{OUT}$
	f = 50Hz to 10kHz, $C_{REF} = 0$		74			74		dB
	f = 50Hz to 10kHz, $C_{REF} = 5\mu F$		86			86		dB
Short circuit current limit	$R_{SC} = 10\Omega$, $V_{OUT} = 0$		65			65		mA
Reference voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output noise voltage	BW = 100Hz to 10kHz, $C_{REF} = 0$		20			20		µVrms
	BW = 100Hz to 10kHz, $C_{REF} = 5\mu F$		2.5			2.5		µVrms
Long term stability			0.1			0.1	0.1	%/1000hrs.
Standby current drain	$I_L = 0$, $V_{IN} = 30V$		2.3	3.5		2.3	4.0	mA
Input voltage range		9.5		40	9.5		40	V
Output voltage range		2.0		37	2.0		37	V
Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges								
Line regulation				0.3			0.3	$\%V_{OUT}$
Load regulation				0.6			0.6	$\%V_{OUT}$
Average temperature coefficient of output voltage	$V_{IN} = 12V$ to $V_{IN} = 15V$ $I_L = 1mA$ to $I_L = 50mA$		0.002	0.015		0.003	0.015	%/°C

NOTES

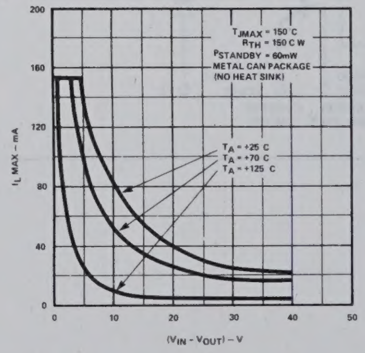
1. $V_{IN} = V+ = V_C = 12V$, $V- = 0V$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10k\Omega$ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

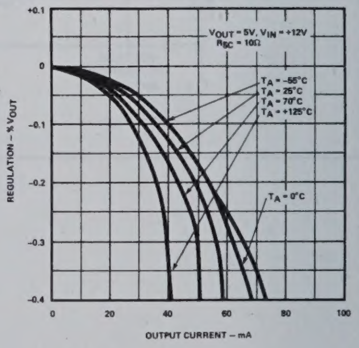
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

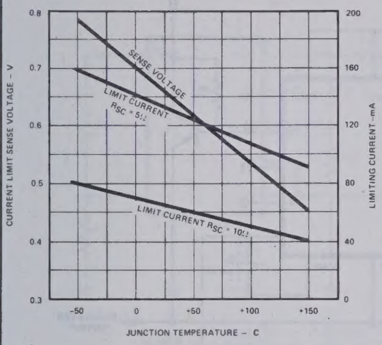


LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

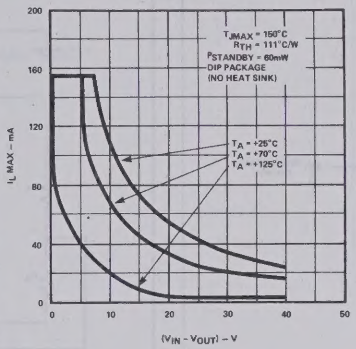


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

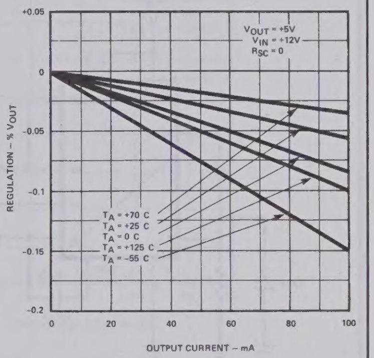
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



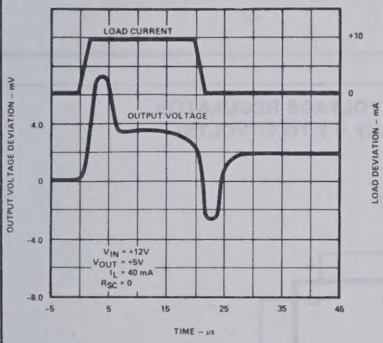
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



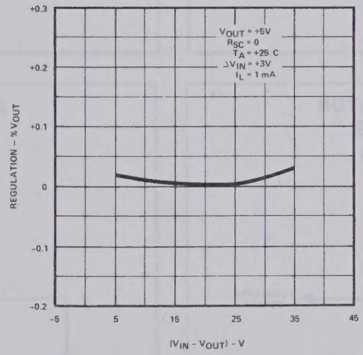
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



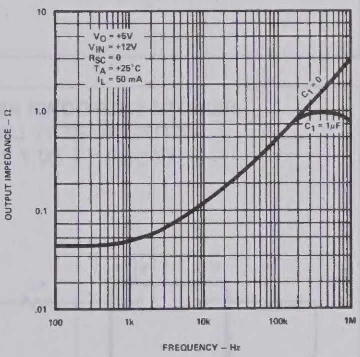
LOAD TRANSIENT RESPONSE



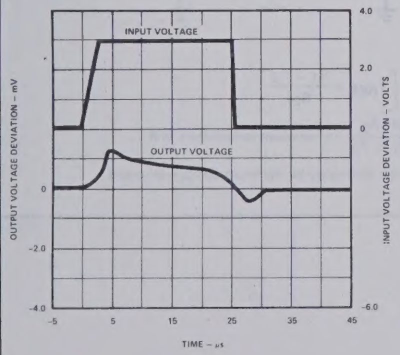
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



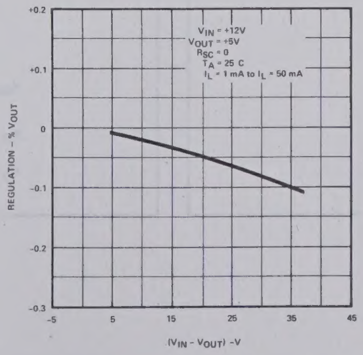
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



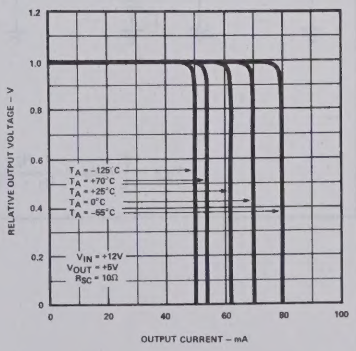
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

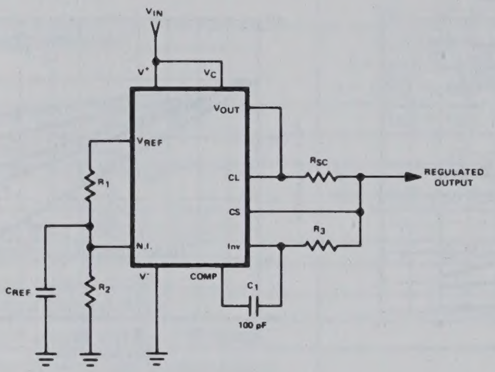


CURRENT LIMITING CHARACTERISTICS



TYPICAL APPLICATIONS

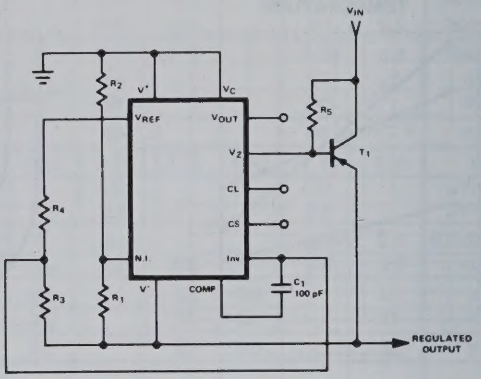
LOW VOLTAGE REGULATOR (V$_{OUT}$ = 2 TO 7 VOLTS)


VIN
V+
VC
VOUT
VREF
R1
RSC
REGULATED OUTPUT
CL
CS
R3
N.I.
Inv
CREF
R2
V−
COMP
C1
100 pF

$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

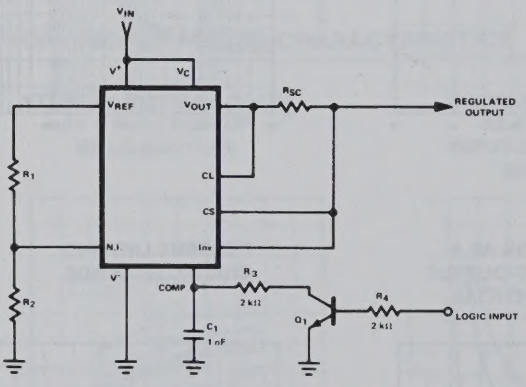
$R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift

NEGATIVE VOLTAGE REGULATOR


VIN
R2
V+
VC
VREF
VOUT
R5
VZ
T1
CL
CS
R4
N.I.
Inv
C1
100 pF
R3
R1
V−
COMP
REGULATED OUTPUT

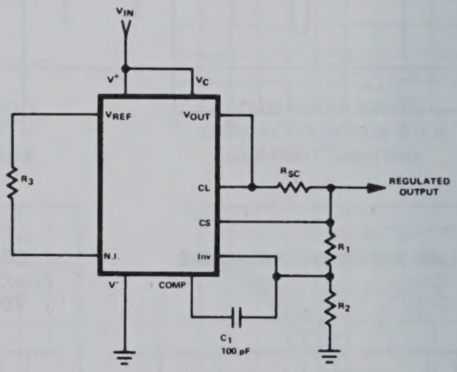
$$V_{out} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R2}{R_1}\right];\quad R_3 = R_4$$

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V$_{OUT}$ = 2 TO 7 VOLTS)


VIN
V+
VC
RSC
VREF
VOUT
REGULATED OUTPUT
R1
CL
CS
N.I.
Inv
V−
R3
2 kΩ
COMP
R4
R2
Q1
2 kΩ
LOGIC INPUT
C1
1 nF

$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R2}\right]$$

HIGH VOLTAGE REGULATOR (V$_{OUT}$ = 7 TO 37 VOLTS)


VIN
V+
VC
VREF
VOUT
R3
RSC
CL
REGULATED OUTPUT
CS
R1
N.I.
Inv
V−
COMP
R2
C1
100 pF

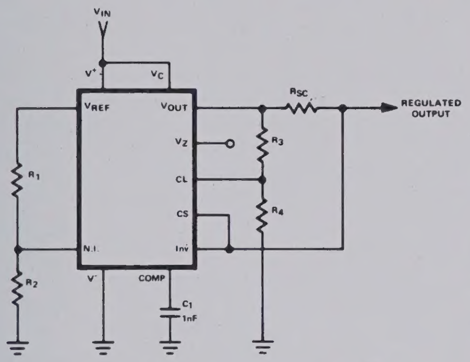
$$V_{out} = \left[V_{REF} \times \frac{R_1 + \quad 2}{R_2}\right]$$

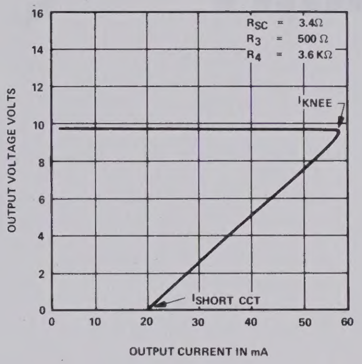
$R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift

R_3 may be eliminated for minimum component count

TYPICAL APPLICATIONS (Cont'd)

FOLDBACK CURRENT LIMITING REGULATOR
(V_{OUT} = 2 TO 7 VOLTS)


V_{IN}
V^+
V_C
V_{REF}
V_{OUT}
V_Z
CL
CS
N.I.
INV
V^-
COMP
R_{SC}
REGULATED OUTPUT
R_1
R_2
R_3
R_4
C_1
1nF



$$I_{KNEE} = \left[\frac{V_{out}\,R_3}{R_{SC}\,R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC}\,R_4}\right]$$

$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}\right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT}\ I_{SC}}{V_{SENSE}\ (I_{KNEE} - I_{SHORTCKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

SECTION 4
TIMERS

Section 4—TIMERS

NE/SE555/SE555C	Timer	177
NE/SA/SE556	Dual Timer	180
NE/SA/SE556-1/SE556-1C	Dual Timer	183
NE/SA/SE558	Quad Timer	186

NE/SE555/SE555C-F,H,N,FE

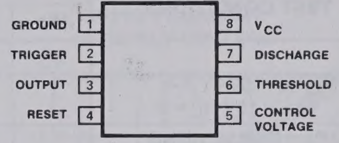
DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

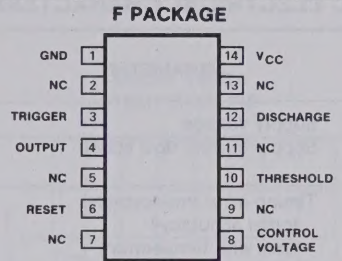
FEATURES

- **Turn off time less than 2μs**
- **Maximum operating frequency greater than 500kHz**
- **Timing from microseconds to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**

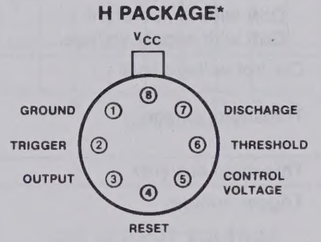
PIN CONFIGURATIONS


N, FE PACKAGE
GROUND
1
TRIGGER
2
OUTPUT
3
RESET
4
8
VCC
7
DISCHARGE
6
THRESHOLD
5
CONTROL VOLTAGE

ORDER PART NO.
NE/SE555N,FE
SE555CN,CFE


F PACKAGE
GND
1
NC
2
TRIGGER
3
OUTPUT
4
NC
5
RESET
6
NC
7
14
VCC
13
NC
12
DISCHARGE
11
NC
10
THRESHOLD
9
NC
8
CONTROL VOLTAGE

ORDER PART NO.
NE/SE555F
SE555CF


H PACKAGE*
VCC
8
GROUND
1
7
DISCHARGE
TRIGGER
2
6
THRESHOLD
OUTPUT
3
5
CONTROL VOLTAGE
4
RESET

ORDER PART NO.
NE/SE555H
SE555CH

*Metal cans (H) not recommended for new designs

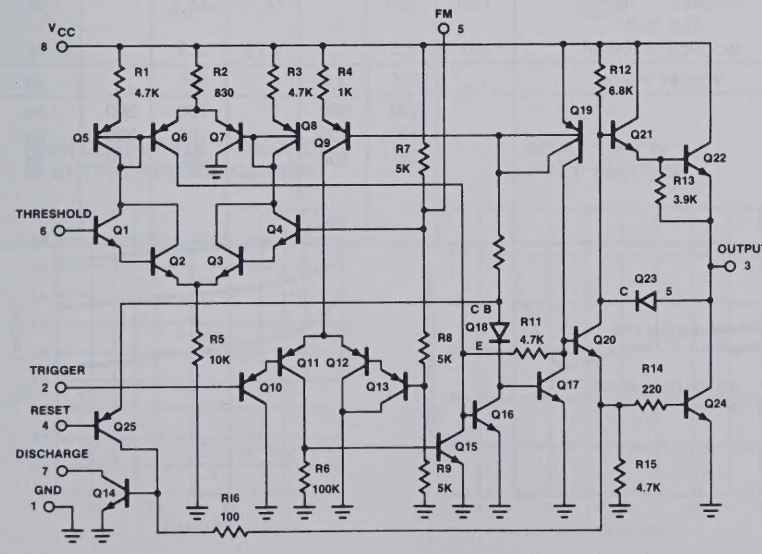
APPLICATIONS

- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Missing pulse detector**

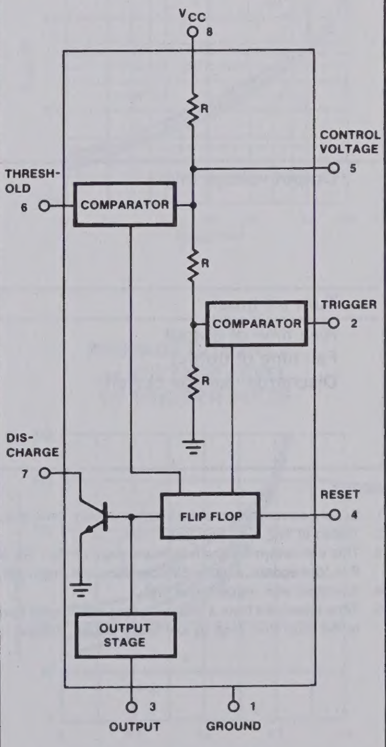
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C,	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	°C
SE555, SE555C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	300	°C

EQUIVALENT SCHEMATIC


VCC
8
FM
5
R1
4.7K
R2
830
R3
4.7K
R4
1K
R12
6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R7
5K
R13
3.9K
THRESHOLD
6
Q1
Q4
Q2
Q3
OUTPUT
3
Q23
C
5
C B
Q18
E
R11
4.7K
Q20
R5
10K
R8
5K
TRIGGER
2
Q10
Q11
Q12
Q13
Q17
R14
220
Q24
RESET
4
Q25
Q16
DISCHARGE
7
Q15
GND
1
Q14
R6
100K
R9
5K
R15
4.7K
RI6
100

BLOCK DIAGRAM


VCC
8
R
CONTROL VOLTAGE
5
THRESH-OLD
6
COMPARATOR
R
TRIGGER
2
COMPARATOR
R
DIS-CHARGE
7
RESET
4
FLIP FLOP
OUTPUT STAGE
3
OUTPUT
1
GROUND

NE/SE555/SE555C-F,H,N,FE

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

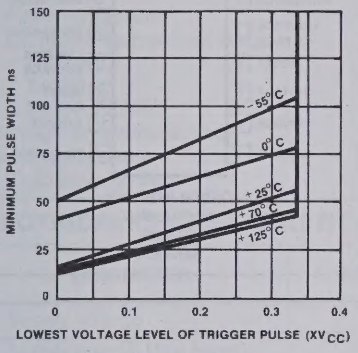
PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	mA
Timing error (monostable)	R_A = 2KΩ to 100KΩ							
Initial accuracy[2]	C = 0.1μF		0.5	2.0		1.0	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		1.5			2.25		%
Drift with temperature	V_{CC} = 15V		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	V_{CC} = 15V	9.6	10.0	10.4	9.0	10.0	11.0	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	V_{CC} = 15V	9.4	10.0	10.6	8.8	10.0	11.2	V
	V_{CC} = 5V	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			0.1	0.25		0.1	0.25	μA
Trigger voltage	V_{CC} = 15V	4.8	5.0	5.2	4.5	5.0	5.6	V
	V_{CC} = 5V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	V_{TRIG} = 0V		0.5	0.9		0.5	2.0	μA
Reset voltage[4]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	V_{RESET} = 0V		0.4	1.0		0.4	1.5	mA
Output voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25		0.3	0.4	V
	I_{SINK} = 5mA		0.05	0.2		0.25	0.35	V
Output voltage (high)	V_{CC} = 15V							
	I_{SOURCE} = 200mA		12.5			12.5		V
	I_{SOURCE} = 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V							
	I_{SOURCE} = 100mA	3.0	3.3		2.75	3.3		V
Turn off time[5]	V_{RESET} = V_{CC}		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

NOTES

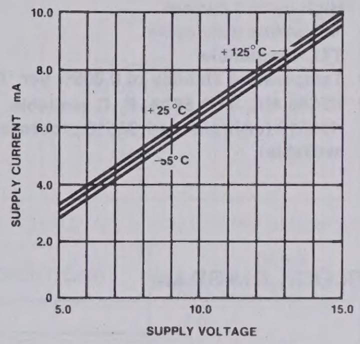
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total R = 10 megohm, and for 5V operation, the max total R = 3.4 megohm.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8 x V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

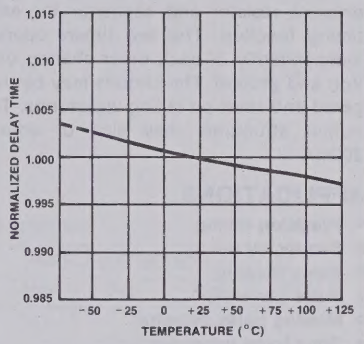
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



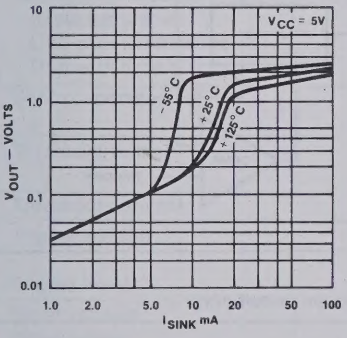
SUPPLY CURRENT vs SUPPLY VOLTAGE



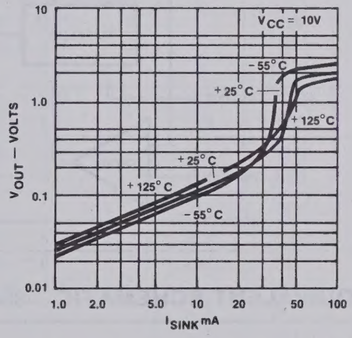
DELAY TIME vs TEMPERATURE



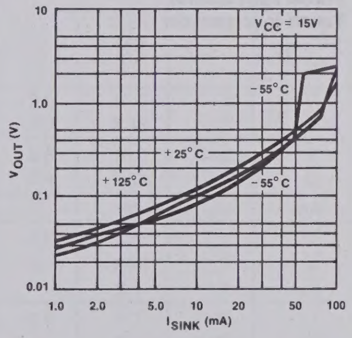
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



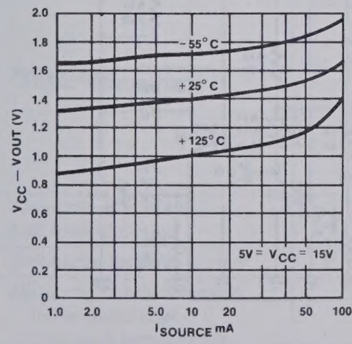
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



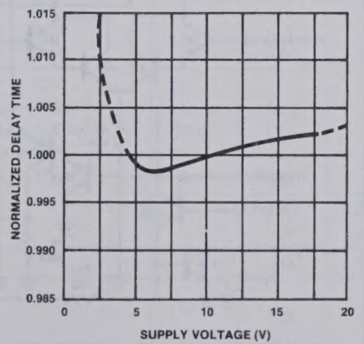
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



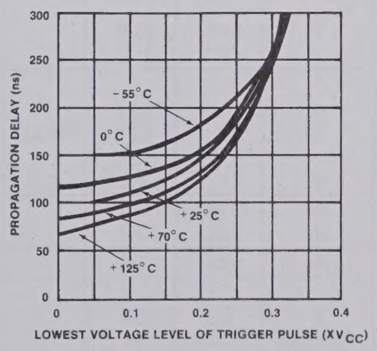
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



DUAL TIMER

NE/SA/SE556

NE/SE556-F,N • SA556-N
SE556C-N

DESCRIPTION

The 556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

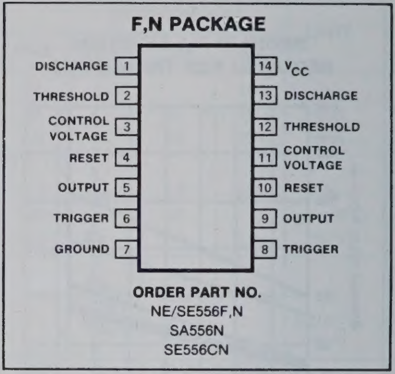
APPLICATIONS

- **Precision timing**
- **Sequential timing**
- **Pulse shaping**
- **Pulse generator**
- **Missing pulse detector**
- **Tone burst generator**
- **Pulse width modulation**
- **Time delay generator**
- **Frequency division**
- **Industrial controls**
- **Pulse position modulation**
- **Appliance timing**
- **Traffic light control**
- **Touch tone encoder**

FEATURES

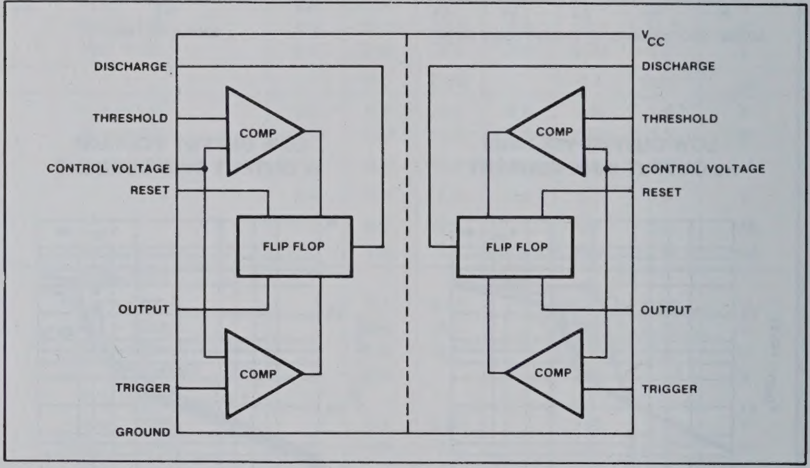
- **Timing from microseconds to hours**
- **Replaces two 555 timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**
- **SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).**

PIN CONFIGURATION

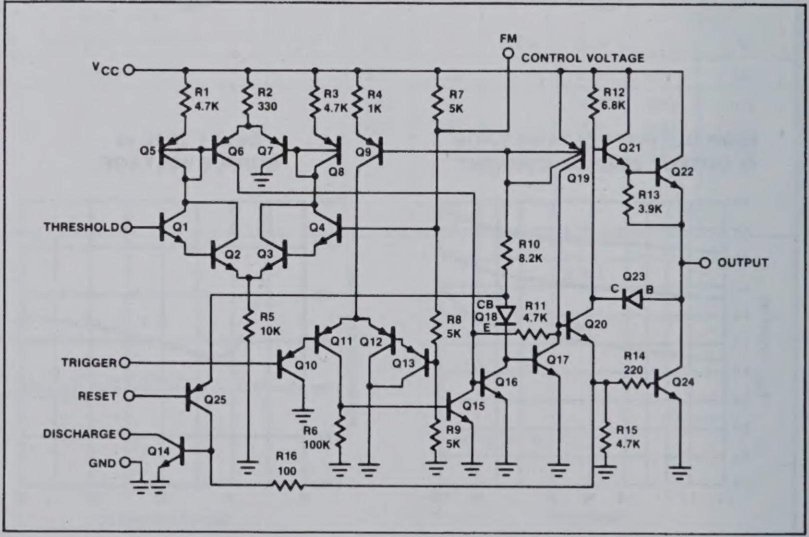

F,N PACKAGE
DISCHARGE 1
THRESHOLD 2
CONTROL VOLTAGE 3
RESET 4
OUTPUT 5
TRIGGER 6
GROUND 7
14 V_{CC}
13 DISCHARGE
12 THRESHOLD
11 CONTROL VOLTAGE
10 RESET
9 OUTPUT
8 TRIGGER

ORDER PART NO.
NE/SE556F,N
SA556N
SE556CN

BLOCK DIAGRAM


DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
GROUND
COMP
FLIP FLOP
COMP
V_{CC}
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
COMP
FLIP FLOP
COMP

EQUIVALENT SCHEMATIC (Shown for one circuit only)


FM
CONTROL VOLTAGE
V_{CC}
R1 4.7K
R2 330
R3 4.7K
R4 1K
R7 5K
R12 6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R13 3.9K
THRESHOLD
Q1
Q2
Q3
Q4
R10 8.2K
OUTPUT
Q23
C
B
R5 10K
CB
Q18
E
R11 4.7K
Q20
R8 5K
Q11
Q12
Q13
TRIGGER
Q10
Q17
R14 220
Q24
Q16
RESET
Q25
Q15
DISCHARGE
R6 100K
R9 5K
R15 4.7K
Q14
GND
R16 100

NE/SE556-F,N • SA556-N
SE556C-N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA556, SE556C	+16	V
SE556	+18	V
Power dissipation	600	mW
Operating temperature range		
NE556	0 to +70	°C
SA556	-40 to +85	°C
SE556, SE556C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (Soldering, 60 sec)	+300	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE556			NE/SA556/SE556C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	$V_{CC} = 5V$ $R_L = \infty$		6	10		6	12	mA
	$V_{CC} = 15V$ $R_L = \infty$		20	24		20	30	mA
Timing error (monostable)	$R_A = 2k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, $R_B = 1k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		1.5			2.25		%
Drift with temperature	$V_{CC} = 15V$		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
	$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100mA$		2.0	2.25		2.0	3.2	V
	$I_{SINK} = 200mA$		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.2		0.25	0.3	V
	$I_{SINK} = 5mA$		0.05	0.15		0.15	0.25	V
Output voltage (high)	$V_{CC} = 15V$							
	$I_{SOURCE} = 200mA$		12.5			12.5		V
	$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5V$							
	$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			10			10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

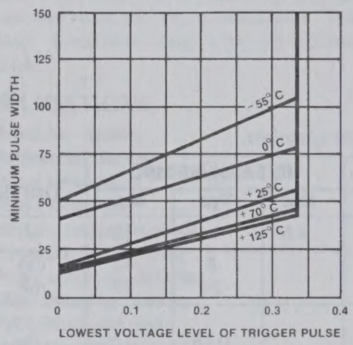
NOTES See following page

NOTES

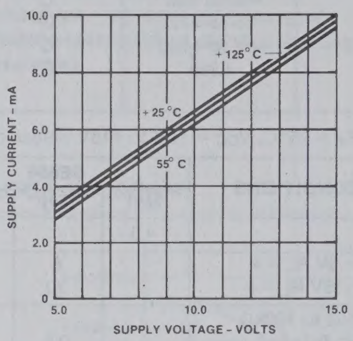
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 meg-ohms, and for 5V operation, the max. total R = 3.4 meg-ohms.
4. Matching charactristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.

TYPICAL PERFORMANCE CHARACTERISTICS

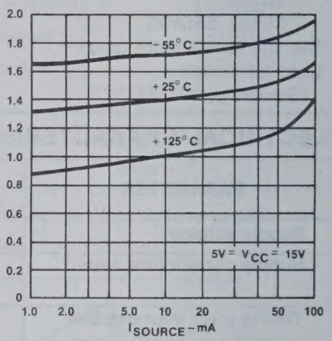
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



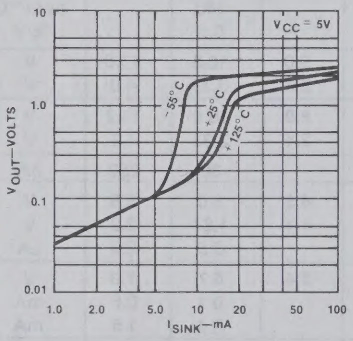
SUPPLY CURRENT vs SUPPLY VOLTAGE



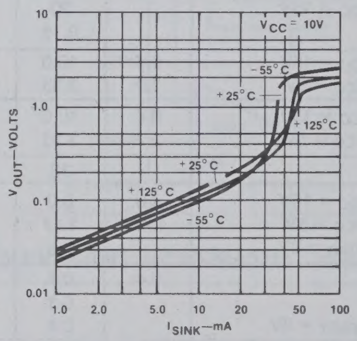
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



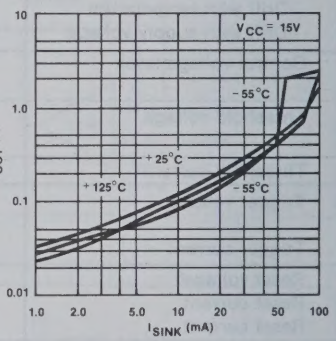
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



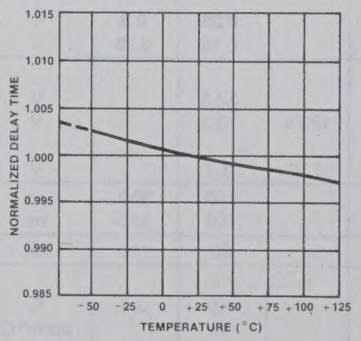
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



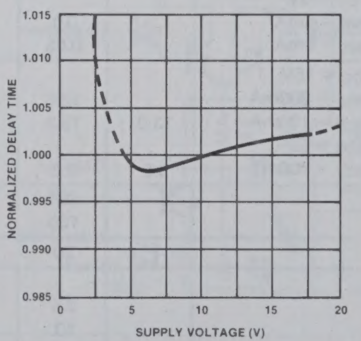
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



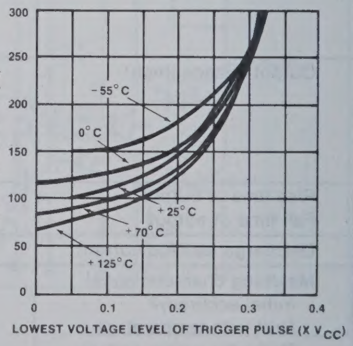
DELAY TIME vs TEMPERATURE



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



DESCRIPTION

The 556-1 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556-1 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

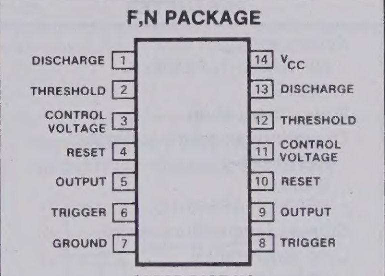
FEATURES

- **Turn off time less than 2μS**
- **Maximum operating frequency greater than 500kHz**
- **Timing from microseconds to hours**
- **Replaces two 555 timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**

APPLICATIONS

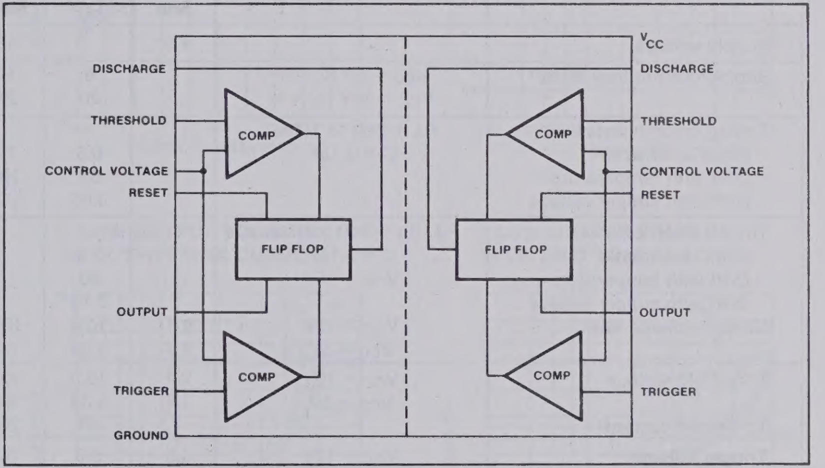
- **Precision timing**
- **Sequential timing**
- **Pulse shaping**
- **Pulse generator**
- **Missing pulse detector**
- **Tone burst generator**
- **Pulse width modulation**
- **Time delay generator**
- **Frequency division**
- **Industrial controls**
- **Pulse position modulation**
- **Appliance timing**
- **Traffic light control**
- **Touch tone encoder**

PIN CONFIGURATION

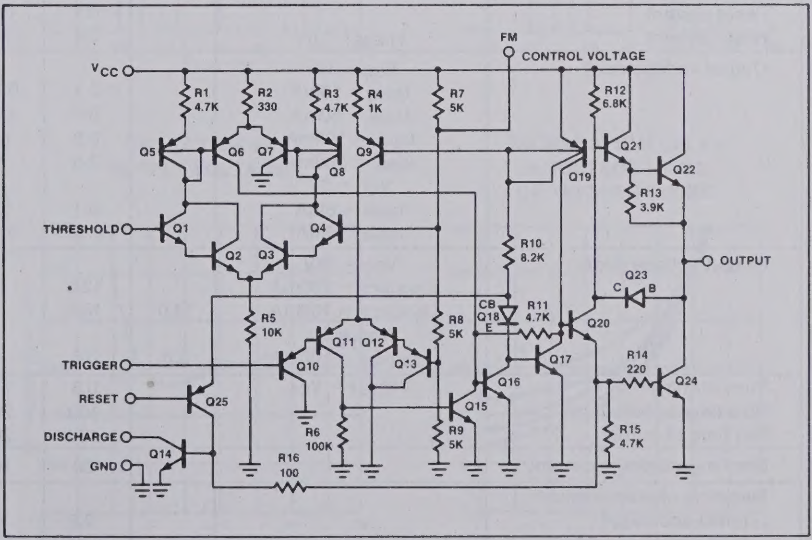

F,N PACKAGE
DISCHARGE 1
THRESHOLD 2
CONTROL VOLTAGE 3
RESET 4
OUTPUT 5
TRIGGER 6
GROUND 7
14 V_{CC}
13 DISCHARGE
12 THRESHOLD
11 CONTROL VOLTAGE
10 RESET
9 OUTPUT
8 TRIGGER

ORDER PART NO.
NE/SA/SE556-1F,N
SE556-1CF,CN

BLOCK DIAGRAM


V_{CC}
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER
GROUND
COMP
FLIP FLOP
COMP
COMP
FLIP FLOP
COMP
DISCHARGE
THRESHOLD
CONTROL VOLTAGE
RESET
OUTPUT
TRIGGER

EQUIVALENT SCHEMATIC (Shown for one circuit only)


FM
CONTROL VOLTAGE
V_{CC}
R1 4.7K
R2 330
R3 4.7K
R4 1K
R7 5K
R12 6.8K
Q5
Q6
Q7
Q8
Q9
Q19
Q21
Q22
R13 3.9K
THRESHOLD
Q1
Q2
Q3
Q4
R10 8.2K
OUTPUT
Q23
C
B
R5 10K
CB
Q18
E
R11 4.7K
Q20
R8 5K
Q11
Q12
Q13
Q17
R14 220
TRIGGER
Q10
Q16
Q24
RESET
Q25
Q15
DISCHARGE
R6 100K
R9 5K
R15 4.7K
Q14
GND
R16 100

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA556-1, SE556-1C	+16	V
SE556-1	+18	V
Power dissipation	1.20	W
Operating temperature range		
NE/SA556-1	0 to +70	°C
SA556-1	-40 to +85	°C
SE556-1, SE556-1C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE556-1			NE556-1/SE556-1C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	$V_{CC} = 5V$ $R_L = \infty$		6	10		6	12	mA
	$V_{CC} = 15V$ $R_L = \infty$		20	24		20	30	mA
Timing error (monostable)	$R_A = 2k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, $R_B = 1k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		1.5			2.25		%
Drift with temperature	$V_{CC} = 15V$		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
	$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100mA$		0.8	1.2		2.0	2.5	V
	$I_{SINK} = 200mA$		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.2		0.25	0.3	V
	$I_{SINK} = 5mA$		0.05	0.15		0.15	0.25	V
Output voltage (high)	$V_{CC} = 15V$							
	$I_{SOURCE} = 200mA$		12.5			12.5		V
	$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5V$							
	$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
Turn off time[6]	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			±10			±10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

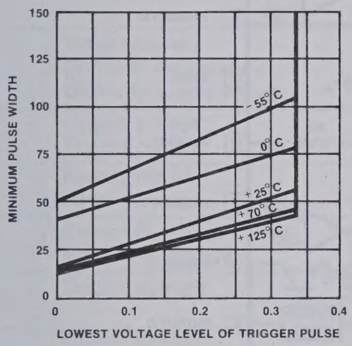
NOTES
See following page

NOTES

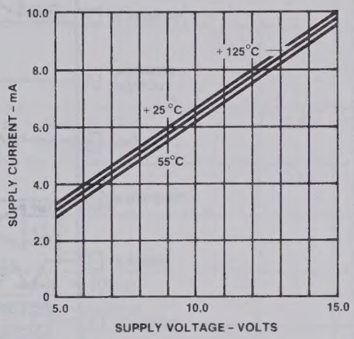
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 megohms, and for 5V operation, the max. total R = 3.4 megohms.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to 0.8 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL CHARACTERISTICS

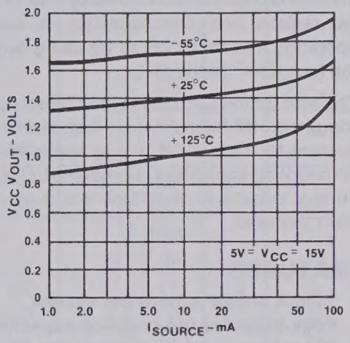
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



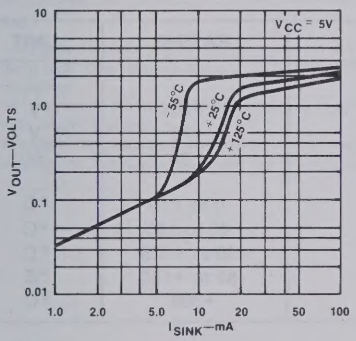
SUPPLY CURRENT vs SUPPLY VOLTAGE



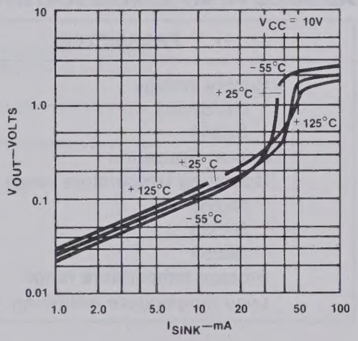
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



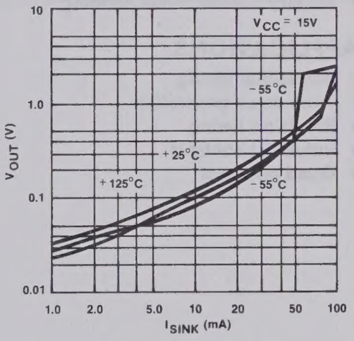
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



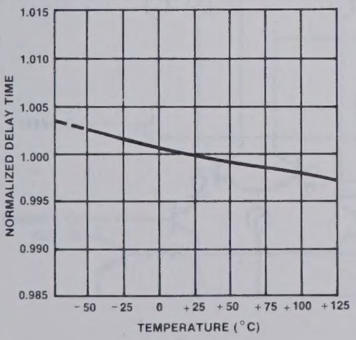
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



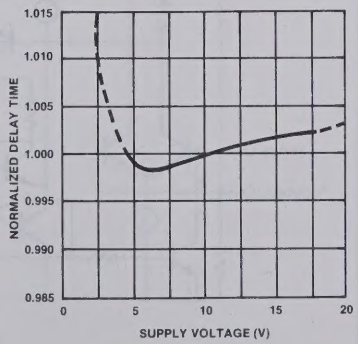
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



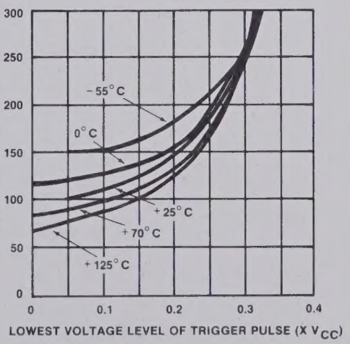
DELAY TIME vs TEMPERATURE



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

FEATURES

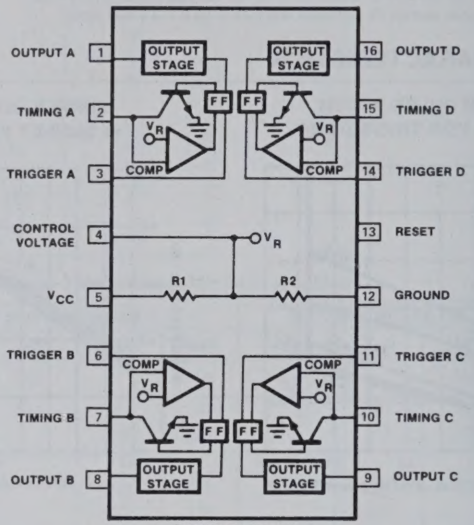
- **100mA output current per section**
- **Edge triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 18V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**
- **Military qualifications pending**

APPLICATIONS

- **Sequential timing**
- **Time delay generation**
- **Precision timing**
- **Industrial controls**
- **Quad one-shot**

PIN CONFIGURATION

F,N PACKAGE

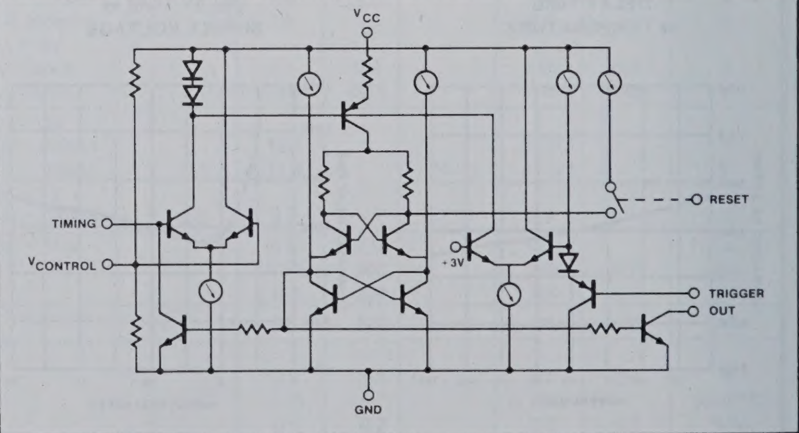

OUTPUT A 1
TIMING A 2
TRIGGER A 3
CONTROL VOLTAGE 4
V_{CC} 5
TRIGGER B 6
TIMING B 7
OUTPUT B 8
OUTPUT C 9
TIMING C 10
TRIGGER C 11
GROUND 12
RESET 13
TRIGGER D 14
TIMING D 15
OUTPUT D 16
OUTPUT STAGE
FF
COMP
V_R
R1
R2

ORDER PART NO.
NE/SA/SE558F NE/SA/SE558N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA558	+16	V
SE558	+18	V
Power dissipation	1.25	W
Operating temperature range		
NE558	0 to +70	°C
SA558	-40 to +85	°C
SE558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

558 EQUIVALENT CIRCUIT


V_{CC}
RESET
TIMING
$V_{CONTROL}$
+3V
TRIGGER
OUT
GND

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558			NE/SA558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current	V_{CC} = Reset = 15V		21	32		27	36	mA
Timing accuracy (T = RC)	R = 2kΩ to 100kΩ C = 1µF							
Initial accuracy			1.0	3		2		%
Drift with temperature			150			150		ppm/°C
Drift with supply voltage			0.1			0.1		%/V
Trigger voltage[1]	V_{CC} = 15V	0.8	1.5	2.4	0.8	1.5	2.4	V
Trigger current	Trigger = 0V		5	30		5	100	µA
Reset voltage[2]		0.8	1.5	2.4	0.8	1.5	2.4	V
Reset current	Reset		50	300		50		µA
Threshold voltage			0.63			0.63		xV_{CC}
Threshold leakage			15			15		nA
Output voltage[3]	I_L = 10mA		0.1	0.2		0.1	0.4	V
	I_L = 100mA		0.7	1.5		1.0	2.0	V
Output leakage			10			10		nA
Propagation delay			1.0			1.0		µs
Risetime of output	I_L = 100mA		100			100		ns
Falltime of output	I_L = 100mA		100			100		ns

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.

SECTION 5
COMPARATORS

Section 5—COMPARATORS

LM111/211/311 Voltage Comparator 191
LM119/219/319 Dual Voltage Comparator 194
LM139/239/339 Quad Voltage Comparator 199
LM193/A/293/A/393/A Low Power Dual Voltage Comparator 204
LM2901 Quad Voltage Comparator 199
LM2903 Low Power Dual Voltage Comparator 204
MC3302 Quad Voltage Comparator 199
NE/SE521 High Speed Dual Differential Comparator/Sense Amp 207
NE/SE522 High Speed Dual Differential Comparator/Sense Amp 211
NE/SE527 Voltage Comparator 215
NE/SE529 Voltage Comparator 219

COMPARATORS SELECTION GUIDE

DEVICE	COMPLEXITY	TEMP. RANGE*	MAX.INP. OFFSET VOLT. (mV)	MAX.INP. CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP.) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE		OUTPUT STRUCTURE	VOLTAGE GAIN (TYP.) V/mV	TTL FANOUT	MAX.DIFF. INP. VOLTAGE V	PACKAGES
				Bias (μA)	Offset (μA)				VOL max (V)	VOH min (V)					
LM111[1]	Single	M	4.00	0.15	0.02	± 15	200	± 14	0.4		O.C.	200	5	± 30	F,T
LM211	Single	E	4.00	0.15	0.02	to	200	± 14	0.4		O.C.	200	5	± 30	F,N,T
LM311	Single	I	10.0	0.30	0.07	+5 and GND	200	± 14	0.4		O.C.	200	5	± 30	F,N,T
NE527[2]	Single	I	10.0	4.00	1.00	± 5 to ± 15	16	± 6	0.5	2.7	TTL		5	± 5	F,K,N
SE527	Single	M	6.00	4.00	1.00	and GND	16	± 6	0.5	2.5	TTL		5	± 5	F,K
NE529[2]	Single	I	10.0	50.0	15.0	± 5 to ± 15	12	± 6	0.5	2.7	TTL		5	± 5	F,K,N
SE529	Single	M	6.00	36.0	9.00	and GND	12	± 6	0.5	2.5	TTL		5	± 5	F,K
LM119[3]	Dual	M	7.00	1.00	0.10	± 15	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM219	Dual	E	7.00	1.00	0.10	to	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM319	Dual	I	10.0	1.20	0.30	± 5 and GND	80	± 13	0.6		O.C.	40	2	± 5	F,K,N
LM193[3]	Dual	M	9.00	0.30	0.10	± 1 to ± 18	1300	0 to VS −2	0.7		O.C.	200	2	36	T
LM293	Dual	E	9.00	0.40	0.15	or	1300	0 to VS −2	0.7		O.C.	200	2	36	N,T
LM393	Dual	I	9.00	0.40	0.15	+2 to +36 GND	1300	0 to VS −2	0.7		O.C.	200	2	36	N,T
LM2903	Dual	E	15.0	0.50	0.20		1300	0 to VS −2	0.7		O.C.	100	2	36	N,T
NE521[4]	Dual	I	10.0	40.0	12.0	+5, −5, GND	7	± 3	0.5	2.7	TTL		12	± 6	F,N
NE522	Dual	I	10.0	40.0	12.0	+5, −5, GND	9	± 3	0.5		O.C.		12	± 6	F,N
LM139[3]	Quad	M	9.00	0.30	0.10		1300	0 to VS −2	0.7		O.C.	200	2	36	F,N
LM239	Quad	E	9.00	0.40	0.15	± 1 to ± 18 or	1300	0 to VS −2	0.7		O.C.	200	2	36	F,N
LM339	Quad	I	9.00	0.40	0.15	+2 to +36	1300	0 to VS −2	0.7		O.C.	200	2	36	F,N
LM2901	Quad	E	15.0	0.50	0.20		1300	0 to VS −2	0.7		O.C.	100	2	36	N
MC3302[3]	Quad	E	40.0	1.00	0.20	+2 to +28 GND	2000	0 to VS −2	0.4		O.C.	30	2	28	N

*Temperature Range
E = Extended
I = Industrial
M = Military

NOTES
1. With strobe; will work from single supply
2. Complementary output gates with individual strobes
3. Will operate from single or dual supplies
4. Ultra high speed

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

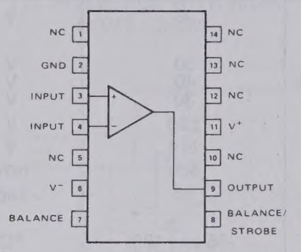
Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the μA710 (200ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

FEATURES

- **Operates from single 5V supply**
- **Maximum input bias current: 150nA (LM311 - 250nA)**
- **Maximum offset current: 20nA (LM311 - 50nA)**
- **Differential input voltage range: ±30V**
- **Power consumption: 135mW at ±15V**
- **High sensitivity—200V/mV**
- **Military qualification pending**

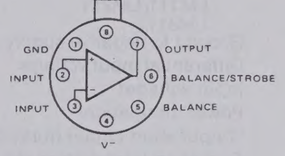
PIN CONFIGURATIONS

F,N-14 PACKAGE


NC 1
GND 2
INPUT 3
INPUT 4
NC 5
V⁻ 6
BALANCE 7
14 NC
13 NC
12 NC
11 V⁺
10 NC
9 OUTPUT
8 BALANCE/STROBE
+
−

ORDER PART NO.
LM111F/LM211F/LM211N-14
LM311F/LM311N-14

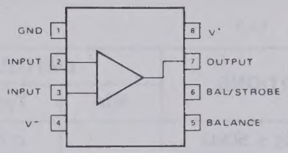
H PACKAGE*


V⁺
8
GND 1
7 OUTPUT
INPUT 2
6 BALANCE/STROBE
INPUT 3
5 BALANCE
4
V⁻

ORDER PART NO.
LM111H/LM211H/LM311H

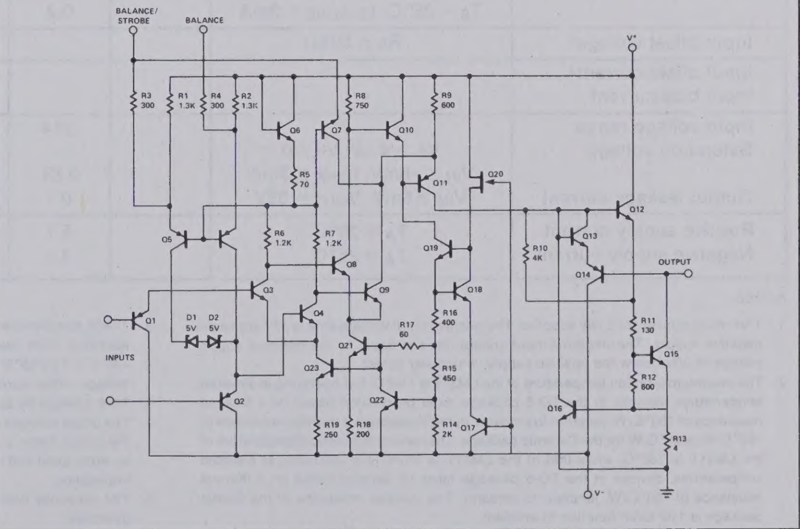
*Metal cans (H) not recommended for new designs

N PACKAGE


GND 1
INPUT 2
INPUT 3
V⁻ 4
8 V⁺
7 OUTPUT
6 BAL/STROBE
5 BALANCE

ORDER PART NO.
LM211N/LM311N
LM311D

EQUIVALENT SCHEMATIC


BALANCE/STROBE
BALANCE
V⁺
R3 300
R1 1.3K
R4 300
R2 1.3K
R8 750
R9 600
Q6
Q7
Q10
R5 70
Q11
Q20
Q12
Q5
R6 1.2K
R7 1.2K
Q8
Q13
R10 4K
Q19
Q14
OUTPUT
Q3
Q9
Q18
Q1
D1 5V
D2 5V
Q4
R17 60
R16 400
R11 130
Q21
Q15
INPUTS
Q23
R15 450
R12 800
Q2
Q22
Q16
R19 250
R18 200
R14 2K
Q17
R13 4
V⁻

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage:		
LM111/LM211	50	V
LM311	40	V
Ground to negative supply voltage	30	V
Differential input voltage	±30	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	sec
Operating temperature range		
LM111	-55 to +125	°C
LM211	-25 to +85	°C
LM311	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS [1,2,3]

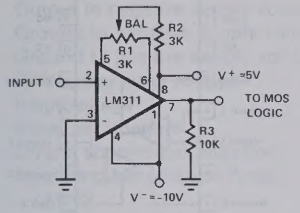
PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[4]	$T_A = 25^\circ C$, $R_S \le 50k\Omega$		0.7	3.0		2.0	7.5	mV
Input offset current[4]	$T_A = 25^\circ C$		4.0	10		6.0	50	nA
Input bias current	$T_A = 25^\circ C$		60	100		100	250	nA
Voltage gain	$T_A = 25^\circ C$		200			200		V/mV
Response time[5]	$T_A = 25^\circ C$		200			200		ns
Saturation voltage	$V_{IN} \le -5mV$, $I_{OUT} = 50mA$ $T_A = 25^\circ C$		0.75	1.5		0.75	1.5	V
Strobe on current	$T_A = 25^\circ C$		3.0			3.0		mA
Output leakage current	$V_{IN} \ge 5mV$, $V_{OUT} = 35V$ $T_A = 25^\circ C$, $I_{STROBE} = 3mA$		0.2	10		0.2	50	nA
Input offset voltage[4]	$R_S \le 50k\Omega$			4.0			10	mV
Input offset current[4]				20			70	nA
Input bias current				150			300	nA
Input voltage range			±14			±14		V
Saturation voltage	$V+ \ge 4.5V$, $V- = 0$ $V_{IN} \le -6mV$, $I_{SINK} \le 8mA$		0.23	0.4		0.23	0.4	V
Output leakage current	$V_{IN} \ge 5mV$, $V_{OUT} = 35V$		0.1	0.5				μA
Positive supply current	$T_A = 25^\circ C$		5.1	6.0		5.1	7.5	mA
Negative supply current	$T_A = 25^\circ C$		4.1	5.0		4.1	5.0	mA

NOTES

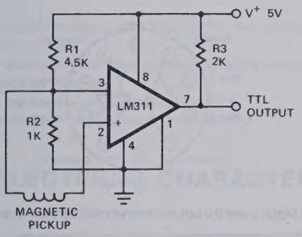
1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, in the N package, a thermal resistance of 162°C/W, and °C/W for the Ceramic package. The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient. The thermal resistance of the Cerdip package is 110°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm 15V$ and $0^\circ C < T_A < 70^\circ C$ unless otherwise specified. With the LM211, however, all temperature specifications are limited to $-25^\circ C \le T_A \le 85^\circ C$ and for the LM111 is limited to $-55^\circ C < T_A < 125^\circ C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

TYPICAL APPLICATIONS

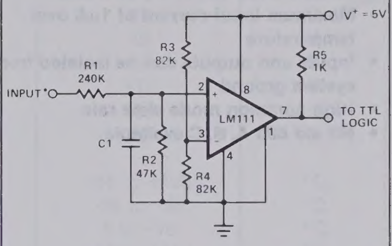
ZERO CROSSING DETECTOR DRIVING MOS LOGIC


BAL
R2
3K
R1
3K
5
6
INPUT
2
+
LM311
-
3
4
8
7
1
V+ =5V
TO MOS
LOGIC
R3
10K
V− =-10V

DETECTOR FOR MAGNETIC TRANSDUCER


V+ 5V
R1
4.5K
R3
2K
3
-
8
LM311
7
TTL
OUTPUT
R2
1K
+
2
1
4
MAGNETIC
PICKUP

TTL INTERFACE WITH HIGH LEVEL LOGIC


V+ = 5V
R3
82K
R5
1K
R1
240K
INPUT*
2
+
8
LM111
3
-
7
1
4
TO TTL
LOGIC
C1
R2
47K
R4
82K

*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

DUAL VOLTAGE COMPARATOR — LM119/219/319

LM119/219/319-F,H,N
LM319-D

DESCRIPTION

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μA710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μA711.

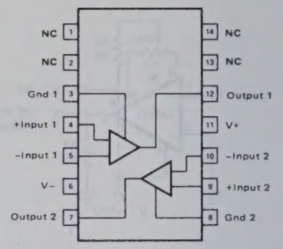
The LM119 is specified from -55°C to +125°C, the LM219 is specified from -25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

FEATURES

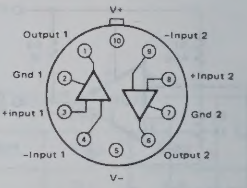
- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Minimum fan-out of 3 (each side)**
- **Maximum input current of 1μA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common mode slew rate**
- **Mil std 883 A, B, C available**

PIN CONFIGURATIONS

D,F,N PACKAGE

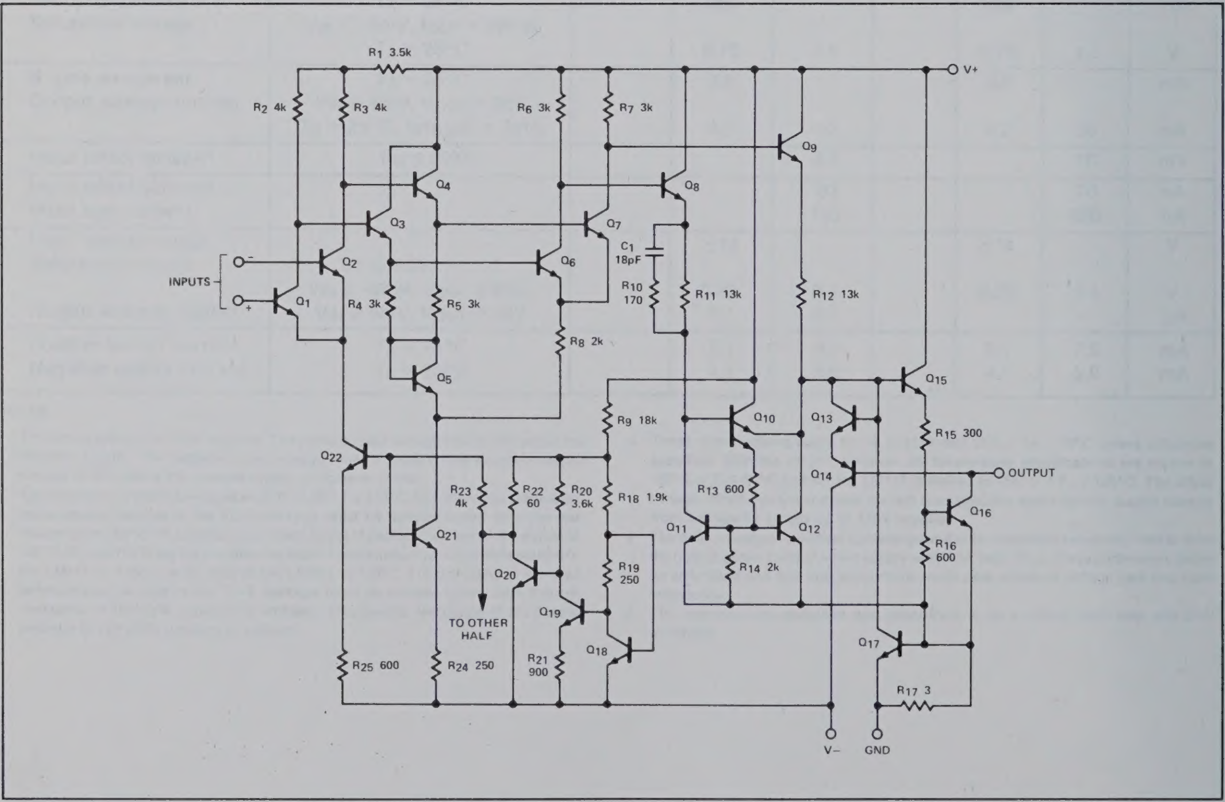

NC 1
NC 2
Gnd 1 3
+Input 1 4
−Input 1 5
V− 6
Output 2 7
Gnd 2 8
+Input 2 9
−Input 2 10
V+ 11
Output 1 12
NC 13
NC 14

H PACKAGE*


V+
10
Output 1
1
−Input 2
9
Gnd 1
2
+Input 2
8
+Input 1
3
Gnd 2
7
−Input 1
4
Output 2
6
5
V−

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC


R1 3.5k
V+
R2 4k
R3 4k
R6 3k
R7 3k
Q9
Q4
Q8
Q3
Q7
C1 18pF
Q2
Q6
INPUTS
−
+
Q1
R4 3k
R5 3k
R10 170
R11 13k
R12 13k
R8 2k
Q5
Q15
R9 18k
Q10
Q13
R15 300
Q22
Q14
OUTPUT
R23 4k
R22 60
R20 3.6k
R18 1.9k
R13 600
Q16
Q21
Q11
Q12
R16 600
R19 250
R14 2k
Q20
Q19
TO OTHER HALF
Q18
Q17
R25 600
R24 250
R21 900
R17 3
V−
GND

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage	36	V
Ground to negative supply voltage	25	V
Ground to positive supply voltage	18	V
Differential input voltage	±5	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	s
Operating temperature range		
LM119	-55 to +125	°C
LM219	-25 to +85	°C
LM319	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NOTES
1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. The absolute maximum junction temperature is 150°C. Device dissipation must be derated as follows:
   N/K package—150°C/watt above 75°C
   F package —110°C/watt above 95°C

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, for LM119, $-55°C \le T_A \le 125°C$; LM219, $-25°C \le T_A \le 85°C$; LM319, $0°C \le T_A \le 70°C$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LM119/219			LM319			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[1,2]	$R_S \le 5K\Omega$, $T_A = 25°C$		0.7	4.0		2.0	8.0	mV
		Over temp.			7			10	mV
I_{OS}	Input offset current[1,2]	$T_A = 25°C$		30	75		80	200	nA
		Over temp.			100			300	nA
I_B	Input bias current[1]	$T_A = 25°C$		150	500		250	1000	nA
		Over temp.			1000			1200	nA
A_V	Voltage gain	$T_A = 25°C$	10	40		8	40		V/mV
V_{OL}	Saturation voltage	$V_{IN}=5mV$, $I_{OUT}=25mA$, $T_A=25°C$		0.75	1.5				V
		$V_{IN}=10mV$, $I_{OUT}=25mA$, $T_A=25°C$					0.75	1.5	V
		$V^+ \ge 4.5V$, $V^- = 0$							
		$V_{IN} = 6mV$, $I_{OUT} = 3.2mA$							
		$T_A \ge 0°C$		0.23	0.4				V
		$T_A \le 0°C$			0.6				
		$V_{IN} = 10mV$, $I_{OUT} = 3.2mA$					0.3	0.4	V
I_{OH}	Output leakage current	$V^- = 0V$, $V_{IN} = 5mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$		0.2	2				µA
		Over temp.		1	10				µA
		$V^- = 0V$, $V_{IN} = 10mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$					0.2	10	µA
V_{IN}	Input voltage range	$V_S = \pm15V$		±13			±13		V
		$V^+ = 5V$, $V^- = 0V$	1		3	1		3	V
V_{ID}	Differential input voltage				±5			±5	V
I^+	Positive supply current	$V^+ = 5V$, $V^- = 0V$, $T_A = 25°C$		4.3			4.3		mA
I^+	Positive supply current	$V_S = \pm15V$, $T_A = 25°C$		8.0	11.5		8.0	12.5	mA
I^-	Negative supply current	$V_S = \pm15V$, $T_A = 25°C$		3.0	4.5		3.0	5.0	mA

NOTES
1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of $V_S = \pm15V$ down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1 volt of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

AC ELECTRICAL CHARACTERISTICS

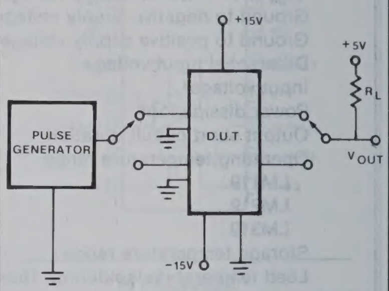
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Response time*	$V_S = \pm15V$, $T_A = 25°C$ $R_L = 500\Omega$ (see test figure)		80		ns

*NOTE

The response time specified is for a 100mV step with 5mV overdrive.

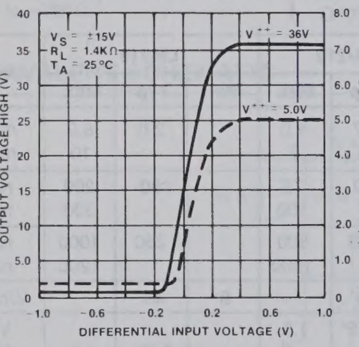
TEST CIRCUIT

RESPONSE TIME MEASUREMENT

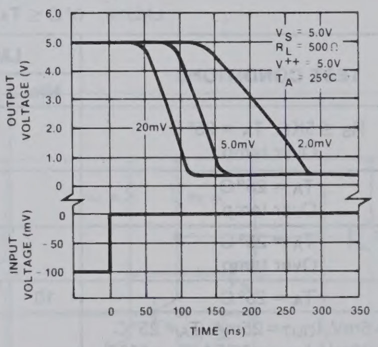


TYPICAL PERFORMANCE CHARACTERISTICS

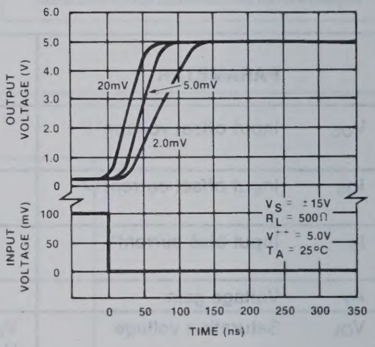
TRANSFER FUNCTION



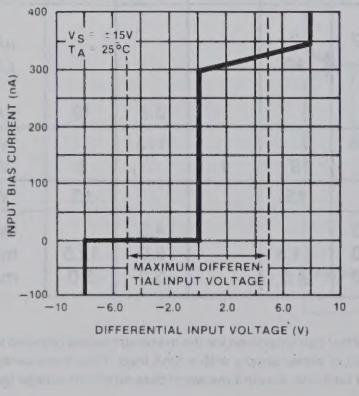
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



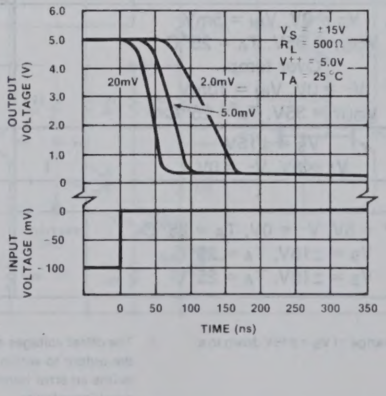
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



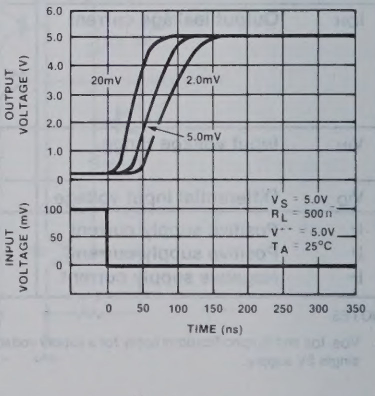
INPUT CHARACTERISTICS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

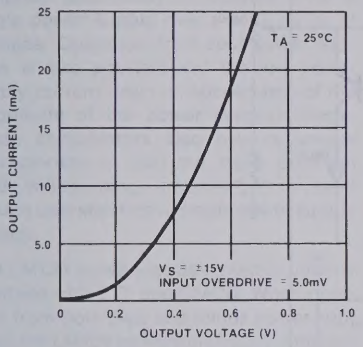


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

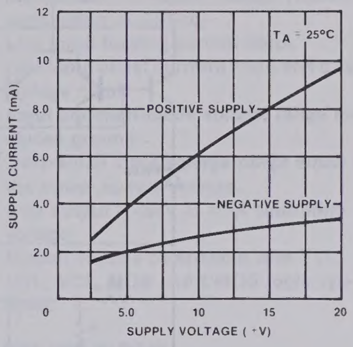


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

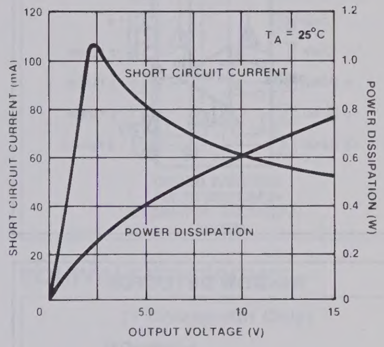
OUTPUT SATURATION VOLTAGE



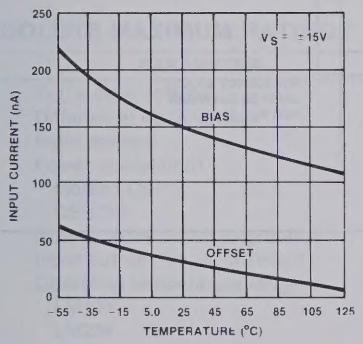
SUPPLY CURRENT



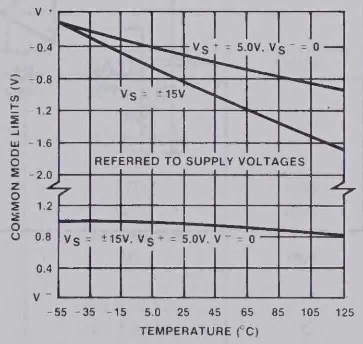
OUTPUT LIMITING CHARACTERISTICS



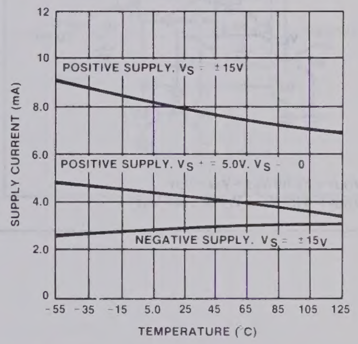
INPUT CURRENTS (LM119/219)



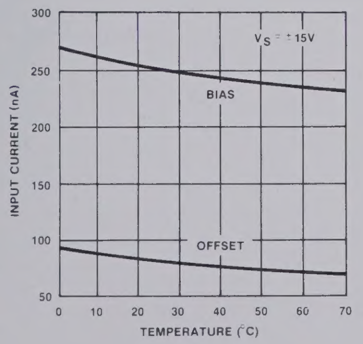
COMMON MODE LIMITS (LM119/219)



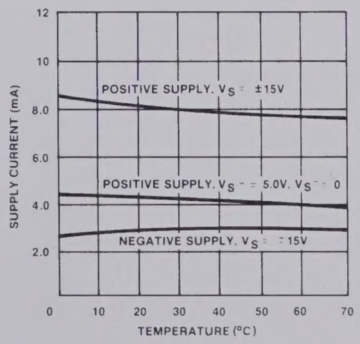
SUPPLY CURRENT (LM119/219)



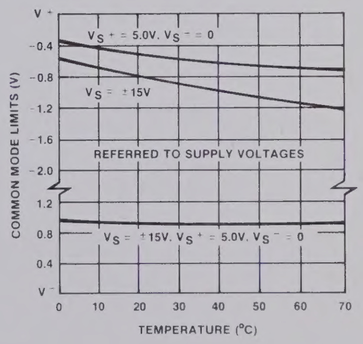
INPUT CURRENTS (LM319)



SUPPLY CURRENTS (LM319)

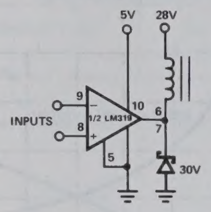


COMMON MODE LIMITS (LM319)

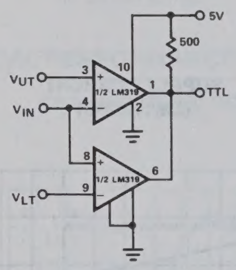


TYPICAL APPLICATIONS

RELAY DRIVER

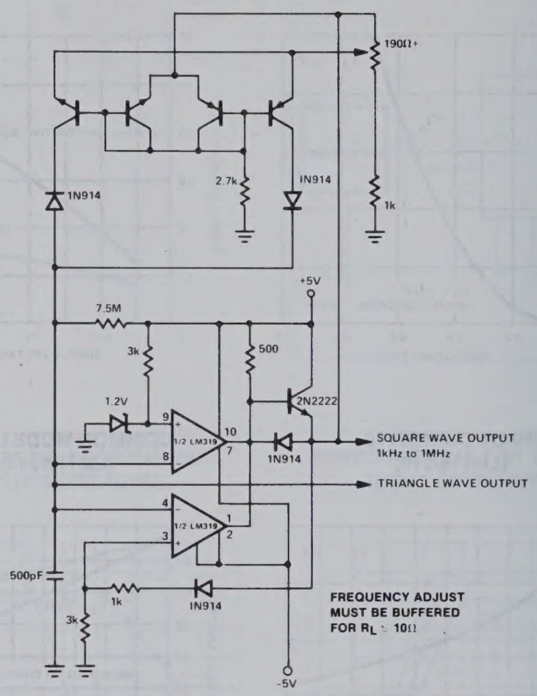

5V
28V
9
INPUTS
8
10
1/2 LM319
6
7
5
30V

WINDOW DETECTOR


5V
500
3
10
1
VUT
1/2 LM319
TTL
VIN
4
2
8
6
1/2 LM319
9
VLT

$V_{OUT} = 5V$ for $V_{LT} < V_{IN} < V_{UT}$
$V_{OUT} = 0$ for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

WIDE RANGE VARIABLE OSCILLATOR


190Ω+
1N914
2.7k
IN914
1k
+5V
7.5M
3k
500
1.2V
9
10
1/2 LM319
8
7
2N2222
IN914
SQUARE WAVE OUTPUT
1kHz to 1MHz
TRIANGLE WAVE OUTPUT
4
1/2 LM319
1
3
2
500pF
1k
IN914
3k
-5V

FREQUENCY ADJUST
MUST BE BUFFERED
FOR $R_L \leq 10\Omega$

QUAD VOLTAGE COMPARATOR

LM139/239/339 MC3302/LM2901

LM139/239/339/2901/MC3302-F,N
LM339-D

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset currrent ±5nA and offset voltage ±2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

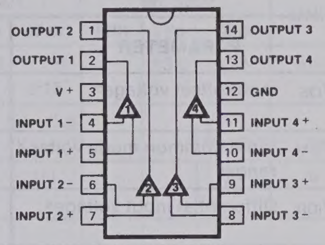
- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	
Differential input voltage	36	
Input voltage	-0.3 to +36	
Power dissipation[1]		
Molded DIP	570	mW
CERDIP	900	mW
Output short circuit to ground[2]	Continuous	
Input current ($V_{IN} < -0.3$Vdc)[3]	50	mA
Operating temperature range		
LM139	-55 to +125	°C
LM239	-25 to +85	°C
LM339	0 to +70	°C
LM2901/MC3302	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

PIN CONFIGURATION

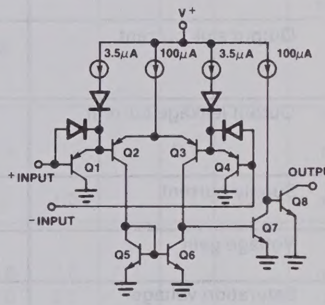
D,F,N PACKAGE



ORDER PART NO.
LM139/239/339F,N
LM2901F,N MC3302F,N
LM339D

EQUIVALENT CIRCUIT

(1 Comparator Only)



LM139/239/339/2901/MC3302-F,N
LM339-D

DC ELECTRICAL CHARACTERISTICS

$V+ = 5\text{Vdc}$, LM139: $-55°C \leq T_A \leq 125°C$ unless otherwise specified
LM239: $-25°C \leq T_A \leq 85°C$ unless otherwise specified
LM339: $0°C \leq T_A \leq 70°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS	LM139			LM239/339			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25°C$ Over temp.		±2.0	±5.0 9.0		±2.0	±5.0 9.0	mV
V_{CM}	Input common mode voltage range[6]	$T_A = 25°C$ Over temp.	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN's} \geq 0\text{Vdc}$ (or V- if used)			V+			V+	V
I_B	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1\text{Vdc}$, $V_{IN(+)} = 0$, $V_O \leq 1.5\text{Vdc}$, $T_A = 25°C$	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1\text{Vdc}$, $V_{IN(-)} = 0$ $V_O = 5\text{Vdc}$, $T_A = 25°C$ $V_O = 30\text{Vdc}$, over temp.		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on all comparators, $T_A = 25°C$		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15\text{Vdc}$ $T_A = 25°C$	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1\text{Vdc}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\text{mA}$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4\text{Vdc}$, $V_{RL} = 5\text{Vdc}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
T_R	Response time[8]	$V_{RL} = 5\text{Vdc}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

LM139/239/339/2901/MC3302-F,N
LM339-D

DC ELECTRICAL CHARACTERISTICS

V+ = 15Vdc, MC3302
LM2901/MC3302: $-40°C \leq T_A \leq 85°C$ unless otherwise specified

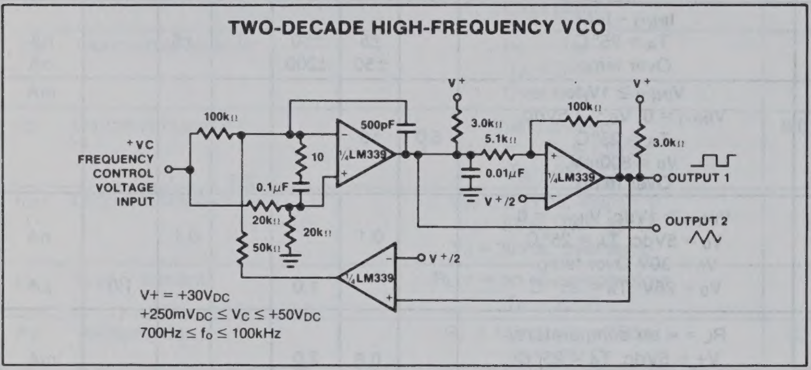
PARAMETER		TEST CONDITIONS	LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV
V_{CM}	Input common mode voltage range[6]	$T_A = 25°C$ Over temp.	0 0		V+−1.5 V+−2.0			V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[4]	Keep all V_{IN}'s ≥ 0Vdc (or V− if need)			V+			V+	V
I_B	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25 200	250 500		25	500 1000	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±5 ±50	±50 ±200		±5		nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1$Vdc, $V_{IN(+)} = 0$, $V_0 \leq 1.5$Vdc, $T_A = 25°C$ $V_0 = 800$mV, Over temp.	6.0	16		2.0			mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1$Vdc, $V_{IN(-)} = 0$ $V_0 = 5$Vdc, $T_A = 25°C$ $V_0 = 30$V Over temp. $V_0 = 28$V $T_A = 25°C$		0.1	1.0		0.1	1.0	nA µA
I_{CC}	Supply current	$R_L = \infty$ on comparators, V+ = 5Vdc, $T_A = 25°C$ V+ = 30V, $T_A = 25°C$ V+ = 5 to 28 Vdc, $T_A = 25°C$		0.8 1.0	2.0 2.5		0.8	2.0	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, V+ = 15Vdc $T_A = 25°C$	25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1$Vdc, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$mA $T_A = 25°C$ Over temp. $I_{SINK} = 2$mA, V+ = 5V to 28V, $T_A = 25°C$		400	400 700		150	400	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4$Vdc, $V_{RL} = 5$Vdc, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
T_R	Response time[8]	$V_{RL} = 5$Vdc, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		µs

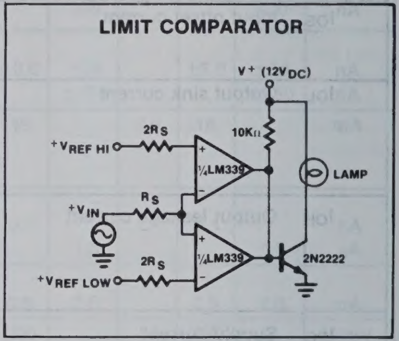
LM139/239/339/2901/MC3302-F,N
LM339-D

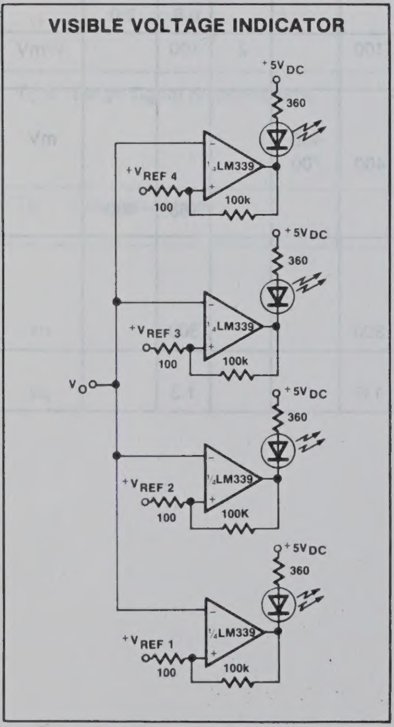
NOTES

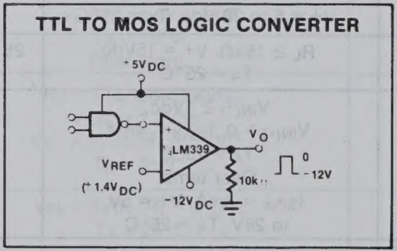
1. For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a 150°C maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.

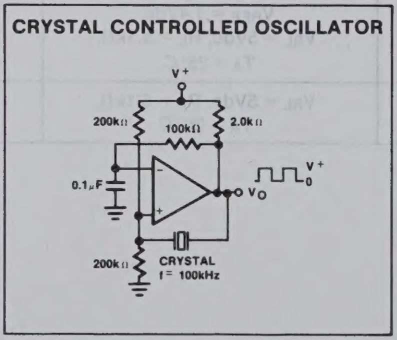
TYPICAL APPLICATIONS


TWO-DECADE HIGH-FREQUENCY VCO
+VC FREQUENCY CONTROL VOLTAGE INPUT
100kΩ
10
0.1µF
20kΩ
50kΩ
20kΩ
500pF
¼LM339
V+
3.0kΩ
5.1kΩ
0.01µF
V+/2
100kΩ
V+
3.0kΩ
¼LM339
OUTPUT 1
OUTPUT 2
V+/2
¼LM339
V+ = +30VDC
+250mVDC ≤ VC ≤ +50VDC
700Hz ≤ fo ≤ 100kHz


LIMIT COMPARATOR
V+ (12VDC)
+VREF HI
2RS
10KΩ
¼LM339
LAMP
+VIN
RS
¼LM339
2N2222
2RS
+VREF LOW

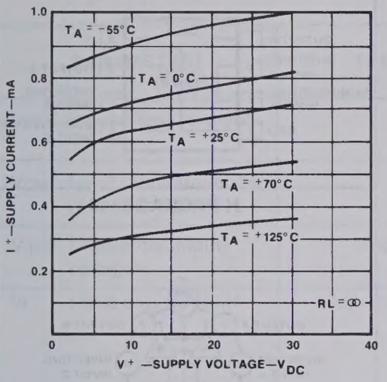

VISIBLE VOLTAGE INDICATOR
+5VDC
360
¼LM339
+VREF 4
100
100k
+5VDC
360
¼LM339
+VREF 3
100
100k
VO
+5VDC
360
¼LM339
+VREF 2
100
100K
+5VDC
360
¼LM339
+VREF 1
100
100k


TTL TO MOS LOGIC CONVERTER
+5VDC
¼LM339
VO
VREF
(+1.4VDC)
-12VDC
10kΩ
0
-12V

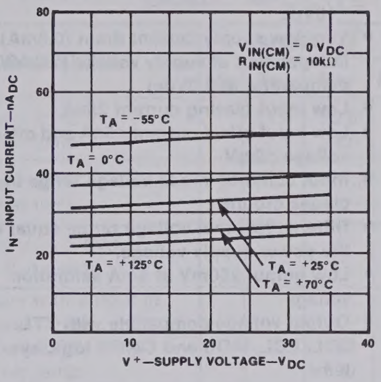

CRYSTAL CONTROLLED OSCILLATOR
V+
200kΩ
100kΩ
2.0kΩ
0.1µF
VO
V+
0
200kΩ
CRYSTAL
f = 100kHz

TYPICAL PERFORMANCE CHARACTERISTICS

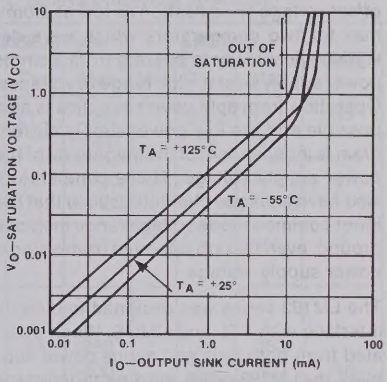
SUPPLY CURRENT



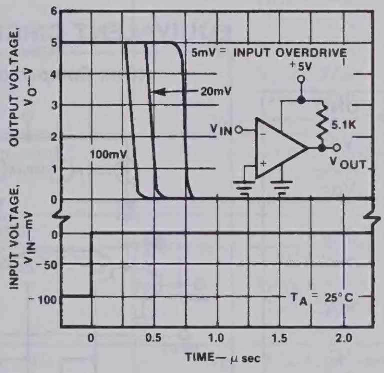
INPUT CURRENT



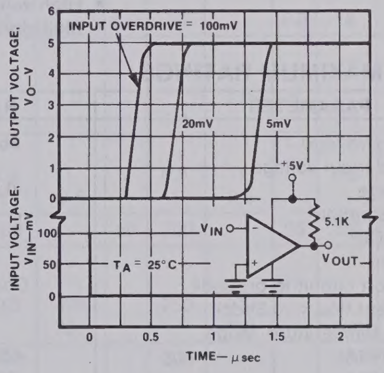
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—POSITIVE TRANSITION



LOW POWER DUAL VOLTAGE COMPARATOR

LM193/293/393 LM193A/293A/393A/LM2903

LM193/293/393/193A/293A/393A/2903-N,FE,H

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

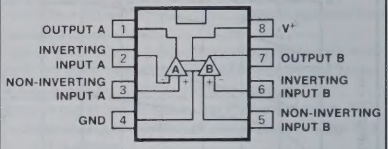
- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset current ±5nA and offset voltage ±2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

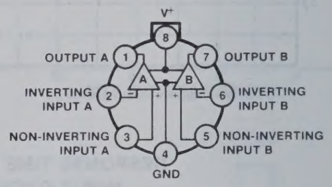
- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATIONS

N,FE PACKAGE


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
GND 4
8 V+
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B

H PACKAGE*


V+
8
OUTPUT A 1
7 OUTPUT B
INVERTING INPUT A 2
6 INVERTING INPUT B
NON-INVERTING INPUT A 3
5 NON-INVERTING INPUT B
4
GND
A
B

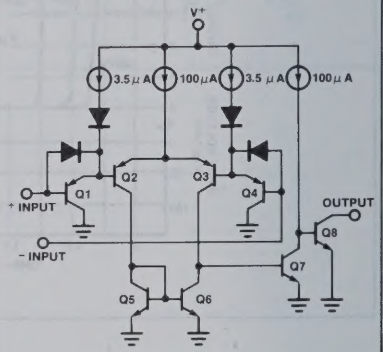
*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	Vdc
Differential input voltage	36	Vdc
Input voltage	-0.3 to +36	Vdc
Power dissipation[1]		
Molded DIP	570	mW
Metal can	900	mW
Output short circuit to ground[2]	Continuous	
Input current ($V_{IN} < -0.3$Vdc)[3]	50	mA
Operating temperature range		
LM193/193A	-55 to +125	°C
LM293/293A	-25 to +85	°C
LM393/393A	0 to +70	°C
LM2903	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT

(One Comparator Only)


V+
3.5μA
100μA
3.5 μA
100μ A
Q1
Q2
Q3
Q4
+ INPUT
− INPUT
OUTPUT
Q8
Q7
Q5
Q6

LM193/293/393/193A/293A/393A/2903-N,FE,H

DC ELECTRICAL CHARACTERISTICS

V+ = 5Vdc, LM193/193A: $-55^\circ C \le T_A \le +125^\circ C$ unless otherwise specified.
LM293/293A: $-25^\circ C \le T_A \le +85^\circ C$ unless otherwise specified.
LM393/393A: $0^\circ C \le T_A \le +70^\circ C$ unless otherwise specified.
LM2903: $-40^\circ C \le T_A \le +85^\circ C$ unless otherwise specified.[7]

PARAMETER		TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25^\circ C$ Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common mode voltage range[6,10]	$T_A = 25^\circ C$ Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN's} \ge 0Vdc$ (or V− if need)			V+			V+			V+	V
I_B	Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25^\circ C$ Over temp.		25	100 300		25	250 400		25 200	250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25^\circ C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $V_0 \le 1.5Vdc$, $T_A = 25^\circ C$	6.0	16		6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \ge 1Vdc$, $V_{IN(-)} = 0$ $V_0 = 30Vdc$ Over temp. $V_0 = 5Vdc$, $T_A = 25^\circ C$		0.1	1.0		0.1	1.0		0.1	1.0	μA na
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_A = 25^\circ C$ V+ = 30V, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA
A_V	Voltage gain	$R_L \ge 15k\Omega$, V+ = 15Vdc, $T_A = 25^\circ C$	50	200		50	200		25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \le 4mA$ $T_A = 25^\circ C$ Over temp.		250	400 700		250	400 700		400	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		300			300			300		ns
T_R	Response time[9]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		1.3			1.3			1.3		μs

DC ELECTRICAL CHARACTERISTICS (Cont'd)

V+ = 5Vdc, LM193/193A: -55°C ≤ T_A ≤ +125°C unless otherwise specified.
LM293/293A: -25°C ≤ T_A ≤ +85°C unless otherwise specified.
LM393/393A: 0°C ≤ T_A ≤ +70°C unless otherwise specified.
LM2903: -40°C ≤ T_A ≤ +85°C unless otherwise specified.[7]

PARAMETER		TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	T_A = 25°C Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV
V_{CM}	Input common mode voltage range[6,10]	T_A = 25°C Over temp.	0 0		V±-1.5 V±-2.0	0 0		V±-1.5 V±-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN's}$ ≥ 0Vdc (or V- if need)			V+			V+	V
I_B	Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1$Vdc, $V_{IN(+)} = 0$, $V_O \leq 1.5$Vdc, T_A = 25°C	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1$Vdc, $V_{IN(-)} = 0$ V_O = 5Vdc, T_A = 25°C V_O = 30Vdc, over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators T_A = 25°C V+ = 30V, over temp.		0.8	1 2.5		0.8	1 2.5	mA
A_V	Voltage gain	$R_L \geq 15K\Omega$, V+ = 15Vdc	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1$Vdc, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$mA T_A = 25°C Over temp.		250	400 700		250	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4Vdc, V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		300			300		ns
T_R	Response time[9]	V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		1.3			1.3		μs

NOTES

1. For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small ($P_D \leq 100$mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong 1.4$Vdc, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. With the LM293/293A, all temperature specifications are limited to -25°C ≤ T_A ≤ +85°C and the LM393/393A, all temperature specifications are limited to 0°C ≤ T_A ≤ +70°C. The LM2903 is limited to -40°C ≤ T_A ≤85°C.
8. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
9. The response time specified is for a 100mV input step with a 5mV overdrive.
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max., and a limiting resistor should be used on all inputs that might exceed the positive supply.

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE521

NE521-F,N
SE521-F

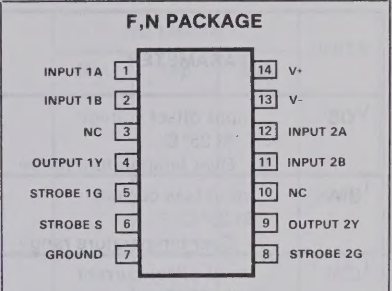
FEATURES

- 12ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

PIN CONFIGURATION

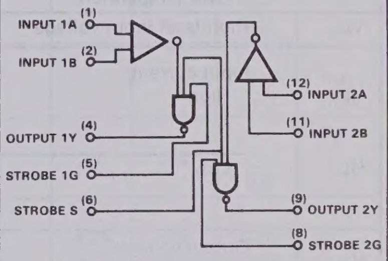

F,N PACKAGE
INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V+
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G

Order Part No.
NE521 F,N
SE521 F

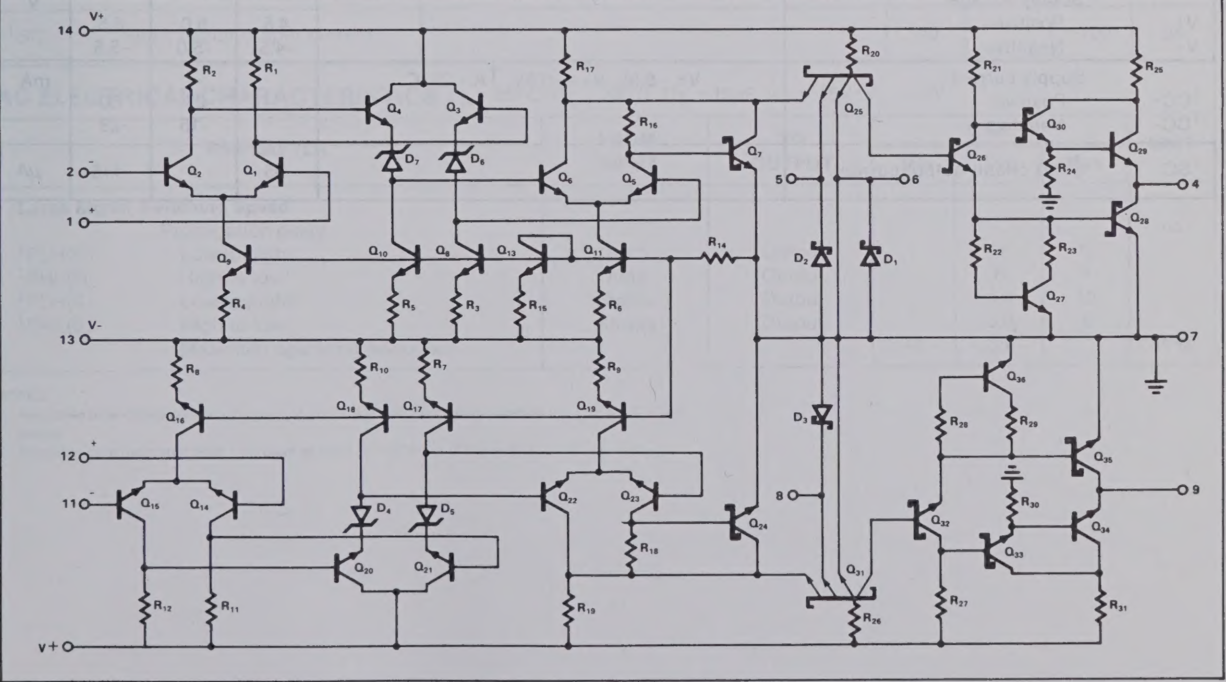
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM


INPUT 1A (1)
INPUT 1B (2)
OUTPUT 1Y (4)
STROBE 1G (5)
STROBE S (6)
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G

EQUIVALENT SCHEMATIC


V+
14
2
1
13
V-
12
11
v+
5
6
8
4
7
9
R2
R1
R17
R20
R21
R25
R16
R24
R4
R5
R3
R15
R6
R14
R22
R23
R8
R10
R7
R9
R28
R29
R30
R18
R12
R11
R19
R26
R27
R31
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
D1
D2
D3
D4
D5
D6
D7

NE521-F,N
SE521-F

DC ELECTRICAL CHARACTERISTICS V+ = +5V, V- = -5V, T_A = -55 to +125°C unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.5V, V- = -4.5V		 6	 7.5 15	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.5V, V- = -5.5V		 7.5	 20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.5V, V- = -5.5V		 1.0	 5 12	μA
V_{CM}	Common mode voltage range	V+ = +4.5V, V- = -4.5V	±3			V
V_{IL}	Low level input voltage At 25°C Over temperature				 0.8 0.7	V
V_{IH}	High level input voltage		2.0			V
I_{IH}	Input current High	V+ = +5.5V, V- = -5.5V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			 50 100	 μA μA
I_{IL}	Low	V_{IL} = 0.5V 1G or 2G strobe Common strobe S			 -2.0 -4.0	 mA mA
V_{OH} V_{OL}	Output voltage High Low	$V_{I(S)}$ = 2.0V V+ = +4.5V, V- = -4.5V, I_{LOAD} = -1mA V+ = +4.5V, V- = -4.5V, I_{LOAD}= 10mA T_A = 25°C, I_{LOAD} = 20mA	 2.5	 3.4	 0.5 0.5	V
V+ V-	Supply voltage Positive Negative		 4.5 -4.5	 5.0 -5.0	 5.5 -5.5	V
I_{CC+} I_{CC-}	Supply current Positive Negative	V+ = 5.5V, V- = -5.5V, T_A = 25°C		 27 -15	 50 -28	mA
I_{SC}	Short circuit output current		-35		-115	μA

NE521-F,N
SE521-F

DC ELECTRICAL CHARACTERISTICS (Cont'd) V+ = +5V, V- = -5V, T_A = 0 to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$ = 2.0V				V
V_{OH}	High	V+ = +4.75V, V- = -4.75V, I_{LOAD} = -1mA	2.7	3.4		
V_{OL}	Low	V+ = +5.25V, V- = -5.25V, I_{LOAD} = 20mA			0.5	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	
I_{SC}	Short circuit output current		-40		-100	μA

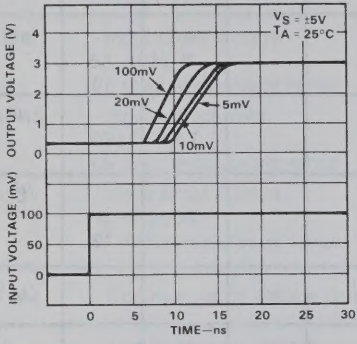
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280 Ω C_L = 15pF V+ = +5V V- = -5V

PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	6	
	Maximum operating frequency			40	55		MHz

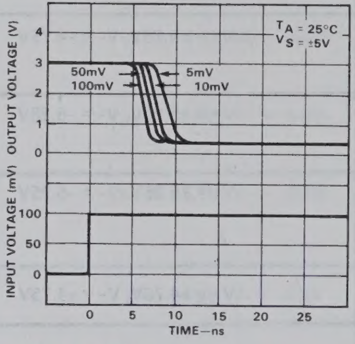
NOTES
1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS

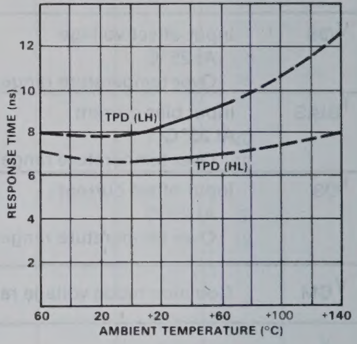
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



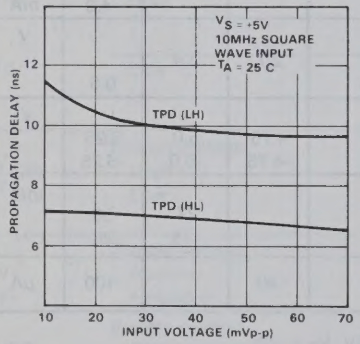
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



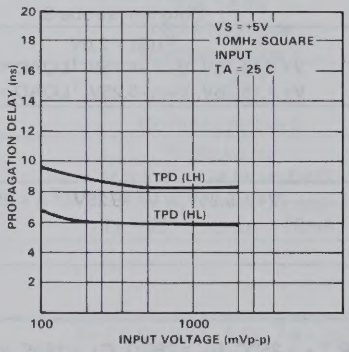
RESPONSE TIME vs TEMPERATURE



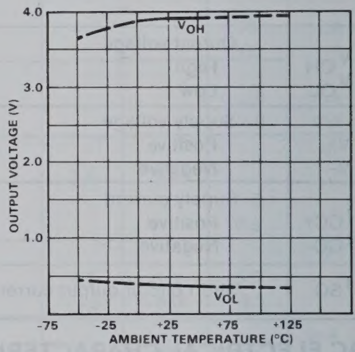
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



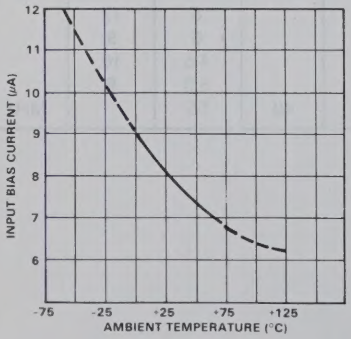
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



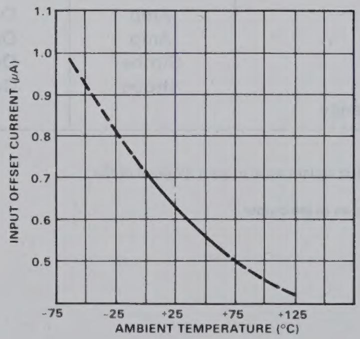
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE522

NE522-F,N • SE522-F

FEATURES

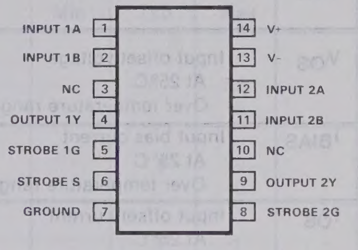
- 15ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Open collector output for wire-OR'd applications
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

PIN CONFIGURATION

F,N PACKAGE

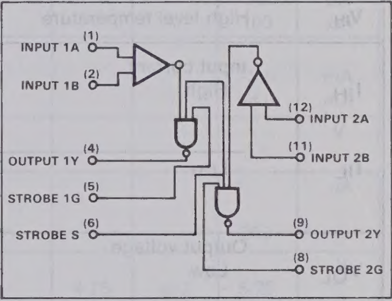

INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V+
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G

Order Part No.
NE522 F,N
SE522 F

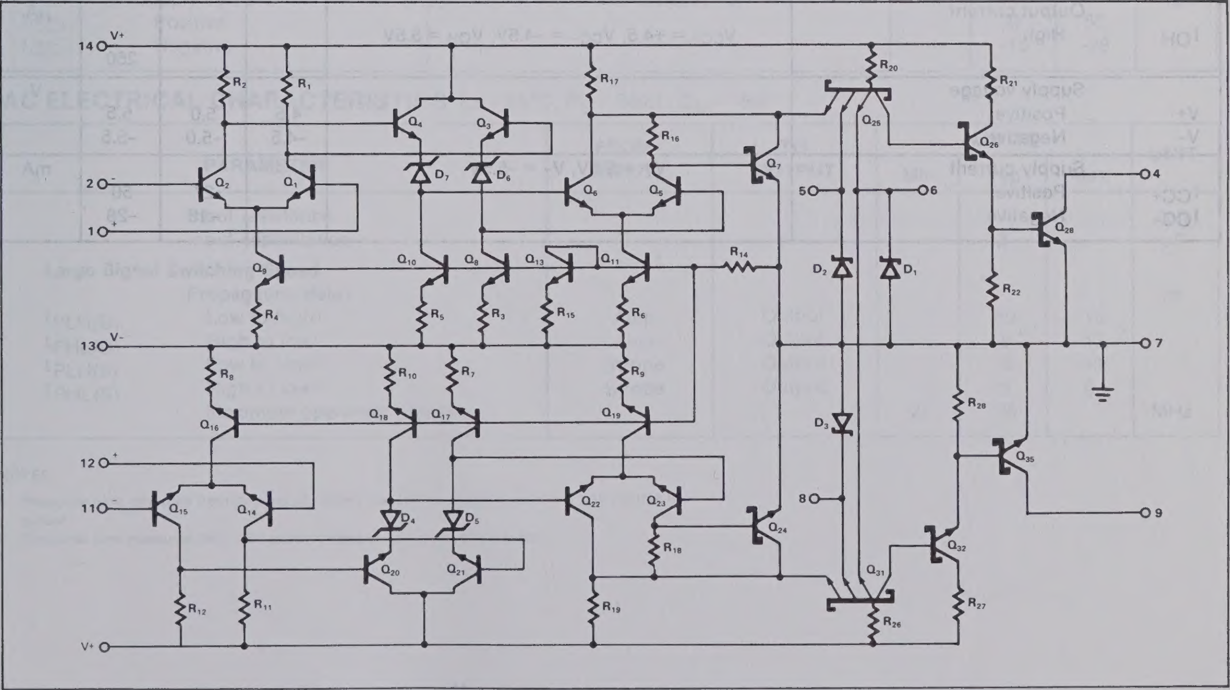
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	±5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE	0 to 70	°C
	SE	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM


INPUT 1A (1)
INPUT 1B (2)
(12) INPUT 2A
(11) INPUT 2B
OUTPUT 1Y (4)
STROBE 1G (5)
STROBE S (6)
(9) OUTPUT 2Y
(8) STROBE 2G

EQUIVALENT SCHEMATIC


14 V+
R2
R1
R17
R20
R21
Q4
Q3
R16
Q25
Q26
Q7
D7
D6
2 -
Q2
Q1
Q6
Q5
5
6
4
1 +
Q28
Q9
Q10
Q8
Q13
Q11
R14
D2
D1
R4
R5
R3
R15
R6
R22
13 V-
7
R8
R10
R7
R9
R28
D3
Q16
Q18
Q17
Q19
Q35
12 +
11 -
Q15
Q14
Q22
Q23
8
Q24
Q32
9
D4
D5
Q20
Q21
R18
Q31
R12
R11
R19
R26
R27
V+

DC ELECTRICAL CHARACTERISTICS ±5V ±10%, T_A = -55 to 125°C unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.5V, V- = -4.5V		6	7.5 15.	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.5V, V- = -5.5V		7.5	20. 40.	µA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.5V, V- = -5.5V		1.0	5. 12.	µA
V_{CM}	Common mode voltage range	V+ = +4.5V, V- = -4.5V	±3			V
V_{IL}	Low level input Voltage at 25°C over temperature				.08 .07	V
V_{IH}	High level temperature		2.0			V
I_{IH}	Input current High	V+ = +5.5V, V- = -5.5V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			50 100	µA µA
I_{IL}	Low	V_{IL} = 0.5V 1G 2G strobe Common strobe S			-2 -4	mA mA
V_{OL}	Output voltage Low	V+ = +4.5V, V- = -4.5V I_{OL} = 20mA, T_A = 25°C I_{OL} = 10mA			.5 .5	V
I_{OH}	Output current High	V_{CC+} = +4.5, V_{CC-} = -4.5V, V_{OH} = 5.5V			250	µA
	Supply voltage					V
V+	Positive		4.5	5.0	5.5	
V-	Negative		-4.5	-5.0	-5.5	
	Supply current	V+ = 5.5V, V- = -5.5V				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	

DC ELECTRICAL CHARACTERISTICS (Cont'd) ±5V ±5%, T_A = 0 to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V− = −4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V− = −5.25V				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V− = −5.25V				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V− = −4.75V	±3			V
	Input current	V+ = +5.25V, V− = −5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			−2.0	mA
		Common strobe S			−4.0	mA
	Output voltage	V+ = +5.25V, V− = −5.25V, $V_{I(S)}$ = 2.0V				V
V_{OL}	Low	I_{LOAD} = 20mA			0.5	
	Output current					μA
I_{OH}	High	V_{CC+} = +4.75, V_{CC-} = −4.75V, V_{OH} = 5.25V			250	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V−	Negative		−4.75	−5.0	−5.25	
	Supply current	V+ = 5.25V, V− = −5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			−15	−28	

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω, C_L = 15pF

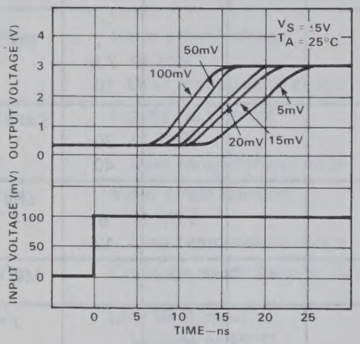
PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
	Input resistance				4		kΩ
	Input capacitance				3		pF
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	13	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	9	
	Maximum operating frequency			25	35		MHz

NOTES

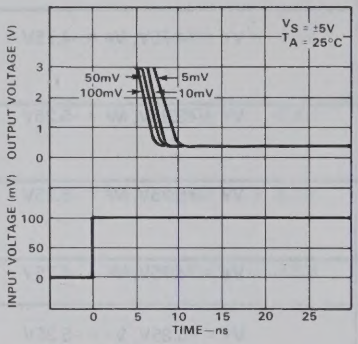
1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS

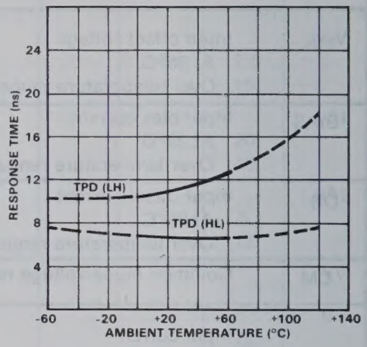
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



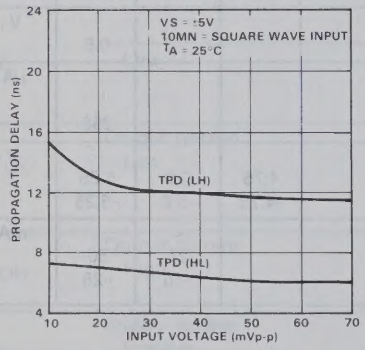
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



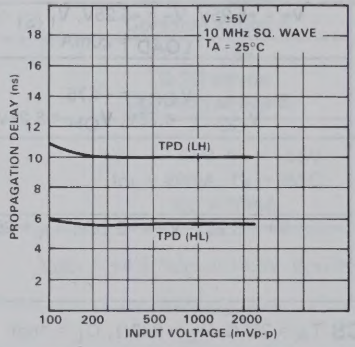
RESPONSE TIME vs TEMPERATURE



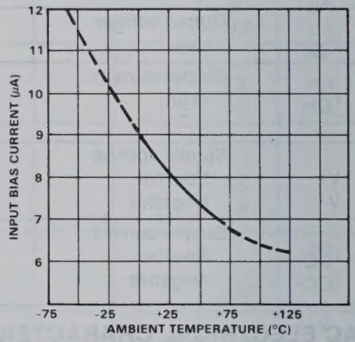
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



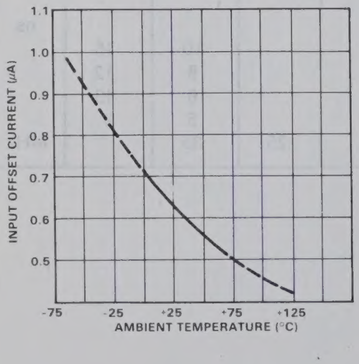
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

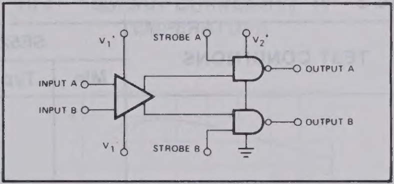
FEATURES

- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Mil std 883A,B,C available**

APPLICATIONS

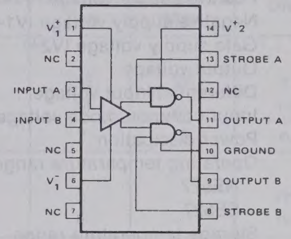
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**

BLOCK DIAGRAM

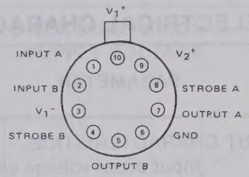

V_1^+
STROBE A
V_2^+
INPUT A
INPUT B
OUTPUT A
OUTPUT B
V_1^-
STROBE B

PIN CONFIGURATIONS

F,N PACKAGE

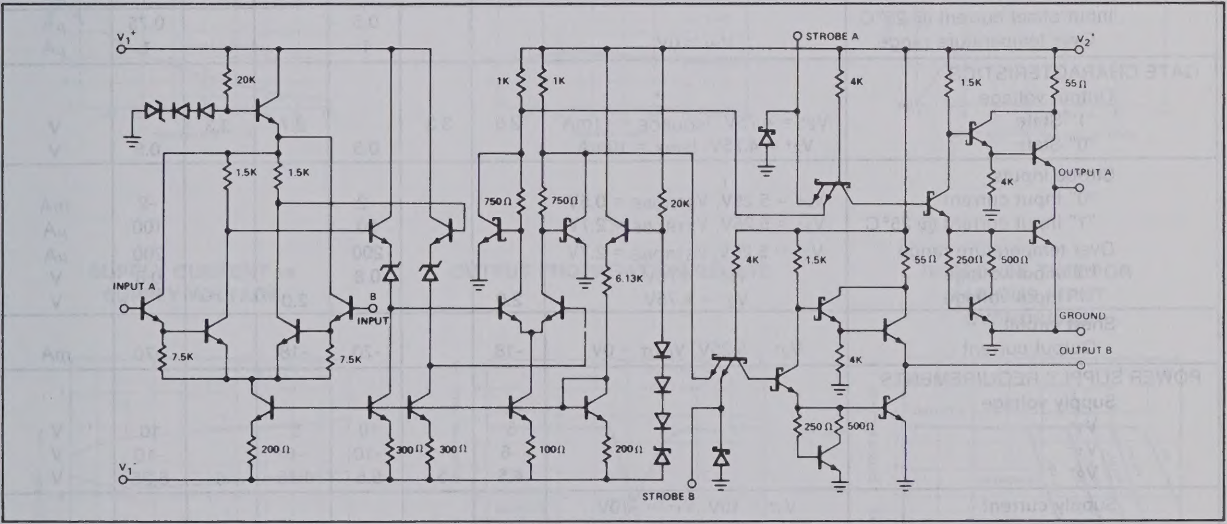

V_1^+ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
V_1^- 6
NC 7
14 V^+_2
13 STROBE A
12 NC
11 OUTPUT A
10 GROUND
9 OUTPUT B
8 STROBE B

H PACKAGE*


V_1^+
INPUT A
V_2^+
INPUT B
STROBE A
V_1^-
OUTPUT A
STROBE B
GND
OUTPUT B
1
2
3
4
5
6
7
8
9
10

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC


V_1^+
20K
1.5K
1.5K
INPUT A
7.5K
7.5K
B INPUT
200 Ω
300 Ω
300 Ω
100 Ω
200 Ω
V_1^-
1K
1K
750 Ω
750 Ω
20K
6.13K
STROBE B
STROBE A
4K
4K
1.5K
4K
250 Ω
500 Ω
V_2^+
1.5K
55 Ω
4K
OUTPUT A
55 Ω
250 Ω
500 Ω
GROUND
OUTPUT B

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE527	0 to +70	°C
SE527	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $V_{1^+} = 10V$, $V_{1^-} = -10V$, $V_{2^+} = +5.0V$

PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @ 25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @ 25°C				2			2	μA
Over temperature range				4			4	μA
Input offset current @ 25°C				0.5			0.75	μA
Over temperature range	$V_{IN} = 0V$			1			1	μA
GATE CHARACTERISTICS								
Output voltage								
"1" State	$V_{2^+} = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_{2^+} = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current	$V_{2^+} = 5.25V$, $V_{STROBE} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C	$V_{2^+} = 5.25V$, $V_{STROBE} = 2.7V$			50			100	μA
Over temperature range	$V_{2^+} = 5.25V$, $V_{STROBE} = 2.7V$			200			200	μA
"0" Input voltage	$V_{2^+} = 4.75V$			0.8			0.8	V
"1" Input voltage	$V_{2^+} = 4.75V$	2.0			2.0			V
Short circuit Output current	$V_{2^+} = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_{1^+}		5		10	5		10	V
V_{1^-}		-6		-10	-6		-10	V
V_{2^+}		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_{1^+} = 10V$, $V_{1^-} = -10V$ $V_{2^+} = 5.25V$							
I_{1^+}	Over temp.			5			5	mA
I_{1^-}	Over temp.			10			10	mA
I_{2^+}	Over temp.			20			20	mA

*NOTE

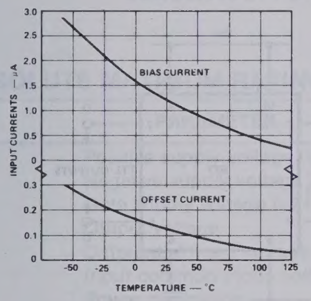
Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

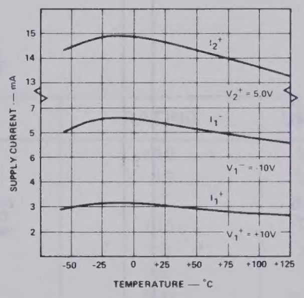
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response propagation delay time	$V_{IN} = \pm 100mV$ step				
t_{PLH}			16	26	ns
t_{PHL}			14	24	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{on} Turn-on time			6		ns
t_{off} Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

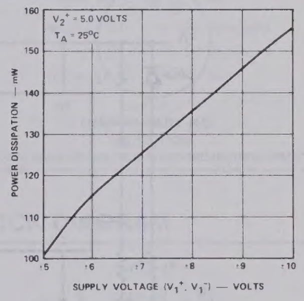
INPUT CURRENTS vs TEMPERATURE



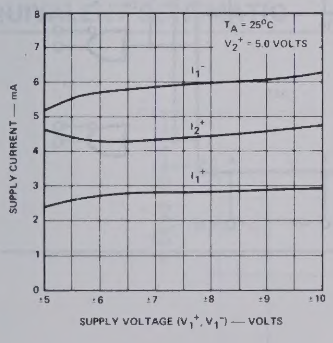
SUPPLY CURRENT vs TEMPERATURE



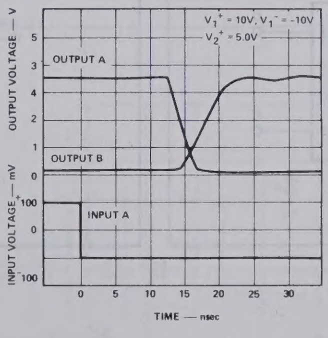
POWER DISSIPATION vs SUPPLY VOLTAGE



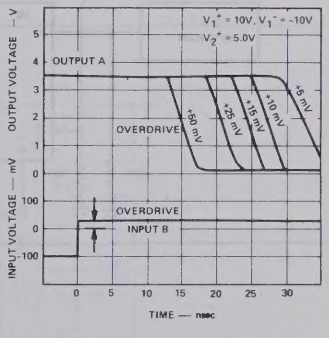
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



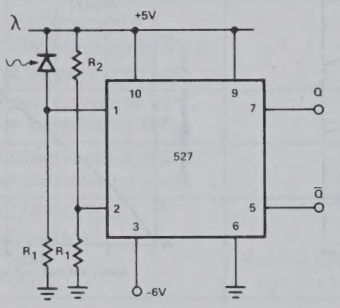
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1−) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

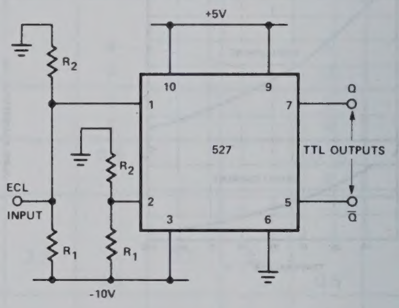
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

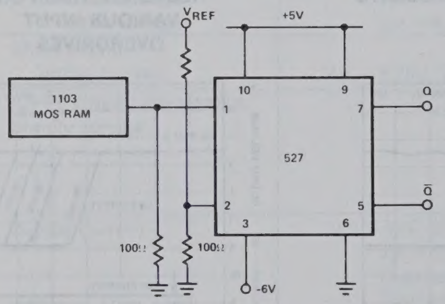
PHOTODIODE DETECTOR


λ
+5V
R2
10
9
1
7
Q
527
Q̄
2
5
3
6
R1
R1
-6V

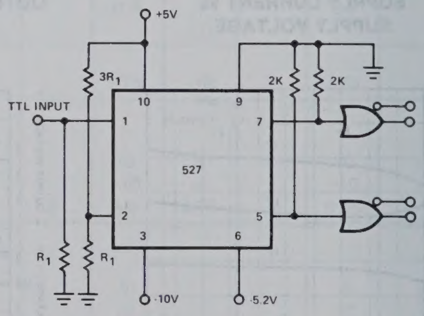
ECL TO TTL INTERFACE


+5V
R2
10
9
1
7
Q
R2
527
TTL OUTPUTS
ECL
INPUT
2
5
Q̄
3
6
R1
R1
-10V

MOS MEMORY SENSE AMP


VREF
+5V
1103
MOS RAM
10
9
1
7
Q
527
Q̄
2
5
3
6
100Ω
100Ω
-6V

TTL TO ECL INTERFACE


+5V
3R1
2K
2K
TTL INPUT
10
9
1
7
527
2
5
3
6
R1
R1
-10V
-5.2V

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

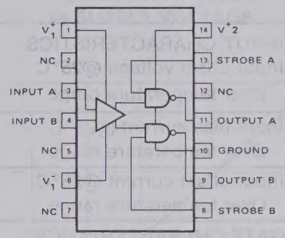
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**

APPLICATIONS

- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **Mil std 883A,B,C available**

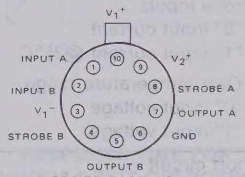
PIN CONFIGURATION

F,N PACKAGE


V_1^+ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
V_1^- 6
NC 7
14 V^+2
13 STROBE A
12 NC
11 OUTPUT A
10 GROUND
9 OUTPUT B
8 STROBE B

ORDER PART NO.
NE/SE529F,NE529N

H PACKAGE*


V_1^+
INPUT A
V_2^+
INPUT B
STROBE A
V_1^-
OUTPUT A
STROBE B
GND
OUTPUT B
1
2
3
4
5
6
7
8
9
10

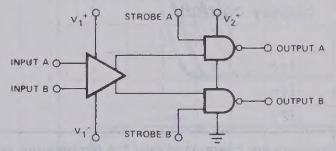
ORDER PART NO.
NE/SE529H

*Metal cans (H) not recommended for new designs

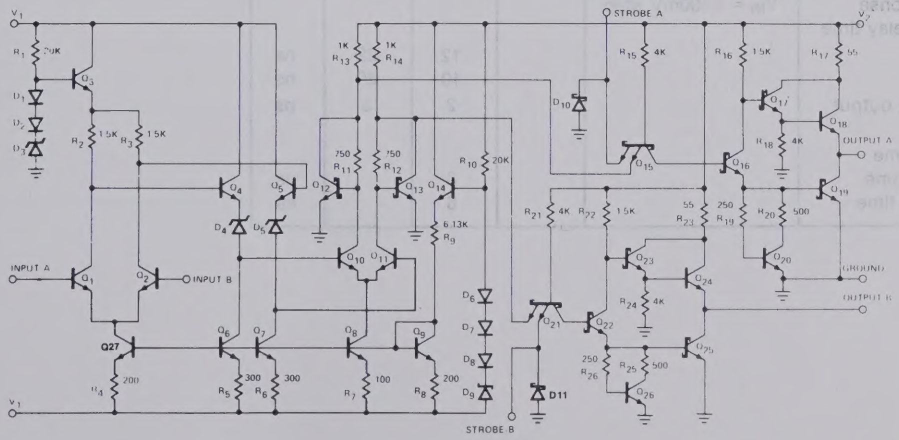
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM


V_1^+
STROBE A
V_2^+
OUTPUT A
INPUT A
INPUT B
OUTPUT B
V_1^-
STROBE B

EQUIVALENT SCHEMATIC


V_1
R_1 20K
Q_3
D_1
D_2
D_3
R_2 1.5K
R_3 1.5K
Q_4
Q_5
D_4
D_5
INPUT A
Q_1
Q_2
INPUT B
Q27
R_4 200
Q_6
Q_7
R_5 300
R_6 300
1K R_{13}
1K R_{14}
750 R_{11}
750 R_{12}
Q_{12}
Q_{13}
Q_{14}
Q_{10}
Q_{11}
Q_8
Q_9
R_7 100
R_8 200
R_{10} 20K
6.13K R_9
D_6
D_7
D_8
D_9
STROBE B
V_1
STROBE A
D_{10}
R_{15} 4K
Q_{15}
R_{16} 1.5K
Q_{16}
Q_{17}
R_{17} 55
V_2
Q_{18}
R_{18} 4K
OUTPUT A
Q_{19}
R_{21} 4K
R_{22} 1.5K
55 R_{23}
250 R_{19}
R_{20} 500
Q_{20}
GROUND
Q_{23}
Q_{24}
OUTPUT B
Q_{21}
Q_{22}
R_{24} 4K
250 R_{26}
R_{25} 500
Q_{25}
Q_{26}
D11

DC ELECTRICAL CHARACTERISTICS $V_1+ = +10V$, $V_2+ = +5.0V$, $V_1- = -10V$

PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @25°C			5	12		5	20	µA
Over temperature range	$V_{IN} = 0V$			36			50	µA
Input offset current @25°C			2	3		2	5	µA
Over temperature range	$V_{IN} = 0V$			9			15	µA
GATE CHARACTERISTICS								
Output voltage								
"1" state	$V_2+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" state	$V_2+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" input current	$V_2+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" input current @25°C	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	µA
Over temperature range	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			200			200	µA
"0" input voltage	$V_2+ = 4.75V$			0.8			0.8	V
"1" input voltage	$V_2+ = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_1+		5		10	5		10	V
V_1-		-6		-10	-6		-10	V
V_2+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_1+ = 10V$, $V_1- = -10V$ $V_2+ = 5.25V$							
I_1+	Over temp.			5			5	mA
I_1-	Over temp.			10			10	mA
I_2+	Over temp.			20			20	mA

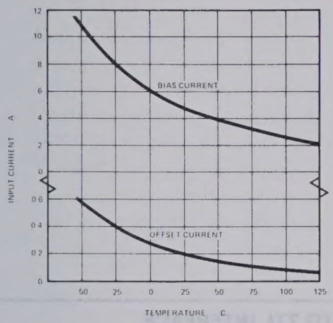
Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

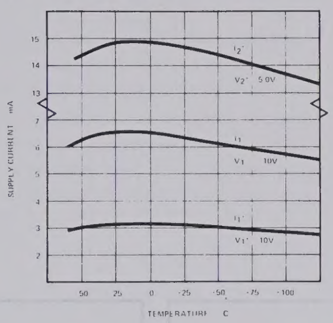
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = \pm100mV$ step				
Propagation delay time					
t_{PLH}			12	22	ns
t_{PHL}			10	20	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{ON} turn-on time			6		ns
t_{OFF} turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

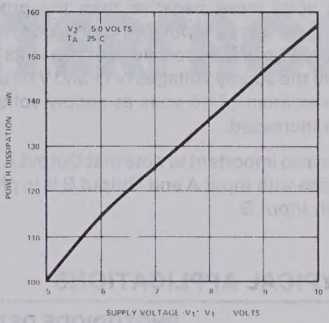
INPUT CURRENTS vs TEMPERATURE



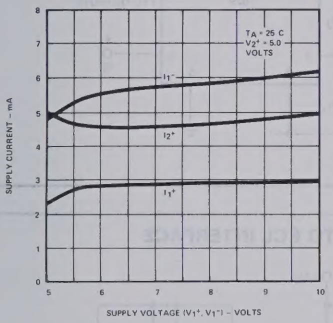
SUPPLY CURRENT vs TEMPERATURE



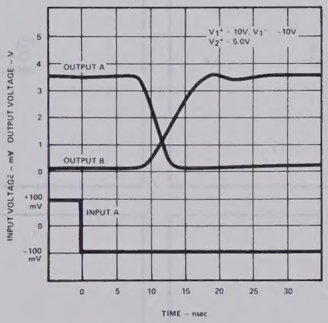
POWER DISSIPATION vs SUPPLY VOLTAGE



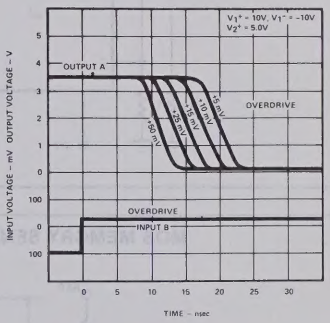
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



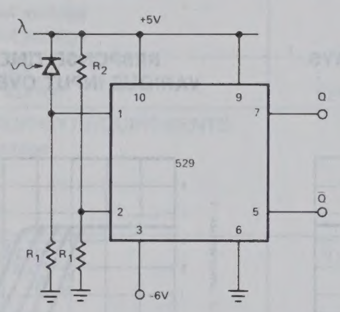
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1–) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1–) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1–) up to a maximum of ±6 volts as supply voltages are increased.

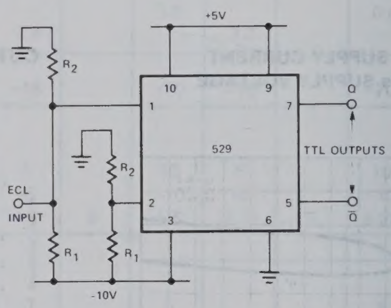
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

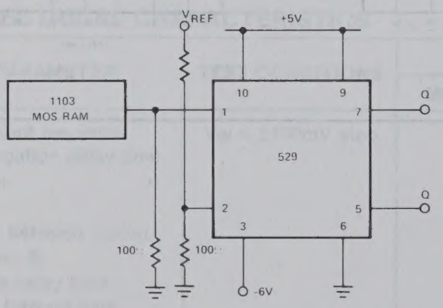
PHOTODIODE DETECTOR


λ
+5V
R2
10
9
1
7
Q
529
2
5
Q̄
3
6
R1
R1
-6V

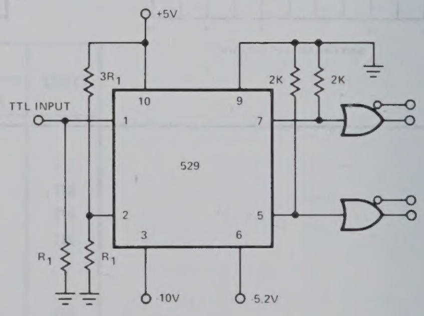
ECL TO TTL INTERFACE


+5V
R2
10
9
Q
1
7
529
TTL OUTPUTS
R2
ECL
INPUT
2
5
3
6
Q̄
R1
R1
-10V

MOS MEMORY SENSE AMP


VREF
+5V
1103
MOS RAM
10
9
1
7
Q
529
2
5
Q
3
6
100
100
-6V

TTL TO ECL INTERFACE


+5V
3R1
2K
2K
TTL INPUT
10
9
1
7
529
2
5
3
6
R1
R1
10V
5.2V

SECTION 6
MICROPROCESSOR INTERFACE

Section 6—MICROPROCESSOR INTERFACE

NE590/591 Addressable Peripheral Drivers 225

NE590-F,N • NE591-F,N

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

FEATURES

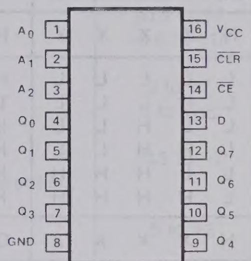
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 9334**

APPLICATIONS

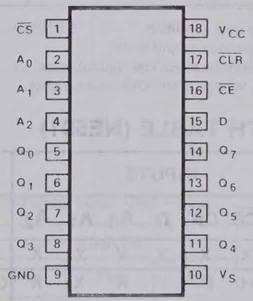
- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATIONS

NE590
F,N PACKAGE



NE591
F,N PACKAGE



PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
—	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
—	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	Memory
H	L	L	L	L	L	H	Q_{N-1}	→	→	→	→	→	→	Addressable Latch
H	L	H	L	L	L	L	Q_{N-1}	→	→	→	→	→	→	
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1}	→	→	→	→	→	
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1}	→	→	→	→	→	→	H	
H	L	H	H	H	H	Q_{N-1}	→	→	→	→	→	→	L	

X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

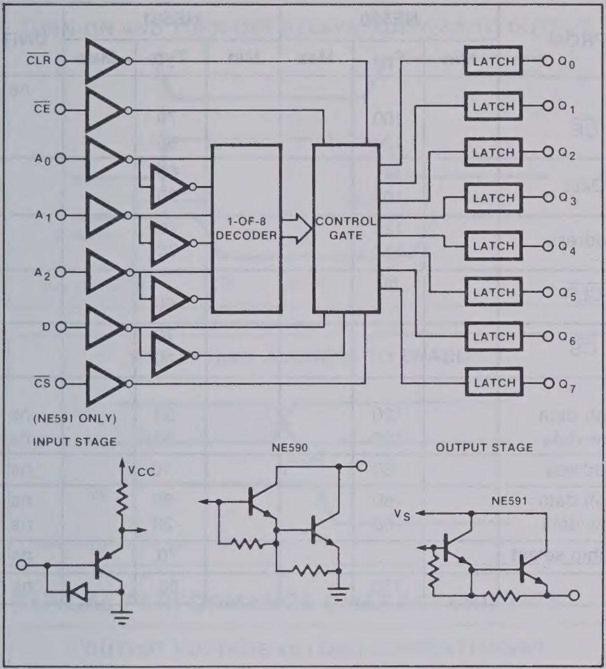
TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	Memory
H	H	L	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	
H	L	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	
H	L	L	L	L	L	L	L	Q_{N-1}	→	→	→	→	→	→	Addressable Latch
H	L	L	H	L	L	L	H	Q_{N-1}	→	→	→	→	→	→	
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}	→	→	→	→	→	
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}	→	→	→	→	→	
H	L	L	L	H	H	H	Q_{N-1}	→	→	→	→	→	→	L	
H	L	L	H	H	H	H	Q_{N-1}	→	→	→	→	→	→	H	

X = Don't care
Q_{N-1} = Previous output state
L = Low voltage level/"OFF" output state
H = High voltage level/"ON" output state

NE590-F,N • NE591-F,N

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage		V
	NE590	0 to +7	
	NE591	0 to V_{CC}	
V_S	Source bus voltage		V
	NE591 only	-0.5 to +7	
V_S-V_{CC}	Source/supply differential voltage		V
	NE591 only	-5 to +2	
I_{OUT}	Output current		mA
	Each output	300	
	All outputs	1000	
P_D	Power dissipation[1]	1	W
	Temperature range		°C
T_A	Ambient	0 to +70	
T_J	Junction	150	
T_{STG}	Storage	-65 to +150	
T_{sold}	Lead soldering temperature (10sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified.[2,3]

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				0.8	
	Output voltage					V
V_{OL}	Low (NE590 only)	I_{OL} = 250mA, T_A = 25°C		1.0	1.3	
		Over temperature			1.5	
V_{OH}	High (NE591 only)	I_{OH} = -250mA, V_{CC} = V_S = 5V	2.9			
	Input current					μA
I_{IH}	High	V_{in} = V_{CC}		0.1	10	
I_{IL}	Low	V_{in} = 0V				
	$\overline{CE}$ input			-25	-60	
	All other inputs			-15	-50	
	Supply current[4]	V_S = V_{CC} = 5V				mA
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					
	NE590			15	50	
	NE591			30	50	

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature:
   NE590N at 95°C/W above 55°C
   NE590F at 100°C/W above 50°C
   NE591N at 90°C/W above 60°C
   NE591F at 93°C/W above 57°C
2. All typical values are at V_{CC} = 5V and T_A = 25°C.
3. For the NE591, V_S = V_{CC} in all tests.
4. Supply current for the NE591 is measured with no output load.

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

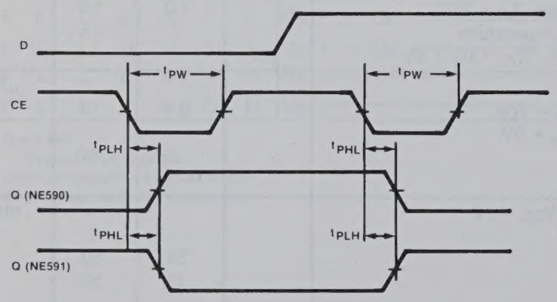
PARAMETER	TO	FROM	NE590			NE591			UNIT
			Min	Typ	Max	Min	Typ	Max	
Propagation delay time									ns
t_{PLH} Low to high[5]	Output	$\overline{CE}$		100			70		
t_{PHL} High to low[5]				130			80		
t_{PLH} Low to high[6]	Output	Data		80			60		
t_{PHL} High to low[6]				100			70		
t_{PLH} Low to high[7]	Output	Address		125			70		
t_{PHL} High to low[7]				115			70		
t_{PLH} Low to high[8]	Output	$\overline{CLR}$		80					
t_{PHL} High to low[8]							60		
t_{PLH} Low to high[5]	Output	$\overline{CS}$					70		
t_{PHL} High to low[5]							80		
SWITCHING SET-UP REQUIREMENTS									
$t_{S(H)}$[9]	Chip enable	High data		120			50		ns
$t_{S(L)}$[9]	Chip enable	Low data		120			70		ns
$t_{S(A)}$[10]	Chip enable	Address		-60			-10		ns
$t_{h(H)}$[9]	Chip enable	High data		-60			-60		ns
$t_{h(L)}$[9]	Chip enable	Low data		-60			-20		ns
$t_{S(CS)}$[9]	Chip enable	Low chip select					70		ns
$t_{pw(E)}$ Chip enable pulse width[5]				150			80		ns

NOTES

5. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
6. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
7. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
8. See Turn-Off Delay, Clear to Output timing diagram.
9. See Setup and Hold Time, Data to Enable timing diagram.
10. See Setup Time, Address to Enable timing diagram.

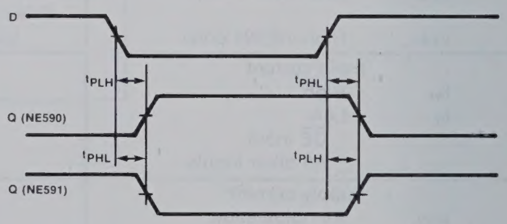
TIMING DIAGRAMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



Other Inputs: $\overline{CLR}$ = H, A = Stable, $\overline{CS}$ = L

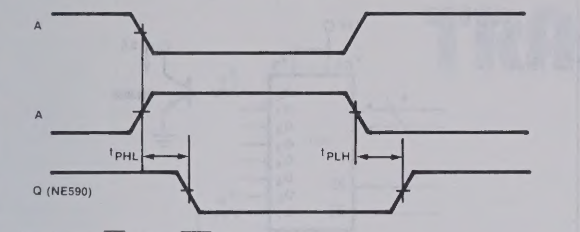
TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



Other Inputs: $\overline{CE}$ = $\overline{CS}$ = L, $\overline{CLR}$ = H, A = Stable

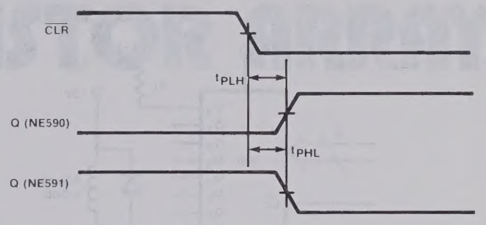
TIMING DIAGRAMS (Cont'd)

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT


A
A
t_{PHL}
t_{PLH}
Q (NE590)

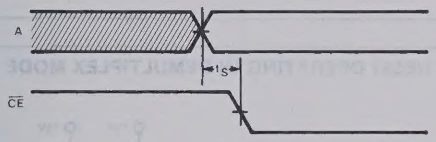
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

TURN-OFF DELAY, CLEAR TO OUTPUT


$\overline{CLR}$
t_{PLH}
Q (NE590)
t_{PHL}
Q (NE591)

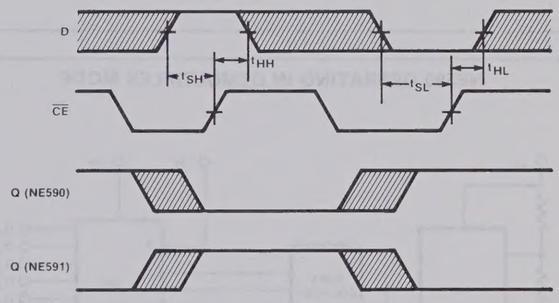
Other Inputs: $\overline{CE}$ = H, $\overline{CS}$ = H

SETUP TIME, ADDRESS TO ENABLE


A
t_S
$\overline{CE}$

Other Inputs: $\overline{CLR}$ = H, $\overline{CS}$ = L

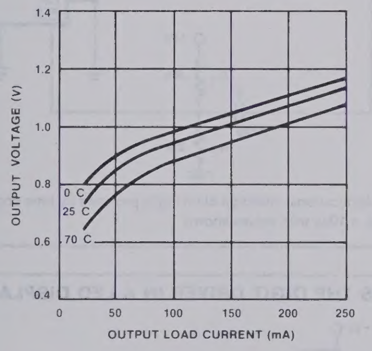
SETUP AND HOLD TIME, DATA TO ENABLE


D
t_{SH}
t_{HH}
t_{SL}
t_{HL}
$\overline{CE}$
Q (NE590)
Q (NE591)

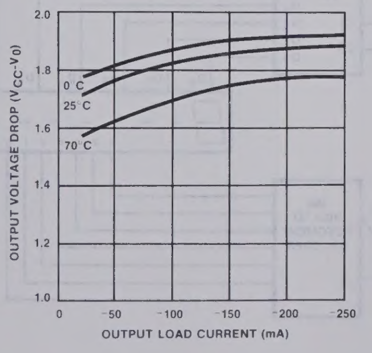
Other Inputs: $\overline{CLR}$ = H, A = Stable, $\overline{CS}$ = L

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE VS LOAD CURRENT(NE590)

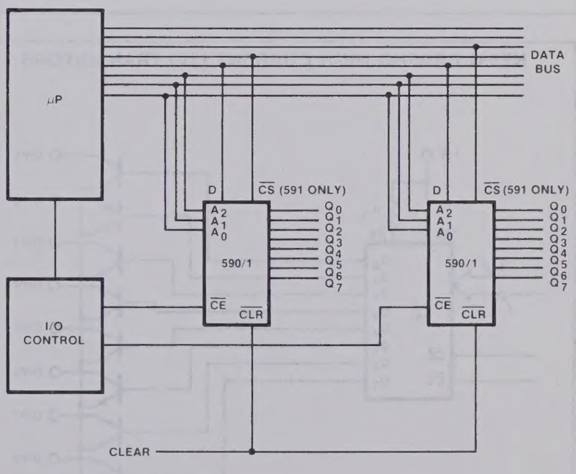


OUTPUT VOLTAGE DROP VS LOAD CURRENT(NE591)



TYPICAL APPLICATIONS

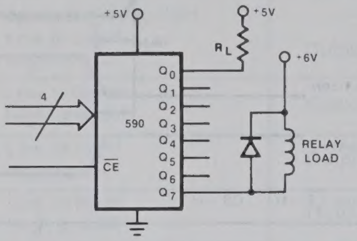
INTERFACING THE 590/591 WITH A MICROPROCESSOR SYSTEM


μP
DATA BUS
I/O CONTROL
D
$\overline{CS}$ (591 ONLY)
A_2
A_1
A_0
590/1
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CLR}$
D
$\overline{CS}$ (591 ONLY)
A_2
A_1
A_0
590/1
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CLR}$
CLEAR

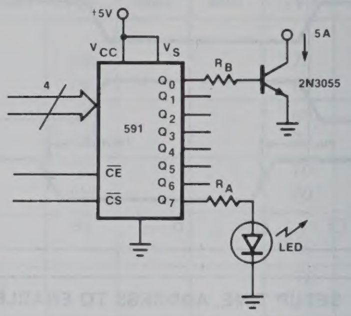
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

TYPICAL APPLICATIONS (Cont'd)

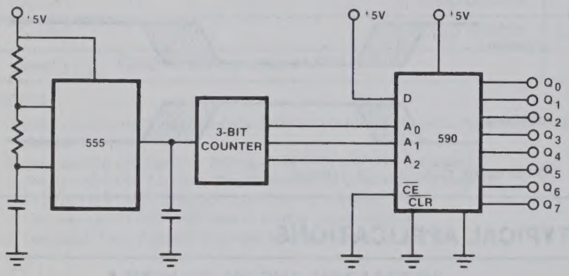
NE590 DRIVING SIMPLE LOADS


+5V
+5V
R_L
+6V
4
590
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
RELAY
LOAD

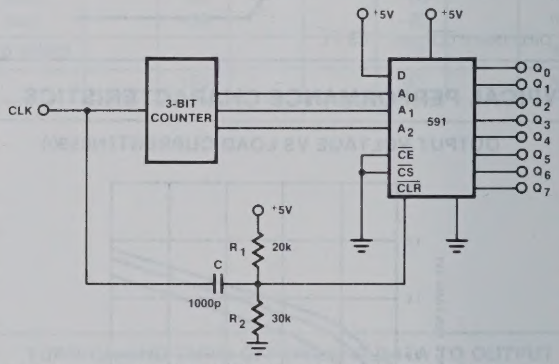
NE591 DRIVING SIMPLE LOADS


+5V
V_{CC}
V_S
R_B
5A
2N3055
4
591
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CS}$
R_A
LED

NE590 OPERATING IN DEMULTIPLEX MODE

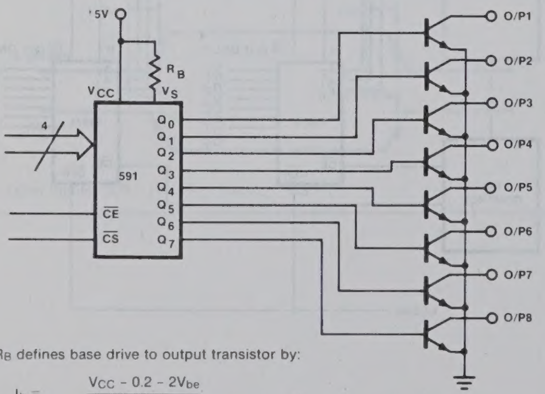

+5V
555
3-BIT
COUNTER
+5V
+5V
D
A_0
A_1
A_2
590
$\overline{CE}$
$\overline{CLR}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7

NE591 OPERATING IN DEMULTIPLEX MODE


+5V
+5V
CLK
3-BIT
COUNTER
D
A_0
A_1
A_2
591
$\overline{CE}$
$\overline{CS}$
$\overline{CLR}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
+5V
R_1
20k
C
1000p
R_2
30k

For display applications, interdigit blanking is provided by time constant $\tau = C(R_1/R_2)$, $\approx 10\mu s$ with values shown.

NE591 DRIVING HIGH CURRENT (5A) TRANSISTORS

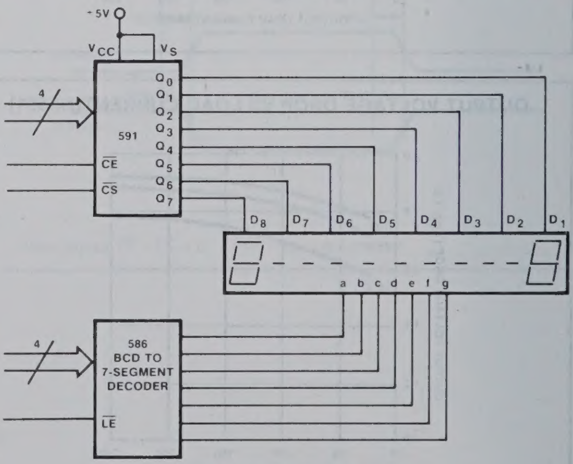

+5V
R_B
V_{CC}
V_S
4
591
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CS}$
O/P1
O/P2
O/P3
O/P4
O/P5
O/P6
O/P7
O/P8

R_B defines base drive to output transistor by:

$$I_b = \frac{V_{CC} - 0.2 - 2V_{be}}{R_b}$$

provided that only one output is ON at any time.

NE591 AS THE DIGIT DRIVER IN A LED DISPLAY SYSTEM


+5V
V_{CC}
V_S
4
591
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CS}$
D_8
D_7
D_6
D_5
D_4
D_3
D_2
D_1
a b c d e f g
4
586
BCD TO
7-SEGMENT
DECODER
$\overline{LE}$

SECTION 7
TRANSISTOR ARRAYS

Section 7—TRANSISTOR ARRAYS

CA3081/3082 Seven Transistor Array 233
ULN2001/2003/2004 High Voltage/High Current Darlington Transistor Arrays 236

SEVEN TRANSISTOR ARRAY CA3081/CA3082

F,N

DESCRIPTION

The CA3081 and CA3082 are monolithic integrated circuits, each consisting of seven separate npn transistors on a common substrate. The transistors are capable of driving loads of up to 100mA. At the same time, the transistor geometry used gives maximum current gain at quite low currents, making the devices also suitable for small-signal applications. In the CA3081, the transistors are connected in a common emitter configuration, while in the CA3082, the collectors are common. The transistor arrays are particularly suitable for driving light-emitting diodes and seven-segment displays, as well as for general purpose applications. The CA3081 and CA3082 are available in both 16-lead dual-in-line plastic and cerdip packages.

FEATURES

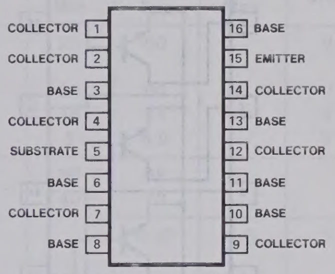
- **Seven transistors permit a wide range of applications in either a common emitter (CA3081) or common-collector (CA3082) configuration.**
- **High I_C: 100mA maximum**
- **Low $V_{CE\ sat}$ (at 50mA): 0.4V typical**

APPLICATIONS

- **Drivers for:**
  Incandescent display devices
  LED
  Relay control
  Thyristor firing

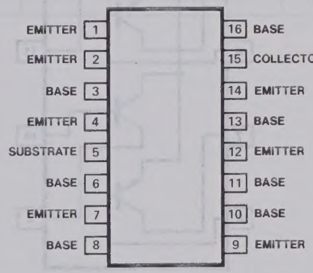
PIN CONFIGURATIONS

CA3081 F,N PACKAGE


COLLECTOR 1
COLLECTOR 2
BASE 3
COLLECTOR 4
SUBSTRATE 5
BASE 6
COLLECTOR 7
BASE 8
16 BASE
15 EMITTER
14 COLLECTOR
13 BASE
12 COLLECTOR
11 BASE
10 BASE
9 COLLECTOR

ORDER PART NO.
CA3081F, CA3081N

CA3082 F,N PACKAGE


EMITTER 1
EMITTER 2
BASE 3
EMITTER 4
SUBSTRATE 5
BASE 6
EMITTER 7
BASE 8
16 BASE
15 COLLECTOR
14 EMITTER
13 BASE
12 EMITTER
11 BASE
10 BASE
9 EMITTER

ORDER PART NO.
CA3082F, CA3082N

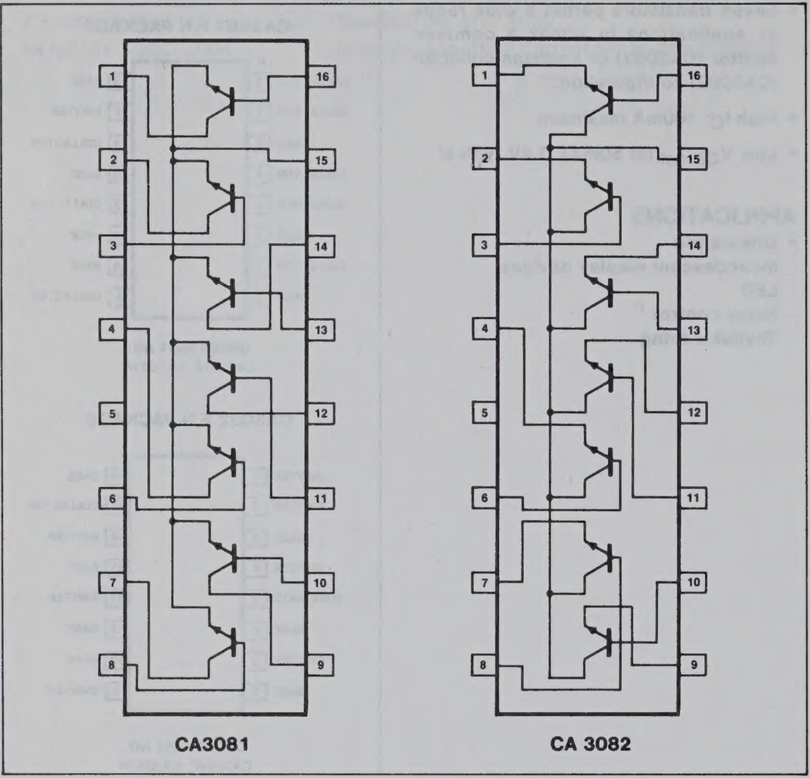
PIN DESIGNATION (CA3081)

PIN NO.	SYMBOL	NAME AND FUNCTION
1	C1	Collector, Transistor 1
2	C2	Collector, Transistor 2
3	B2	Base, Transistor 2
4	C5	Collector, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	C7	Collector, Transistor 7
8	B7	Base, Transistor 7
9	C6	Collector, Transistor 6
10	B6	Base, Transistor 6
11	B4	Base, Transistor 4
12	C4	Collector, Transistor 4
13	B3	Base, Transistor 3
14	C3	Collector, Transistor 3
15	E	Common emitter
16	B1	Base, Transistor 1

PIN DESIGNATION (CA3082)

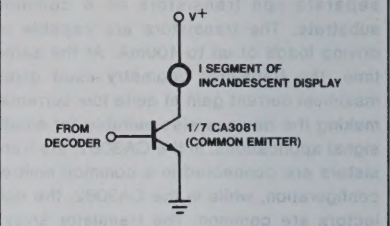
PIN	SYMBOL	NAME AND FUNCTION
1	E1	Emitter, Transistor 1
2	E2	Emitter, Transistor 2
3	B2	Base, Transistor 2
4	E5	Emitter, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	E6	Emitter, Transistor 6
8	B6	Base, Transistor 6
9	E7	Emitter, Transistor 7
10	B7	Base, Transistor 7
11	B4	Base, Transistor 4
12	E4	Emitter, Transistor 4
13	B3	Base. Transistor 3
14	E3	Emitter, Transistor 3
15	C	Common collector
16	B1	Base, Transistor 1

BLOCK DIAGRAM



CA3081 CA 3082

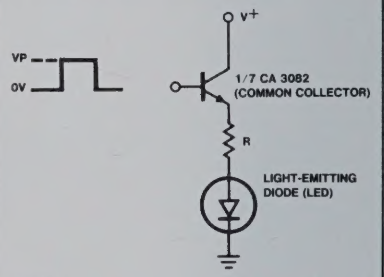
TYPICAL READ-OUT DRIVER APPLICATIONS


V+
I SEGMENT OF INCANDESCENT DISPLAY
FROM DECODER
1/7 CA3081 (COMMON EMITTER)

NOTE

Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.

Figure 6



NOTES

Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

*The resistance for R is determined by the relationship

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I(LED)}$$

$R = 0$ for $V_P = V_{BE} + V_F(LED)$

Where: V_P = Input pulse voltage

V_F = Forward voltage drop across the diode

Figure 7

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

PARAMETER		RATING	UNIT
P	Power dissipation:		
	Any one transistor	500	mW
P_{TOT}	Total package	750	mW
	Above 55°C	Derate Linearly 6.67	mW/°C
	Ambient temperature range:		
T_A	Operating	−55 to +125	°C
T_{stg}	Storage	−65 to +150	°C
	Lead temperature (10 seconds)	265	°C
V_{CEO}	Collector to emitter voltage[1]	16	V
V_{CBO}	Collector to base voltage[1]	20	V
V_{CIO}	Collector to substrate voltage[1,2]	20	V
V_{EBO}	Emitter to base voltage[1]	5	V
I_C	Collector current[1]	100	mA
I_B	Base current[1]	20	mA

NOTES

1. Ratings apply for each transistor in the device.
2. The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC ELECTRICAL CHARACTERISTICS FOR EACH TRANSISTOR $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
V_{CBO} (BR)	Collector to base breakdown voltage	$I_C = 500\mu A$, $I_E = 0$	20	60		V
V_{CIO} (BR)	Collector to substrate breakdown voltage	$I_C = 500\mu A$, $I_E = 0$, $I_B = 0$	20	60		V
V_{CEO} (BR)	Collector to emitter breakdown voltage	$I_C = 1mA$, $I_B = 0$	16	24		V
V_{EBO} (BR)	Emitter to base breakdown voltage	$I_C = 500\mu A$	5	6.9		V
h_{FE}	DC forward current Transfer Ratio	$V_{CE} = 0.5V$, $I_C = 30mA$	30	68		
		$V_{CE} = 0.8V$, $I_C = 50mA$	40	70		
V_{BE} sat	Base to emitter saturation voltage	$I_C = 30mA$, $I_B = 1mA$		0.87	1.0	V
V_{CE} sat	Collector to emitter saturation voltage					
	CA3081/CA3082	$I_C = 30mA$, $I_B = 1mA$		0.27	0.5	V
	CA3081	$I_C = 50mA$, $I_B = 5mA$		0.4	0.7	V
	CA3082	$I_C = 50mA$, $I_B = 5mA$		0.4	0.8	V
I_{CEO}	Collector cutoff current	$V_{CE} = 10V$, $I_B = 0$			10	µA
I_{CBO}	Collector cutoff current	$V_{CB} = 10V$, $I_E = 0$			1	µA

TYPICAL PERFORMANCE CHARACTERISTICS

h_{FE} vs I_C

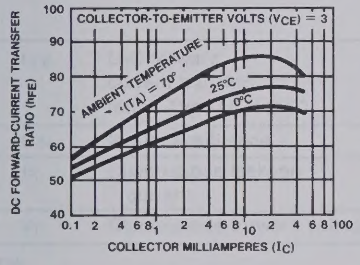


Figure 2

V_{BEsat} vs I_C

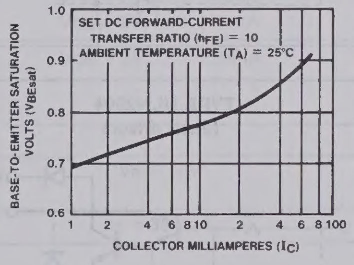


Figure 3

V_{CEsat} vs I_C at $T_A = 25°C$

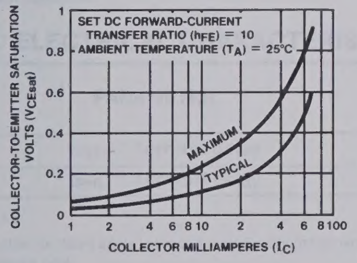


Figure 4

V_{CEsat} vs I_C at $T_A = 70°C$

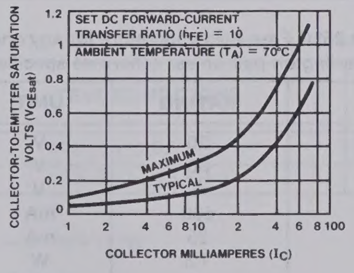


Figure 5

HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

ULN2001/2003/2004

ULN2001/2003/2004-N,F

DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type ULN-2001 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type ULN-2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.

The Type ULN-2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN-2003.

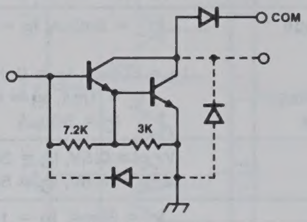
In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic package.

FEATURES

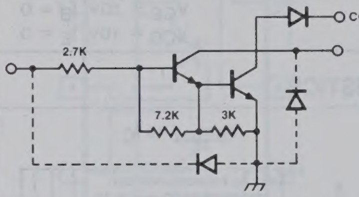
- **Peak inrush current 600mA**
- **Protected internally against inductive loads**
- **Open collector topology**
- **Compatible with most logic technologies**

EQUIVALENT SCHEMATICS

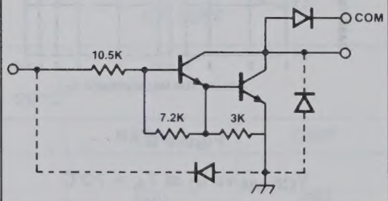
TYPE ULN2001
(each driver)



TYPE ULN2003
(each driver)

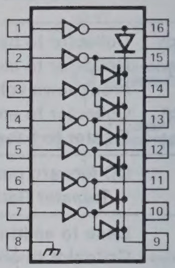


TYPE ULN2004
(each driver)



PIN CONFIGURATION

N,F PACKAGE



ORDER PART NO.
ULN2001N,F
ULN2003N,F
ULN2004N,F

ABSOLUTE MAXIMUM RATINGS

at 25°C Free-Air temperature for any one Darlington pair unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CE}	Output voltage	50	V
V_{IN}	Input voltage	30	V
V_{EBO}	Emitter base voltage	6	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_D	Power dissipation	1.3	W
	Derating factor above 25°C	95	°C/W
T_A	Ambient temperature range (operating)	0 to +85	°C
T_S	Storage temperature range	-65 to +150	°C

*NOTE
Under normal operating conditions, these units will sustain 350mA per output with $V_{CE(SAT)}$ = 1.6V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
I_{CEX}	Output leakage current	$V_{CE} = 50V$, $T_A = 70°C$	1A	—	—	100	μA
	Type ULN-2004	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 1V$	1B	—	—	500	μA
$V_{CE(SAT)}$	Collector-emitter Saturation voltage	$I_C = 350mA$, $I_B = 500\mu A$	2	—	1.25	1.6	V
		$I_C = 200mA$, $I_B = 350\mu A$	2	—	1.1	1.3	V
		$I_C = 100mA$, $I_B = 250\mu A$	2	—	0.9	1.1	V
$I_{IN(ON)}$	Input current						
	Type ULN-2003	$V_{IN} = 3.85V$	3	—	0.93	1.35	mA
	Type ULN-2004	$V_{IN} = 5V$	3	—	0.35	0.5	mA
		$V_{IN} = 12V$	3	—	1.0	1.45	mA
$I_{IN(OFF)}$	Input current	$I_C = 500\mu A$, $T_A = 70°C$	4	50	65	—	μA
$V_{IN(ON)}$	Input voltage						
	Type ULN-2003	$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	2.4	V
		$V_{CE} = 2V$, $I_C = 250mA$	5	—	—	2.7	V
		$V_{CE} = 2V$, $I_C = 300mA$	5	—	—	3.0	V
	Type ULN-2004	$V_{CE} = 2V$, $I_C = 125mA$	5	—	—	5.0	V
		$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	6.0	V
		$V_{CE} = 2V$, $I_C = 275mA$	5	—	—	7.0	V
		$V_{CE} = 2V$, $I_C = 350mA$	5	—	—	8.0	V
h_{FE}	D-C forward current transfer ratio Type ULN-2001	$V_{CE} = 2V$, $I_C = 350mA$	2	1000		—	—
C_{IN}	Input capacitance		—	—	15	30	pF
I_R	Clamp diode leakage current	$V_R = 50V$	6	—	—	50	μA
V_F	Clamp diode forward voltage	$I_F = 350mA$	7	—	1.7	2	V

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.[1,2,3]

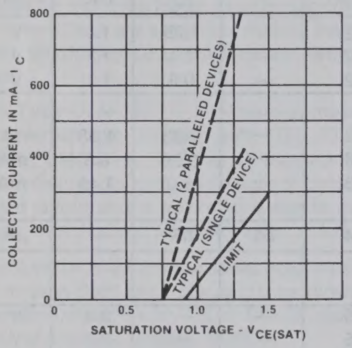
PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
t_{PLH}	Turn-on delay	$0.5\ E_{IN}$ to $0.5\ E_{OUT}$	—	—	1.0	5	μs
t_{PHL}	Turn-off delay	$0.5\ E_{IN}$ to $0.5\ E_{OUT}$	—	—	1.0	5	μs

NOTES

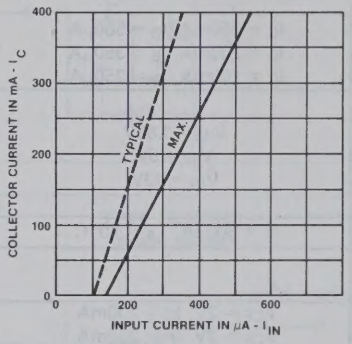
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

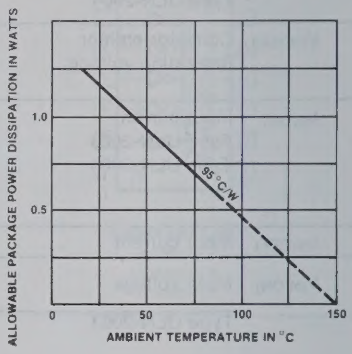
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



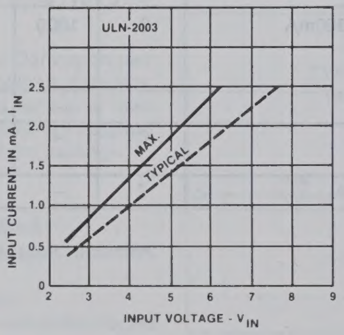
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



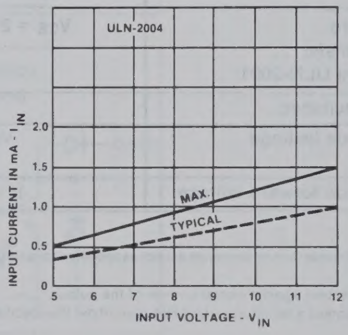
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2003



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2004



TEST FIGURES

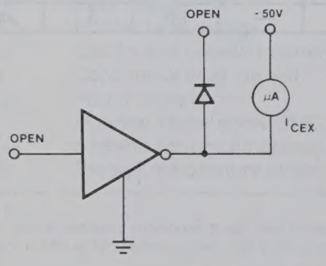

OPEN
-50V
µA
I_{CEX}
OPEN

Figure 1A

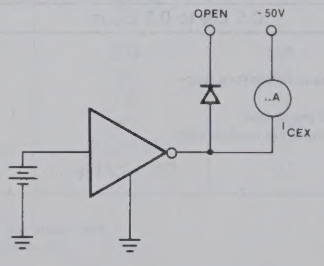

OPEN
-50V
µA
I_{CEX}

Figure 1B

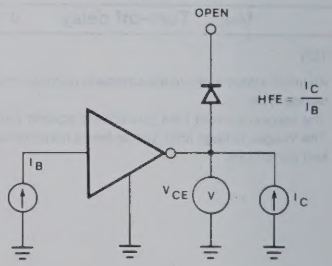

OPEN
HFE = $\frac{I_C}{I_B}$
I_B
V_{CE}
V
I_C

Figure 2

TEST FIGURES (Cont'd)

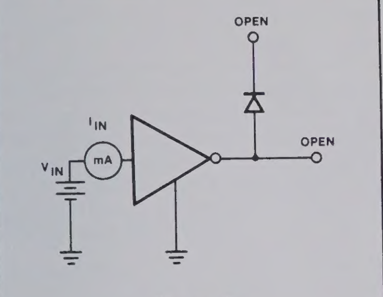

OPEN
I_{IN}
mA
V_{IN}
OPEN

Figure 3

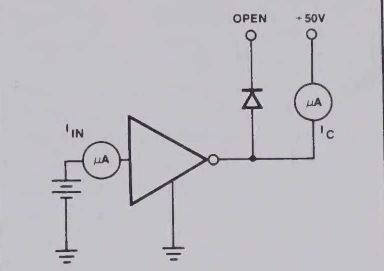

OPEN
+50V
I_{IN}
μA
μA
I_C

Figure 4

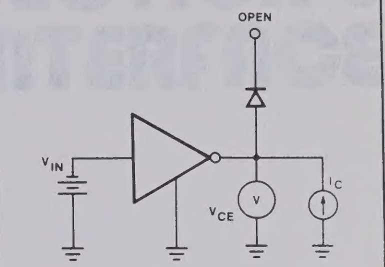

OPEN
V_{IN}
V_{CE}
V
I_C

Figure 5

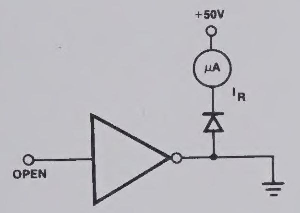

+50V
μA
I_R
OPEN

Figure 6

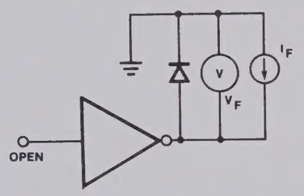
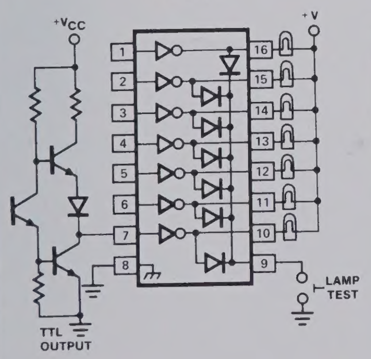


Figure 7

TYPICAL APPLICATIONS

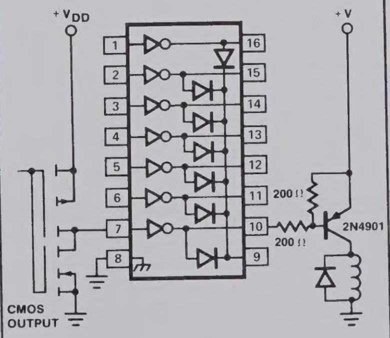
TTL TO LOAD

ULN2003


+V_{CC}
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
LAMP TEST
TTL OUTPUT

BUFFER FOR HIGHER CURRENT LOADS

ULN2004


+V_{DD}
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
200 Ω
200 Ω
2N4901
CMOS OUTPUT

SECTION 8
INTERFACE

Section 8—INTERFACE

DS7820/8820	Dual Line Receiver	243
DS7820A/8820A	Dual Line Receiver	245
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MC1488	Quad Line Driver	251
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75S207	High Speed Dual Sense Amplifier for MOS Memories	263
75S208	High Speed Dual Sense Amplifier for MOS Memories	266

DUAL LINE RECEIVER

DS7820/DS8820

DS7820/8820-F,N

DESCRIPTION

The DS7820, specified from -55°C to 125°C, and the DS8820, specified from 0°C to 70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

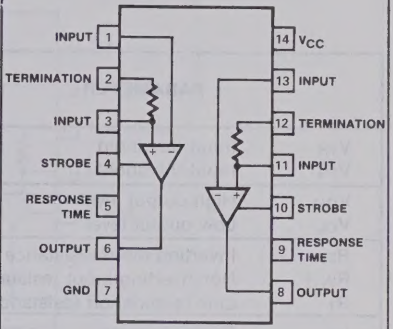
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

FEATURES

- **Operation from a single +5V logic supply**
- **Input voltage range of ±15V**
- **Independent channel strobing**
- **High input resistance**
- **Fanout of two with DTL or TTL**
- **Output can be wire OR'ed**
- **DS7820 Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE

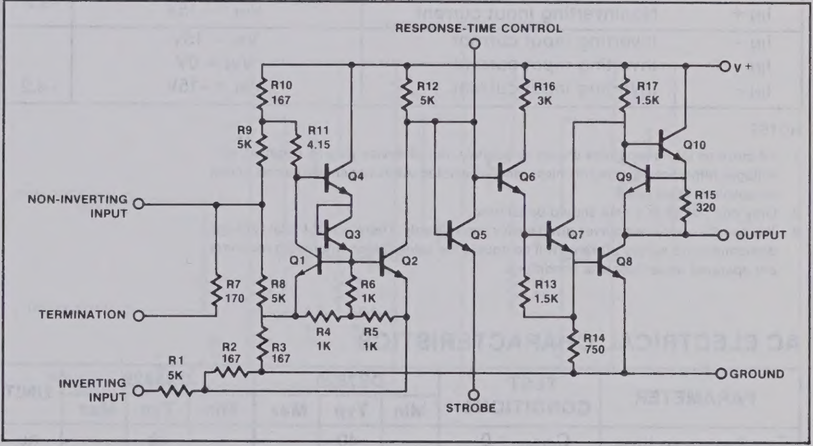


INPUT 1
TERMINATION 2
INPUT 3
STROBE 4
RESPONSE TIME 5
OUTPUT 6
GND 7
8 OUTPUT
9 RESPONSE TIME
10 STROBE
11 INPUT
12 TERMINATION
13 INPUT
14 VCC
+
−

ORDER PART NO.

DS7820N, DS8820N
DS7820F, DS8820F

CIRCUIT SCHEMATIC



RESPONSE-TIME CONTROL
V+
R10 167
R12 5K
R16 3K
R17 1.5K
R9 5K
R11 4.15
Q10
Q4
Q6
Q9
R15 320
NON-INVERTING INPUT
Q3
Q5
Q7
OUTPUT
Q1
Q2
Q8
R7 170
R8 5K
R6 1K
R13 1.5K
TERMINATION
R4 1K
R5 1K
R14 750
R2 167
R3 167
R1 5K
GROUND
INVERTING INPUT
STROBE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	25	mA
Power dissipation	600	mW
Operating temperature range		
DS7820	-55 to +125	°C
DS8820	0 to 70	°C
Lead temperature (soldering, 10sec)	300	°C

NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DS7820/8820-F,N

DC ELECTRICAL CHARACTERISTICS

Specifications apply for 4.5V ≤ V_{CC} ≤ 5.5, -15V ≤ V_{CM} ≤ 15V and -55°C ≤ T_A ≤ +125°C for the DS7820 or 0°C ≤ T_A ≤ +70°C for the DS8820 unless otherwise specified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.[1,2,3]

PARAMETER		TEST CONDITIONS	DS7820			DS8820			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{TH}	Input threshold	V_{IN} = 0V	-0.5	0	0.5	-0.5	0	0.5	V
V_{TH}	Input threshold	-15V ≤ V_{IN} ≤ 15V	-1.0	0	1.0	-1.0	0	1.0	V
V_{OH}	High output level	I_{OUT} ≤ -0.2mA	2.5		5.5	2.5		5.5	V
V_{OL}	Low output level	I_{SINK} ≤ 3.5mA	0		0.4	0		0.4	V
R_{IN} -	Inverting input resistance		3.6	5.0		3.6	5.0		kΩ
R_{IN} +	Noninverting input resistance		1.8	2.5		1.8	2.5		kΩ
R_T	Line termination resistance		120	170	250	120	170	250	Ω
I_{ST}	Strobe current	V_{Strobe} = 0.4V		1.0	1.4		1.0	1.4	mA
I_{ST}	Strobe current	V_{Strobe} = 5.5V			-5			-5	µA
I_{CC}	Supply current[3]	V_{IN} = 15V		3.2	6.0		3.2	6.0	mA
I_{CC}	Supply current[3]	V_{IN} = 0V		5.8	10.2		5.8	10.2	mA
I_{CC}	Supply current[3]	V_{IN} = -15V		8.3	15.0		8.3	15.0	mA
I_{IN} +	Noninverting input current	V_{IN} = 15V		3.0	7.0		5.0	7.0	mA
I_{IN} +	Noninverting input current	V_{IN} = 0V	-1.6	-1.0		-1.6	-1.0		mA
I_{IN} +	Noninverting input current	V_{IN} = -15V	-9.8	-7.0		-9.8	-7.0		mA
I_{IN} -	Inverting input current	V_{IN} = 15V		3.0	4.2		3.0	4.2	mA
I_{IN} -	Inverting input current	V_{IN} = 0V		0	-0.5		0	-0.5	mA
I_{IN} -	Inverting input current	V_{IN} = -15V	-4.2	-3.0		-4.2	-3.0		mA

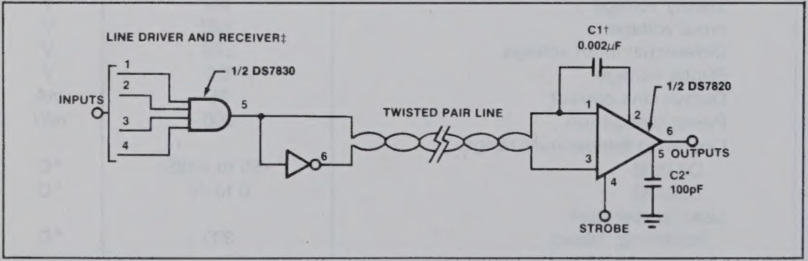
NOTES

1. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
2. Only one output at a time should be shorted.
3. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	DS7820			DS8820			UNIT
			Min	Typ	Max	Min	Typ	Max	
T_R	Response time	C_{delay} = 0		40			40		ns
T_R	Response time	C_{delay} = 100pF		150			150		ns

DS7820-DS8820 TYPICAL APPLICATION



†Exact value depends on line length

‡V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830

*Optional to control response time

N/F

DESCRIPTION

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

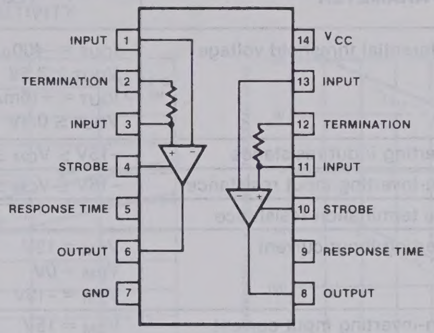
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (-55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

FEATURES

- **Operation from a single +5V logic supply**
- **Input voltage range of ±15V**
- **Strobe low forces output to "1" state**
- **High input resistance**
- **Fanout of ten with either DTL or TTL integrated circuits**
- **Outputs can be wire OR'ed**
- **Series 54/74 compatible**

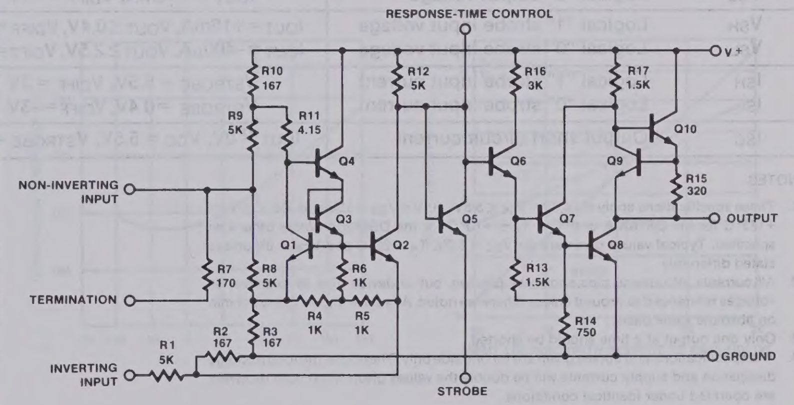
PIN CONFIGURATION

N/F PACKAGE


INPUT 1
TERMINATION 2
INPUT 3
STROBE 4
RESPONSE TIME 5
OUTPUT 6
GND 7
14 VCC
13 INPUT
12 TERMINATION
11 INPUT
10 STROBE
9 RESPONSE TIME
8 OUTPUT

ORDER PART NO.
DS7820AN, DS7820AF
DS8820AN, DS8820AF

EQUIVALENT SCHEMATIC


RESPONSE-TIME CONTROL
V+
R10 167
R12 5K
R16 3K
R17 1.5K
R9 5K
R11 4.15
Q4
Q10
Q6
Q9
R15 320
NON-INVERTING INPUT
Q3
Q5
Q7
OUTPUT
Q1
Q2
Q8
R7 170
R8 5K
R6 1K
R13 1.5K
TERMINATION
R4 1K
R5 1K
R14 750
R2 167
R3 167
R1 5K
GROUND
INVERTING INPUT
STROBE

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	50	mA
Power dissipation	600	mW
Operating temperature range		
DS7820A	-55 to +125	°C
DS8820A	0 to +70	°C
Lead temperature (soldering, 60sec)	300	°C

*NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2,3,4]

	PARAMETER	TEST CONDITIONS	DS7820A/DS8820A			UNIT
			Min	Typ	Max	
V_{TH}	Differential threshold voltage	$I_{OUT} = -400\mu A$ $-3V \le V_{CM} \le +3V$		0.06	0.5	V
		$V_{OUT} \ge 2.5V$ $-15V \le V_{CM} \le +15V$		0.06	1.0	V
		$I_{OUT} = +16mA$ $-3V \le V_{CM} \le +3V$		-0.08	-0.5	V
		$V_{OUT} \le 0.4V$ $-15V \le V_{CM} \le +15V$		-0.08	-1.0	V
R_I^-	Inverting input resistance	$-15V \le V_{CM} \le +15V$	3.6	5		kΩ
R_I^+	Non-inverting input resistance	$-15V \le V_{CM} \le +15V$	1.8	2.5		kΩ
R_T	Line termination resistance		120	170	250	Ω
I_I^-	Inverting input current	$V_{CM} = 15V$		3.0	4.2	mA
		$V_{CM} = 0V$		0	-0.5	mA
		$V_{CM} = -15V$		-3.0	-4.2	mA
I_I^+	Non-inverting input current	$V_{CM} = 15V$		5.0	7.0	mA
		$V_{CM} = 0V$		-1.0	-1.6	mA
		$V_{CM} = -15V$		-7.0	-9.8	mA
I_{CC}	Power supply current	$V_{DIFF} = -1V$, $V_{CM} = 15V$		3.9	6.0	mA
		$I_{OUT} =$ Logical "0" $V_{CM} = -15V$		9.2	14.0	mA
		$V_{DIFF} = -0.5V$, $V_{CM} = 0V$		6.5	10.2	mA
V_{OH}	Logical "1" output voltage	$I_{OUT} = -400\mu A$, $V_{DIFF} = 1V$	2.5	4.0	5.5	V
V_{OL}	Logical "0" output voltage	$I_{OUT} = +16mA$, $V_{DIFF} = -1V$	0	0.22	0.4	V
V_{SH}	Logical "1" strobe input voltage	$I_{OUT} = +16mA$, $V_{OUT} \le 0.4V$, $V_{DIFF} = -3V$	2.1			V
V_{SL}	Logical "0" strobe input voltage	$I_{OUT} = -400\mu A$, $V_{OUT} \ge 2.5V$, $V_{DIFF} = -3V$			0.9	V
I_{SH}	Logical "1" strobe input current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$		0.01	5.0	μA
I_{SL}	Logical "0" strobe input current	$V_{STROBE} = 0.4V$, $V_{DIFF} = -3V$		-1.0	-1.4	mA
I_{SC}	Output short circuit current	$I_{OUT} = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$	-2.8	-4.5	-6.7	mA

NOTES

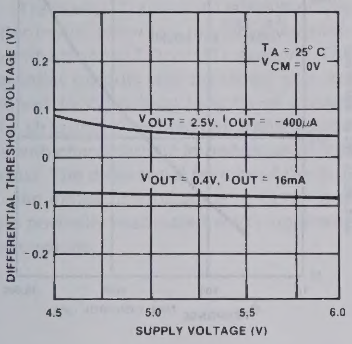
1. These specifications apply for $4.5V \le V_{CC} \le 5.5V$, $-15V \le V_{CM} \le 15V$ and $-55°C \le T_A \le +125°C$ for the DS7820A or $0°C \le T_A \le +70°C$ for the DS8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
3. Only one output at a time should be shorted.
4. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

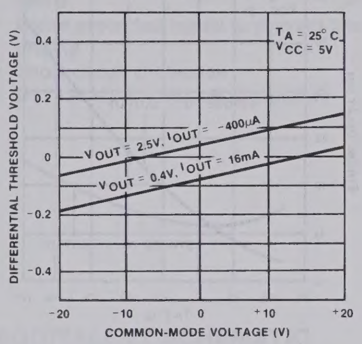
	PARAMETER	TEST CONDITIONS	DS7820A/DS8820A			UNIT
			Min	Typ	Max	
t_{PD0}	Propagation delay, differential input to "0" output			30	45	ns
t_{PD1}	Propagation delay, differential input to "1" output			27	40	ns
t_{PD0}	Propagation delay, strobe input to "0" output			16	25	ns
t_{PD1}	Propagation delay, strobe input to "1" output			18	30	ns

TYPICAL PERFORMANCE CHARACTERISTICS

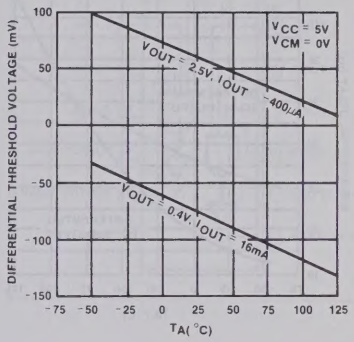
SUPPLY VOLTAGE SENSITIVITY



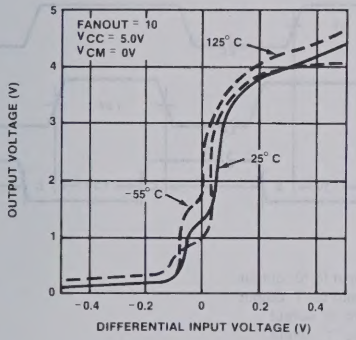
COMMON-MODE VOLTAGE SENSITIVITY



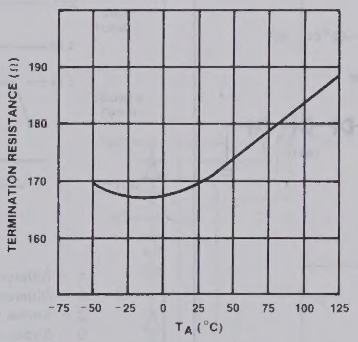
TEMPERATURE SENSITIVITY



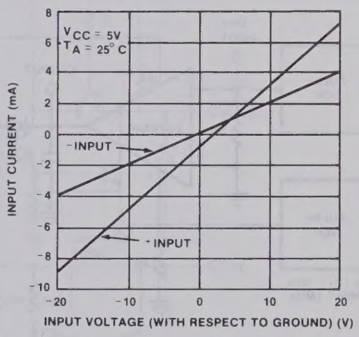
TRANSFER FUNCTION



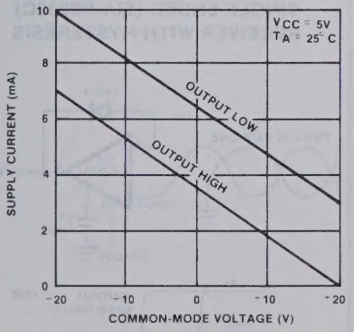
TERMINATION RESISTANCE



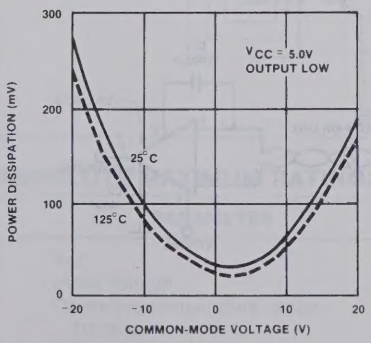
INPUT CHARACTERISTICS



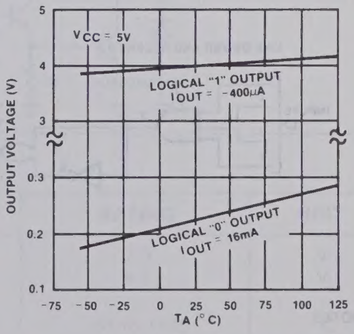
POWER SUPPLY CURRENT



INTERNAL POWER DISSIPATION

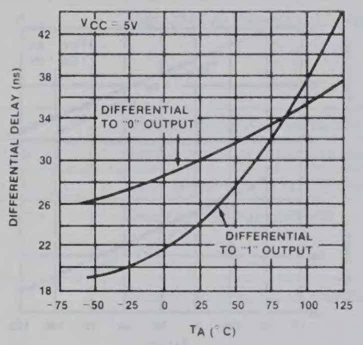


OUTPUT VOLTAGE LEVELS

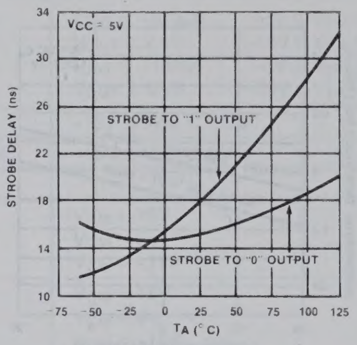


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

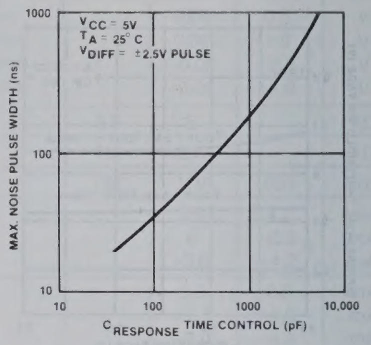
DIFFERENTIAL INPUT DELAYS



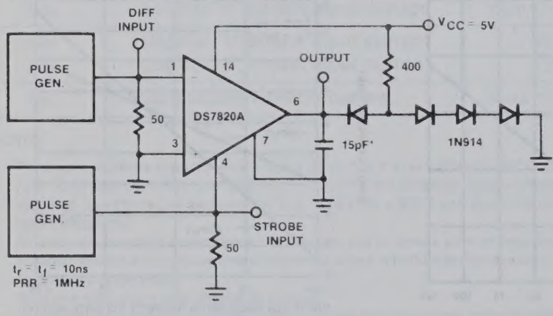
STROBE DELAYS



NOISE REJECTION

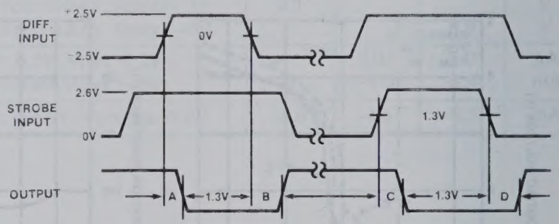


AC TEST CIRCUIT


DIFF INPUT
PULSE GEN.
50
1
3
14
DS7820A
4
7
6
OUTPUT
VCC = 5V
400
15pF*
1N914
PULSE GEN.
STROBE INPUT
50
tr = tf = 10ns
PRR = 1MHz

*Includes Jig and Probe

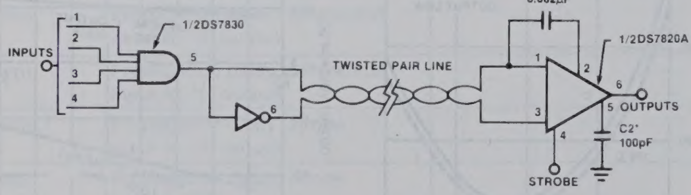
VOLTAGE WAVEFORM


DIFF. INPUT
+2.5V
0V
-2.5V
STROBE INPUT
2.6V
0V
1.3V
OUTPUT
A
1.3V
B
C
1.3V
D

A = Differential input to "0" output
B = Differential input to "1" output
C = Strobe input to "0" output
D = Strobe input to "1" output

TYPICAL APPLICATIONS

LINE DRIVER AND RECEIVER‡


1/2DS7830
INPUTS
1
2
3
4
5
6
TWISTED PAIR LINE
C1†
0.002μF
1/2DS7820A
1
2
3
4
6
5
OUTPUTS
C2*
100pF
STROBE

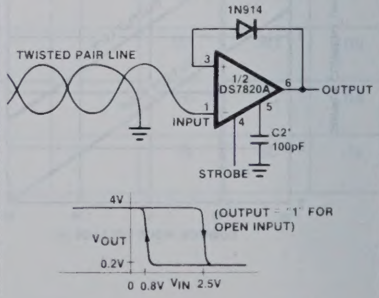
NOTES

†Exact value depends on line length

‡VCC is 4.5V to 5.5V for both the DS7820 and DS7830

*Optional to control response time

SINGLE ENDED (EIA-RS232C) RECEIVER WITH HYSTERESIS


1N914
TWISTED PAIR LINE
3
1/2 DS7820A
6
OUTPUT
1
INPUT
4
5
C2*
100pF
STROBE
4V
VOUT
0.2V
(OUTPUT = "1" FOR OPEN INPUT)
0 0.8V VIN 2.5V

DUAL DIFFERENTIAL LINE DRIVER DS7830/DS8830

DS7830/8830-F,N

DESCRIPTION

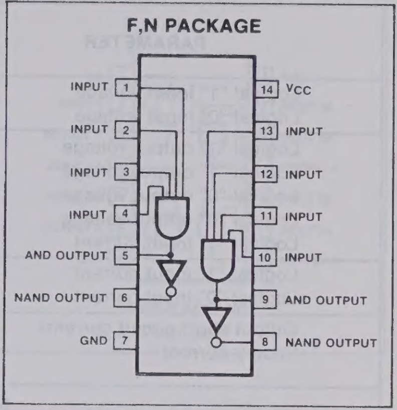
The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

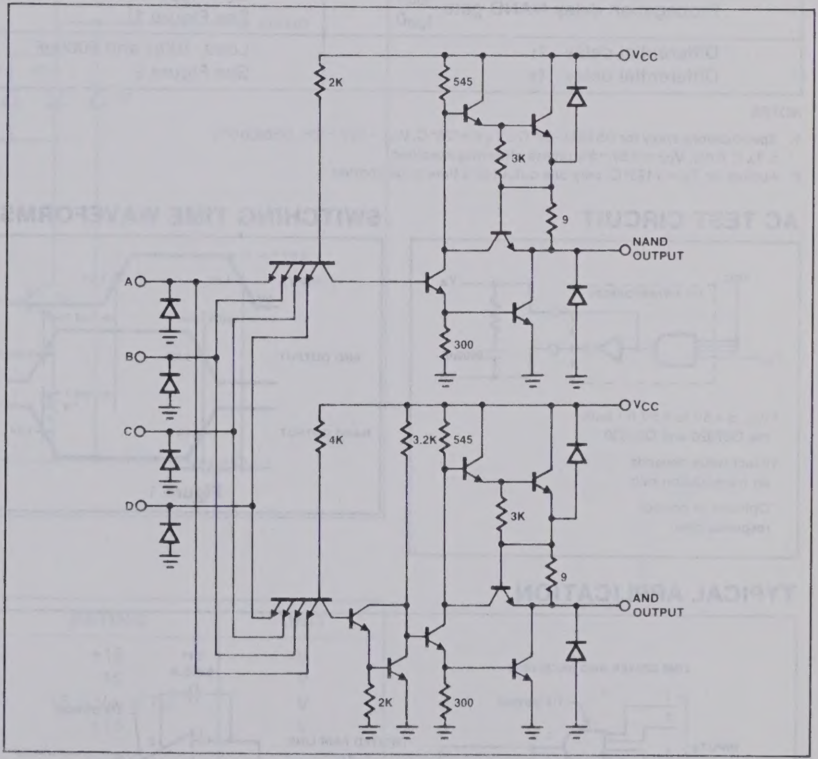
FEATURES

- Single 5 volt power supply
- High speed
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- Short circuit protection
- DS7830 Mil std 883A,B,C available

PIN CONFIGURATION


F,N PACKAGE
INPUT 1
INPUT 2
INPUT 3
INPUT 4
AND OUTPUT 5
NAND OUTPUT 6
GND 7
14 VCC
13 INPUT
12 INPUT
11 INPUT
10 INPUT
9 AND OUTPUT
8 NAND OUTPUT

EQUIVALENT SCHEMATIC


VCC
2K
545
3K
9
NAND OUTPUT
A
B
C
D
300
VCC
4K
3.2K
545
3K
9
AND OUTPUT
2K
300

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC}	7.0	V
Input voltage	5.5	V
Operating temperature range		
DS7830	-55 to +125	°C
DS8830	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DS7830/8830-F,N

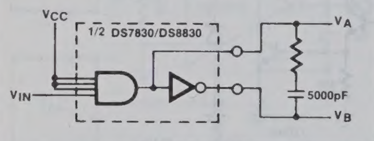
ELECTRICAL CHARACTERISTICS $T_A = 25°C$ $V_{CC} = 5V$ unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Logical "1" input voltage		2.0			V
Logical "0" input voltage				0.8	V
Logical "1" output voltage	$V_{IN} = 0.8V$ $I_{OUT} = -0.8mA$	2.4			V
Logical "1" output voltage	$V_{IN} = 0.8V$ $I_{OUT} = -40mA$	1.8	2.9		V
Logical "0" output voltage	$V_{IN} = 2.0V$ $I_{OUT} = +32mA$		0.2	0.4	V
Logical "0" output voltage	$V_{IN} = 2.0V$ $I_{OUT} = +40mA$		0.22	0.5	V
Logical "1" input current	$V_{IN} = +2.4V$			120	μA
Logical "1" input current	$V_{IN} = 5.5V$			2	mA
Logical "0" input current	$V_{IN} = 0.4V$			4.8	mA
Output short circuit current[2]	$V_{CC} = 5.0V$	-40	-100	-120	mA
Supply current	$V_{CC} = 5.0V$ $V_{IN} = 5.0V$ (Each driver)		11	18	mA
Propagation delay AND gate $t_{pd}1$	$T_A = 25°C$		8	12	ns
Propagation delay AND gate $t_{pd}0$	$V_{CC} = 5.0V$		11	18	ns
Propagation delay NAND gate $t_{pd}1$	$C_L = 15pF$		8	12	ns
Propagation delay NAND gate $t_{pd}0$	See Figure 1		5	8	ns
Differential delay t_1	Load, 100Ω and 5000pF		12	16	ns
Differential delay t_2	See Figure 2		12	16	ns

NOTES

1. Specifications apply for DS7830 $-55°C \le T_A \le +125°C$, $V_{CC} = +5V \pm 10\%$, DS8830 $0°C \le T_A \le 70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified.
2. Applies for $T_A = +125°C$, only one output at a time to be shorted.

AC TEST CIRCUIT


VCC
1/2 DS7830/DS8830
VA
VIN
5000pF
VB

†V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830

†Exact value depends on transmission rate

*Optional to control response time

SWITCHING TIME WAVEFORMS

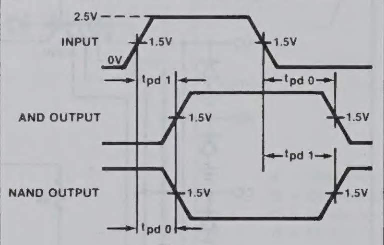

2.5V
INPUT
0V
1.5V
1.5V
tpd 1
tpd 0
AND OUTPUT
1.5V
1.5V
tpd 1
NAND OUTPUT
1.5V
1.5V
tpd 0

Figure 1

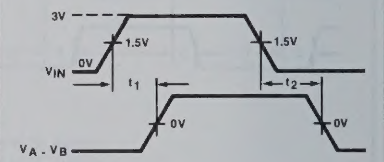
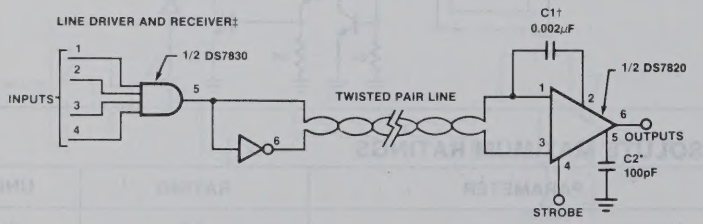

3V
1.5V
1.5V
VIN
0V
t1
t2
0V
0V
VA - VB

Figure 2

TYPICAL APPLICATION


LINE DRIVER AND RECEIVER‡
1
2
3
4
INPUTS
1/2 DS7830
5
6
TWISTED PAIR LINE
C1†
0.002μF
1/2 DS7820
1
2
3
4
5
6
OUTPUTS
C2*
100pF
STROBE

†Exact value depends on line length

‡V_{CC} is 4.5V to 5.5V for the DS7820 and DS7830

*Optional to control response time

QUAD LINE DRIVER MC1488

MC1488-F,N

DESCRIPTION

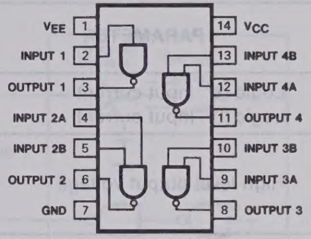
The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES

- **Current limited output: ±10mA Typ**
- **Power-off source impedance: 300Ω Min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

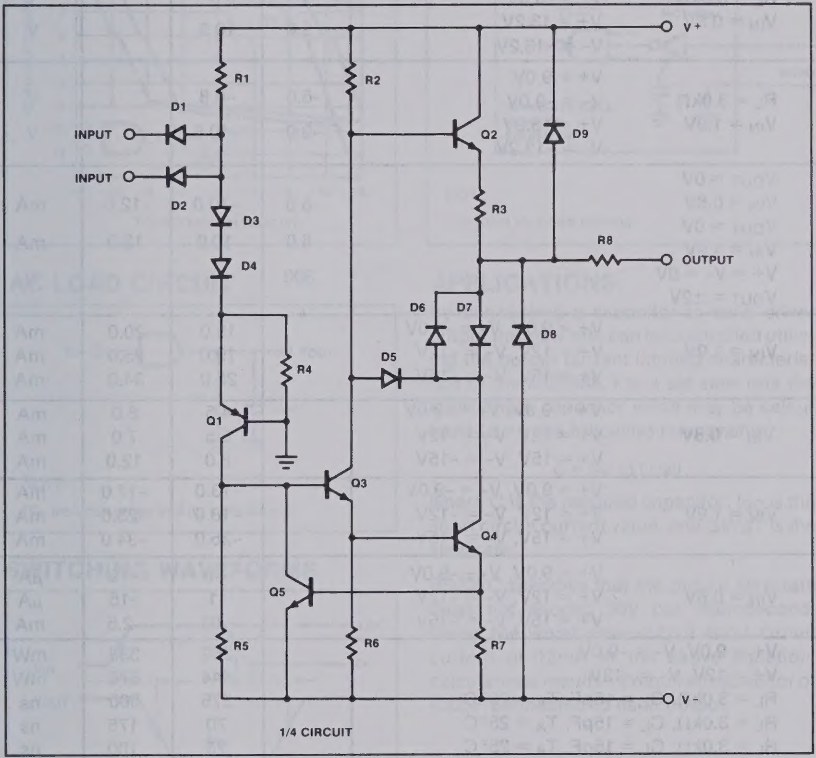
PIN CONFIGURATION

F,N PACKAGE


VEE 1
INPUT 1 2
OUTPUT 1 3
INPUT 2A 4
INPUT 2B 5
OUTPUT 2 6
GND 7
14 VCC
13 INPUT 4B
12 INPUT 4A
11 OUTPUT 4
10 INPUT 3B
9 INPUT 3A
8 OUTPUT 3

ORDER PART NO.
MC1488N/F

CIRCUIT SCHEMATIC


V+
R1
R2
D1
INPUT
INPUT
D2
D3
D4
Q2
D9
R3
R8
OUTPUT
D6
D7
D8
D5
R4
Q1
Q3
Q4
Q5
R5
R6
R7
V-
1/4 CIRCUIT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V_{IN})	$-15 \leq V_{IN} \leq 7.0$	V
Output voltage	±15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS

$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$ unless otherwise specified.
All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$.*

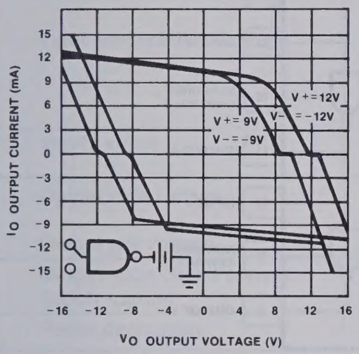
PARAMETER	TEST CONDITIONS		LIMITS			UNIT
			Min	Typ	Max	
Logic "0" input current	$V_{IN} = 0V$			-1.0	-1.6	mA
Logic "1" input current	$V_{IN} = +5.0V$			.005	10.0	μA
High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	$V+ = 9.0V$ $V- = -9.0V$	6.0	7.0		V
		$V+ = 13.2V$ $V- = -13.2V$	9.0	10.5		V
Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	$V+ = 9.0V$ $V- = -9.0V$	-6.0	-6.8		V
		$V+ = 13.2V$ $V- = -13.2V$	-9.0	-10.5		V
High level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		-6.0	-10.0	-12.0	mA
Low level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
Output resistance	$V+ = V- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
Positive supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		15.0	20.0	mA
		$V+ = 12V$, $V- = -12V$		19.0	25.0	mA
		$V+ = 15V$, $V- = -15V$		25.0	34.0	mA
	$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		4.5	6.0	mA
		$V+ = 12V$, $V- = -12V$		5.5	7.0	mA
		$V+ = 15V$, $V- = -15V$		8.0	12.0	mA
Negative supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V$, $V- = -9.0V$		-13.0	-17.0	mA
		$V+ = 12V$, $V- = -12V$		-18.0	-23.0	mA
		$V+ = 15V$, $V- = -15V$		-25.0	-34.0	mA
	$V_{IN} = 0.8V$	$V+ = 9.0V$, $V- = -9.0V$		-1	-15	μA
		$V+ = 12V$, $V- = -12V$		-1	-15	μA
		$V+ = 15V$, $V- = -15V$		-.01	-2.5	mA
Power dissipation	$V+ = 9.0V$, $V- = -9.0V$			252	333	mW
	$V+ = 12V$, $V- = -12V$			444	576	mW
Propagation delay to "1" (t_{pd1})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
Propagation delay to "0" (t_{pd0})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
Rise time (t_r)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
Fall time (t_f)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

NOTE

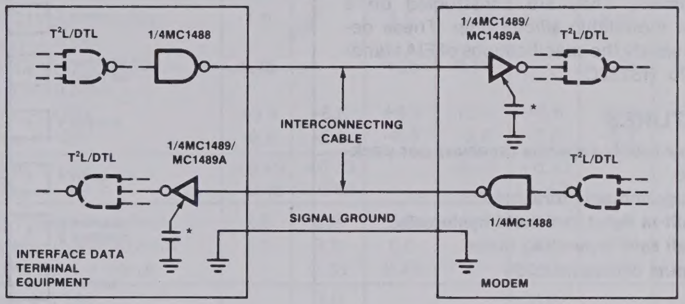
*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



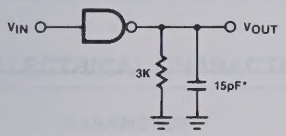
RS232C DATA TRANSMISSION


T²L/DTL
1/4MC1488
1/4MC1489/
MC1489A
T²L/DTL
*
INTERCONNECTING
CABLE
T²L/DTL
1/4MC1489/
MC1489A
*
T²L/DTL
SIGNAL GROUND
1/4MC1488
INTERFACE DATA
TERMINAL
EQUIPMENT
MODEM

NOTE

*Optional for noise filtering

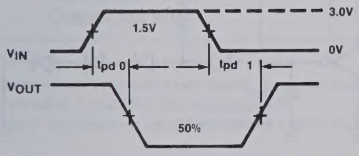
AC LOAD CIRCUIT


VIN
VOUT
3K
15pF*

NOTE

*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS


3.0V
1.5V
VIN
0V
tpd 0
tpd 1
VOUT
50%

NOTE

t_r and t_f are measured between 10% and 90% of the output waveform

APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

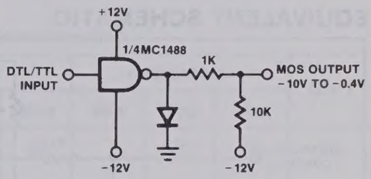
$$C = I_{SC}\ (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

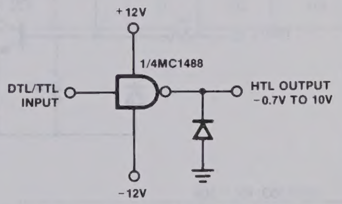
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS

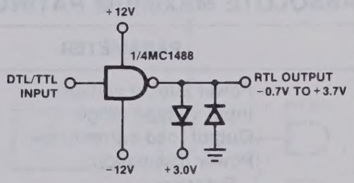
DTL/TTL-TO-MOS TRANSLATOR


+12V
1/4MC1488
DTL/TTL
INPUT
1K
MOS OUTPUT
-10V TO -0.4V
10K
-12V
-12V

DTL/TTL-TO-HTL TRANSLATOR


+12V
1/4MC1488
DTL/TTL
INPUT
HTL OUTPUT
-0.7V TO 10V
-12V

DTL/TTL-TO-RTL TRANSLATOR


+12V
1/4MC1488
DTL/TTL
INPUT
RTL OUTPUT
-0.7V TO +3.7V
-12V
+3.0V

QUAD LINE RECEIVERS MC1489/MC1489A

DESCRIPTION

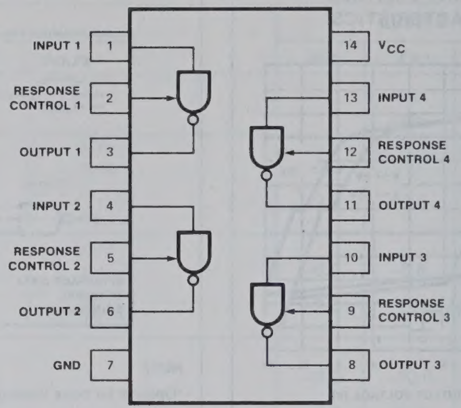
The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

FEATURES

- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

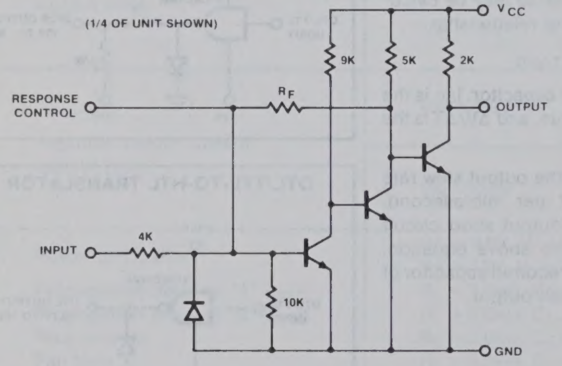
PIN CONFIGURATION

F,N PACKAGE


INPUT 1
1
RESPONSE CONTROL 1
2
OUTPUT 1
3
INPUT 2
4
RESPONSE CONTROL 2
5
OUTPUT 2
6
GND
7
14
V_{CC}
13
INPUT 4
12
RESPONSE CONTROL 4
11
OUTPUT 4
10
INPUT 3
9
RESPONSE CONTROL 3
8
OUTPUT 3

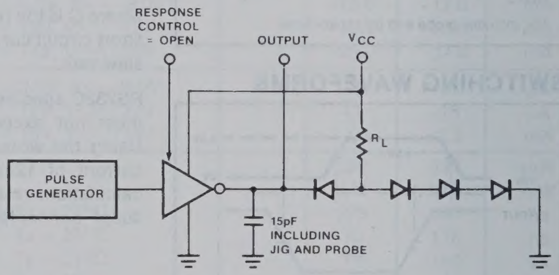
ORDER PART NO.
MC1489F/MC1489AF/MC1489N/MC1489AN

EQUIVALENT SCHEMATIC


(1/4 OF UNIT SHOWN)
V_{CC}
9K
5K
2K
RESPONSE CONTROL
R_F
OUTPUT
INPUT
4K
10K
GND

MC1489: R_F = 10k
MC1489A: R_F = 2k

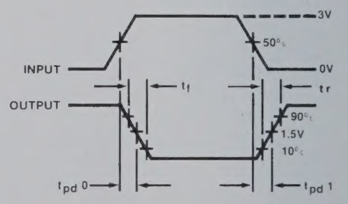
AC TEST CIRCUIT


RESPONSE CONTROL = OPEN
OUTPUT
V_{CC}
R_L
PULSE GENERATOR
15pF INCLUDING JIG AND PROBE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	±30	V
Output load current	20	mA
Power dissipation:		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C

VOLTAGE WAVEFORMS


3V
50%
INPUT
0V
t_f
t_r
OUTPUT
90%
1.5V
10%
t_{pd} 0
t_{pd} 1

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $0°C \leq T_A \leq +75°C$ unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489 Min	MC1489 Typ	MC1489 Max	MC1489A Min	MC1489A Typ	MC1489A Max	UNIT
Input high threshold voltage	$T_A = 25°C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10mA$	1.0		1.5	1.75		2.25	V
Input low threshold voltage	$T_A = 25°C$, $V_{OUT} \leq 2.5V$, $I_{OUT} = -0.5mA$	0.75		1.25	0.75		1.25	V
	$V_{IN} = +25V$	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	$V_{IN} = -25V$	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	
Input current	$V_{IN} = +3V$	+0.43	+0.53		+0.43	+0.53		mA
	$V_{IN} = -3V$	-0.43	-0.53		-0.43	-0.53		
Output high voltage	$V_{IN} = 0.75V$, $I_{OUT} = -0.5mA$	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, $I_{OUT} = -0.5mA$	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10mA$		0.33	0.45		0.33	0.45	V
Output short circuit current	$V_{IN} = 0.75V$		3.0			3.0		mA
Supply current	$V_{IN} = 5.0V$		20	26		20	26	mA
Power dissipation	$V_{IN} = 5.0V$		100	130		100	130	mW

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $T_A = 25°C$ unless otherwise specified.[1,2]

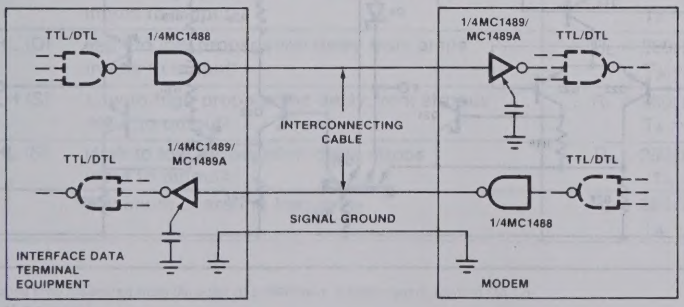
PARAMETER	TEST CONDITIONS	MC1489 Min	MC1489 Typ	MC1489 Max	MC1489A Min	MC1489A Typ	MC1489A Max	UNIT
Input to output "high" Propagation delay (t_{pd1})	$R_L = 3.9k\Omega$ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	$R_L = 390\Omega$ (AC test circuit)		20	50		20	50	ns
Output rise time	$R_L = 3.9k\Omega$ (AC test circuit)		110	175		110	175	ns
Output fall time	$R_L = 390\Omega$ (AC test circuit)		9	20		9	20	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

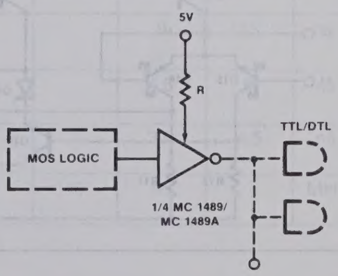
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION


TTL/DTL
1/4MC1488
1/4MC1489/
MC1489A
TTL/DTL
INTERCONNECTING
CABLE
TTL/DTL
1/4MC1489/
MC1489A
TTL/DTL
SIGNAL GROUND
1/4MC1488
INTERFACE DATA
TERMINAL
EQUIPMENT
MODEM

*Optional for noise filtering

MOS TO TTL/DTL TRANSLATOR


5V
R
TTL/DTL
MOS LOGIC
1/4 MC 1489/
MC 1489A

DESCRIPTION

The 75S107 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75107A. If features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S107 maintains ±3V common mode voltage range, 7.5mV input offset voltage and 5μA offset current. It also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe/gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

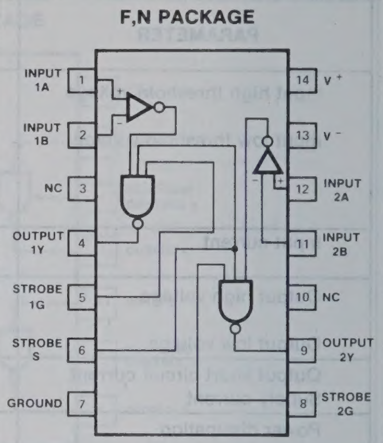
FEATURES

- **Functionally equivalent and pin compatible to SN75107A**
- **17ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **STTL compatible strobes and outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

APPLICATIONS

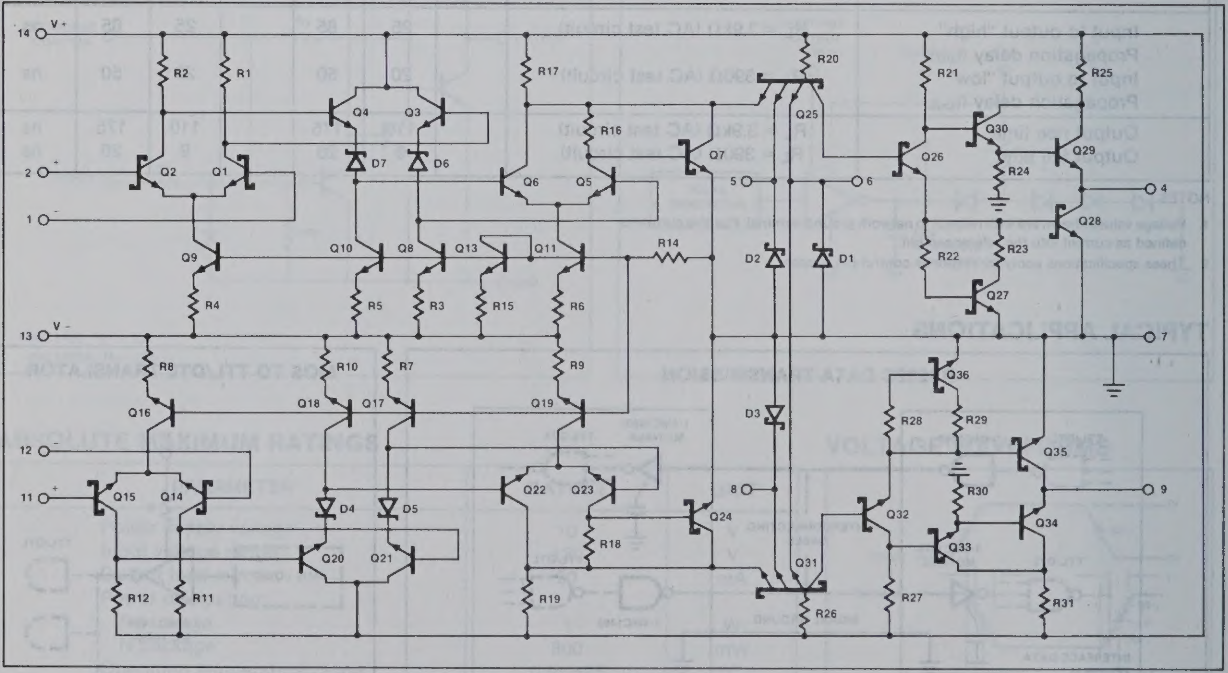
- **MOS memory sense amp**
- **A/D conversion**
- **High speed line receiver**

PIN CONFIGURATION


F,N PACKAGE
INPUT 1A
1
INPUT 1B
2
NC
3
OUTPUT 1Y
4
STROBE 1G
5
STROBE S
6
GROUND
7
14
V+
13
V−
12
INPUT 2A
11
INPUT 2B
10
NC
9
OUTPUT 2Y
8
STROBE 2G
+
−

ORDER PART NO.
75S107F
75S107N

EQUIVALENT SCHEMATIC


14 V+
2
1
13 V−
12
11
R1
R2
Q1
Q2
Q3
Q4
D6
D7
Q5
Q6
R17
R16
Q7
Q25
R20
5
6
Q26
R21
Q30
R25
Q29
R24
4
Q28
R22
R23
Q27
7
Q9
R4
Q10
Q8
Q13
Q11
R5
R3
R15
R6
R14
D2
D1
R8
R10
R7
R9
Q16
Q18
Q17
Q19
D3
Q36
R28
R29
Q35
Q15
Q14
D4
D5
Q22
Q23
8
Q24
R30
9
Q32
Q34
Q20
Q21
R18
Q33
Q31
R12
R11
R19
R26
R27
R31

ELECTRICAL CHARACTERISTICS

T_A = 0 to +70°C, V+ = +5.00, V- = -5.00 unless otherwise specified.

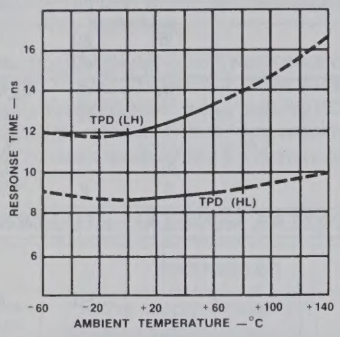
PARAMETER		TEST CONDITIONS	75S107			UNIT
			Min	Typ	Max	
AMPLIFIER INPUT						
	Input offset voltage	V+ = 4.75, V- = -4.75			25	mV
	Input bias current @ 25°C	V+ = 5.25, V- = -5.25		7.5	20	μA
	over temp. range	V+ = 5.25, V- = -5.25			40	μA
	Input offset current @ 25°C	V+ = 5.25, V- = -5.25		1.0	5	μA
	over temp. range	V+ = 5.25, V- = -5.25			12	μA
	Input common mode voltage range	V+ = 4.75, V- = -4.75	±3			V
	Input resistance			4		kΩ
	Input capacitance			3	6	pF
	Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS						
I_{IH}	High level input current into 1G or 2G strobe	V+ = 5.25, V- = -5.25				
		V_{IH} = 2.7V			50	μA
		V_{IH} = 5.25V			1	mA
I_{IH}	High level input current into common strobe S	V+ = 5.25, V- = -5.25				
		V_{IH} = 2.7V			100	μA
		V_{IH} = 5.25V			2	mA
I_{IL}	Low level input current into 1G or 2G	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-2.0	mA
I_{IL}	Low level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-4.0	mA
V_{OH}	High level output voltage	V+ = 4.75V, $V_{I(S)}$ = 2.0V V- = -4.75V I_{LOAD} = -1mA	2.7	3.4		V
V_{OL}	Low level output voltage	V+ = 4.75 V- = -4.75 I_{LOAD} = 20mA $V_{I(S)}$ = 2.0V			0.5	V
POWER SUPPLY REQUIREMENTS						
	Supply voltage					
V+			4.75	5.00	5.25	V
V-			-4.75	-5.00	-5.25	V
I_{CC}+	Supply current	V+ = 5.25V		20	30	mA
I_{CC}-		V- = -5.25V T_A = 25°C		-11	-15	mA
I_{OS}	Short circuit output current	V+ = +5.25 V- = -5.25	-40		-100	mA
LARGE SIGNAL SWITCHING SPEED						
T_pLH (D)	Low to high propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		12	17	ns
T_pHL (D)	High to low propagation delay from amps inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		9	13	ns
T_pLH (S)	Low to high propagation delay from strobes input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		4.5	6	ns
T_pHL (S)	High to low propagation delay strobe input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		3.0	4.5	ns
	Maximum operating frequency	R_L = 280Ω C_L = 15pF T_A = 25°C	40	55		MHz

NOTES

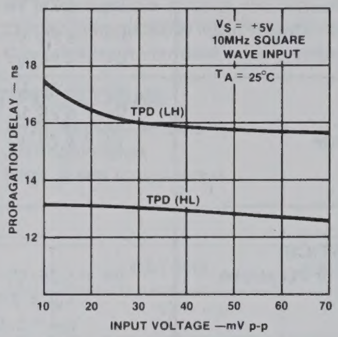
1. Response time measured from 0V point of ±100mV_{P-P} 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point to input to 1.5V point of output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

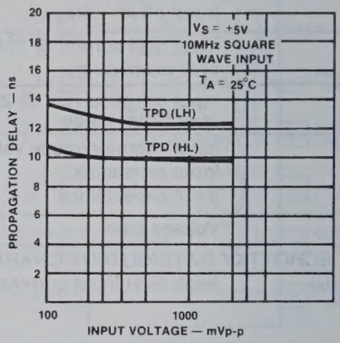
RESPONSE TIME vs TEMPERATURE



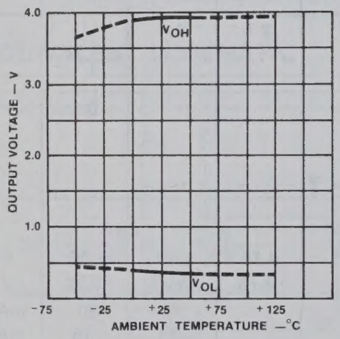
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



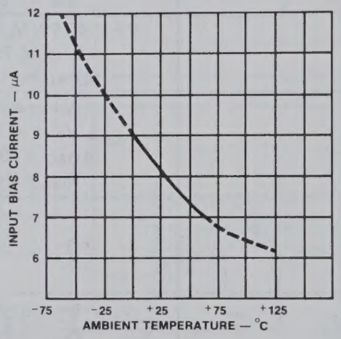
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



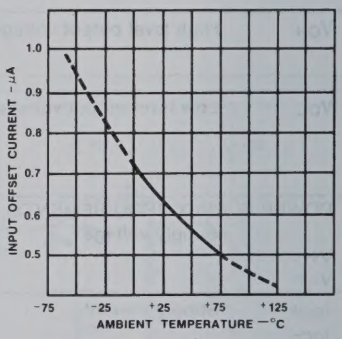
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



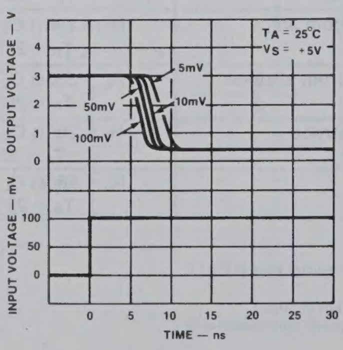
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



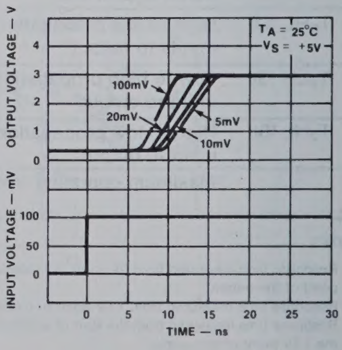
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



HIGH SPEED DUAL LINE RECEIVER 75S108

75S108-F,N

DESCRIPTION

The 75S108 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75108N. It features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S108 maintains ±3V common mode voltage range, 7.5mV input offset voltage and 5μA offset current. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

FEATURES

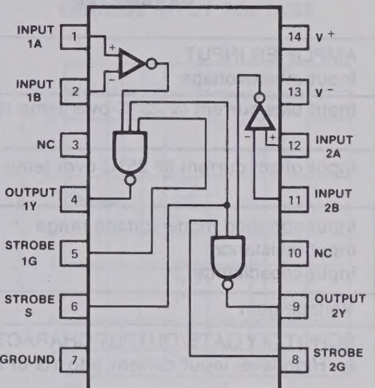
- **Functionally equivalent and pin compatible to SN75108A**
- **17ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL compatible strobes and outputs**
- **Open collector outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

APPLICATIONS

- **High speed line receiver**
- **MOS memory sense amp**
- **A/D conversion**

PIN CONFIGURATION

F,N PACKAGE



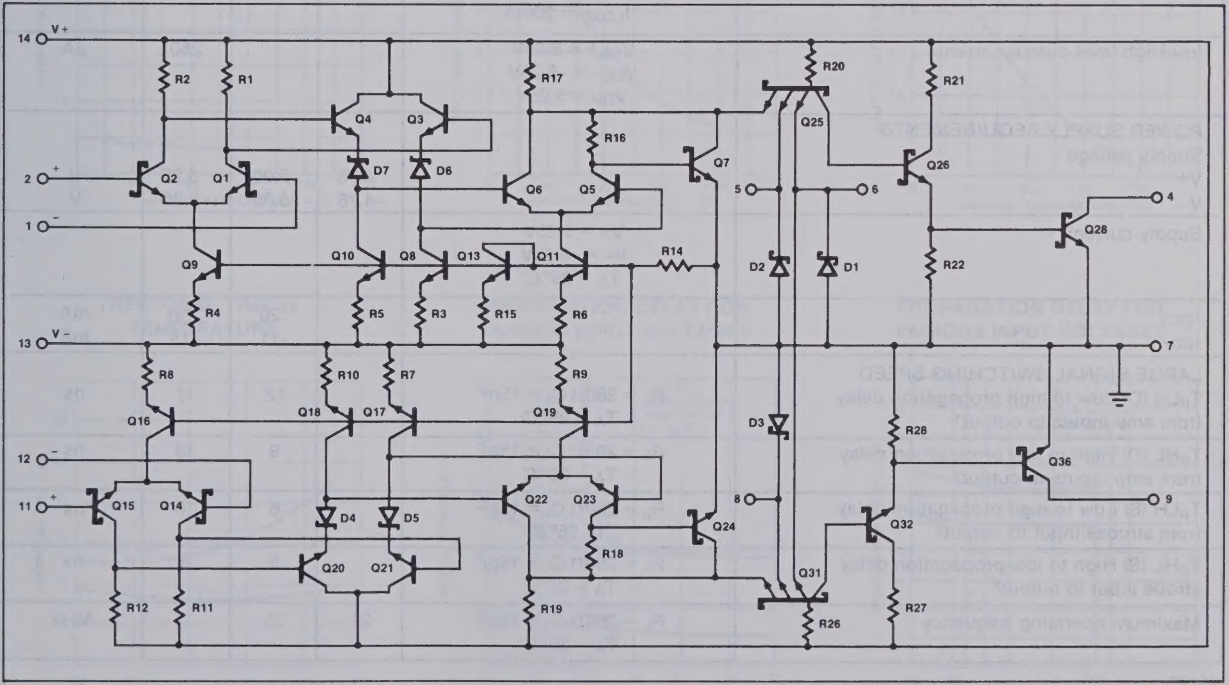
INPUT 1A
1
INPUT 1B
2
NC
3
OUTPUT 1Y
4
STROBE 1G
5
STROBE S
6
GROUND
7
14
V +
13
V −
12
INPUT 2A
11
INPUT 2B
10
NC
9
OUTPUT 2Y
8
STROBE 2G
+
−

ORDER PART NO.
75S108F
75S108N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V−)	−7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature range	0 to 70	°C
Storage temperature range	−65 to +150	°C
Lead temperature (soldering 60 sec)	+300	°C

EQUIVALENT SCHEMATIC



14
V+
2
+
1
−
13
V −
12
−
11
+
5
6
8
4
7
9
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R14
R15
R16
R17
R18
R19
R20
R21
R22
R26
R27
R28
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q28
Q31
Q32
Q36
D1
D2
D3
D4
D5
D6
D7

ELECTRICAL CHARACTERISTICS

T_A = 0 to 70°C, V+ = +5.00, V- = -5.00 unless otherwise specified.

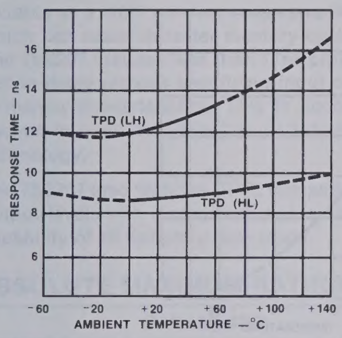
PARAMETER	TEST CONDITIONS	75S108			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT Input offset voltage	V+ = 4.75, V- = -4.75			25	mV
Input bias current @ 25°C over temp range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		7.5	20 40	μA μA
Input offset current @ 25°C over temp range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		1.0	5 12	μA μA
Input common mode voltage range	V+ = 4.75, V- = -4.75	±3		±3	V
Input resistance			4		kΩ
Input capacitance			3	6	pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS I_{IH} High level input current into 1G or 2G strobe	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.25V			50 1	μA mA
I_{IH} High level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.25V			100 2	μA mA
I_{IL} Low level input current into 1G or 2G	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-2.0	mA
I_{IL} Low level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-4.0	mA
V_{OL} Low level output voltage	V+ = 4.75, $V_{I\ (S)}$ = 2.0V V- = -4.75 I_{LOAD} = 20mA			0.5	V
I_{OH} High level output current	V_{CC}+ = 5.25V V_{CC}- = -5.25V V_{OH} = 5.25V			250	μA
POWER SUPPLY REQUIREMENTS Supply voltage V+ V-		4.75 -4.75	5.00 -5.00	5.25 -5.25	V V
Supply current	V+ = 5.25V V- = -5.25V T_A = 25°C				
I_{CC}+ I_{CC}-			20 -11	30 -15	mA mA
LARGE SIGNAL SWITCHING SPEED T_pLH (D) Low to high propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		12	17	ns
T_pHL (D) High to low propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		9	13	ns
T_pLH (S) Low to high propagation delay from strobes input to output[2]	R_L = 280Ω C_L = 15pF T_A 25°C		6	10	ns
T_pHL (S) High to low propagation delay strobe input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		5	8	ns
Maximum operating frequency	R_L = 280Ω C_L = 15pF T_A = 25°C	25	35		MHz

NOTES:

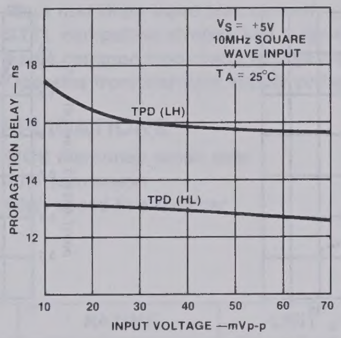
1. Response time measured from 0V point of ±100 mV_{P-P} 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

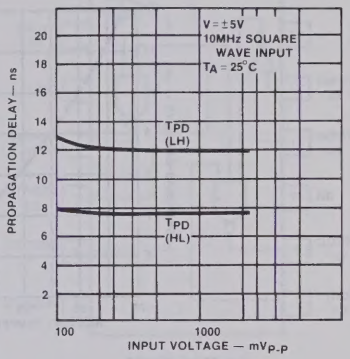
RESPONSE TIME vs TEMPERATURE



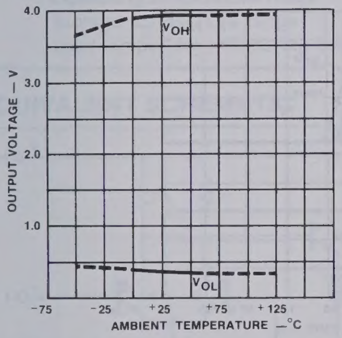
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



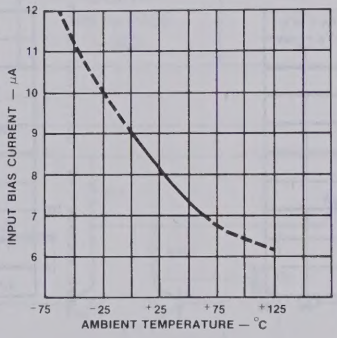
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



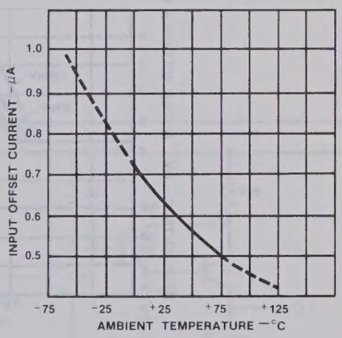
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



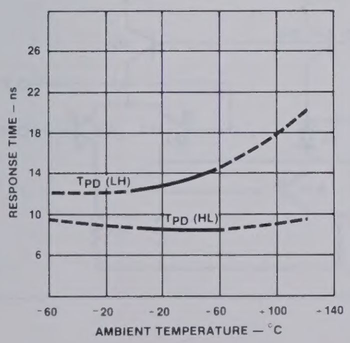
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



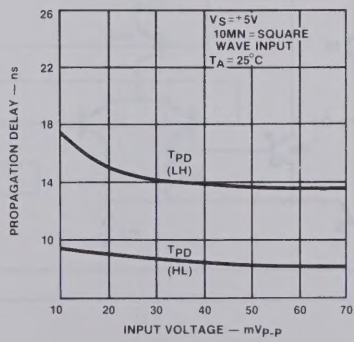
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



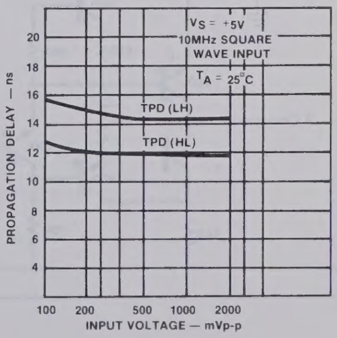
RESPONSE TIME vs TEMPERATURE



PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

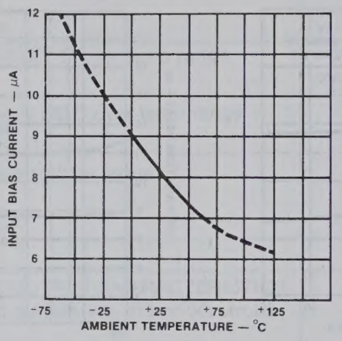


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

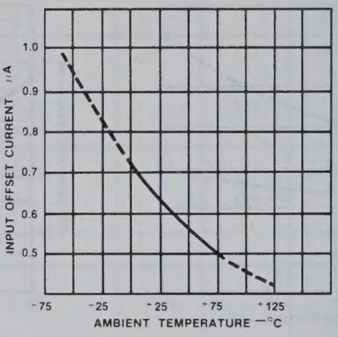


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

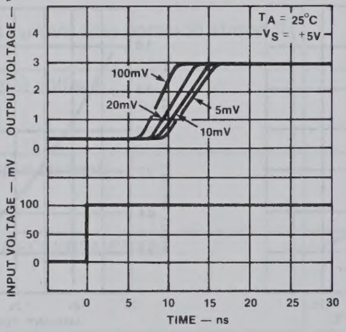
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



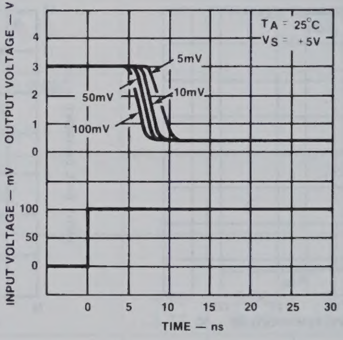
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The 75S207 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75207. The improved input sensitivity of ±10mV makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles. The 75S207 features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S207 also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

FEATURES

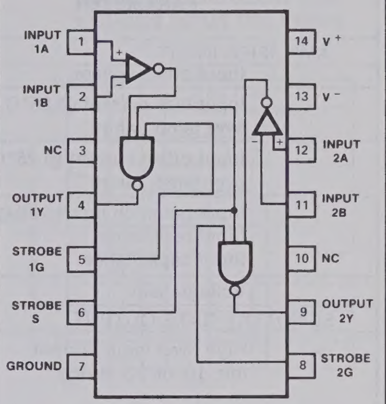
- Functionally equivalent and pin compatible to SN75207
- 17ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- STTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memories sense amp
- A/D conversion
- High speed line receiver

PIN CONFIGURATION

F,N PACKAGE

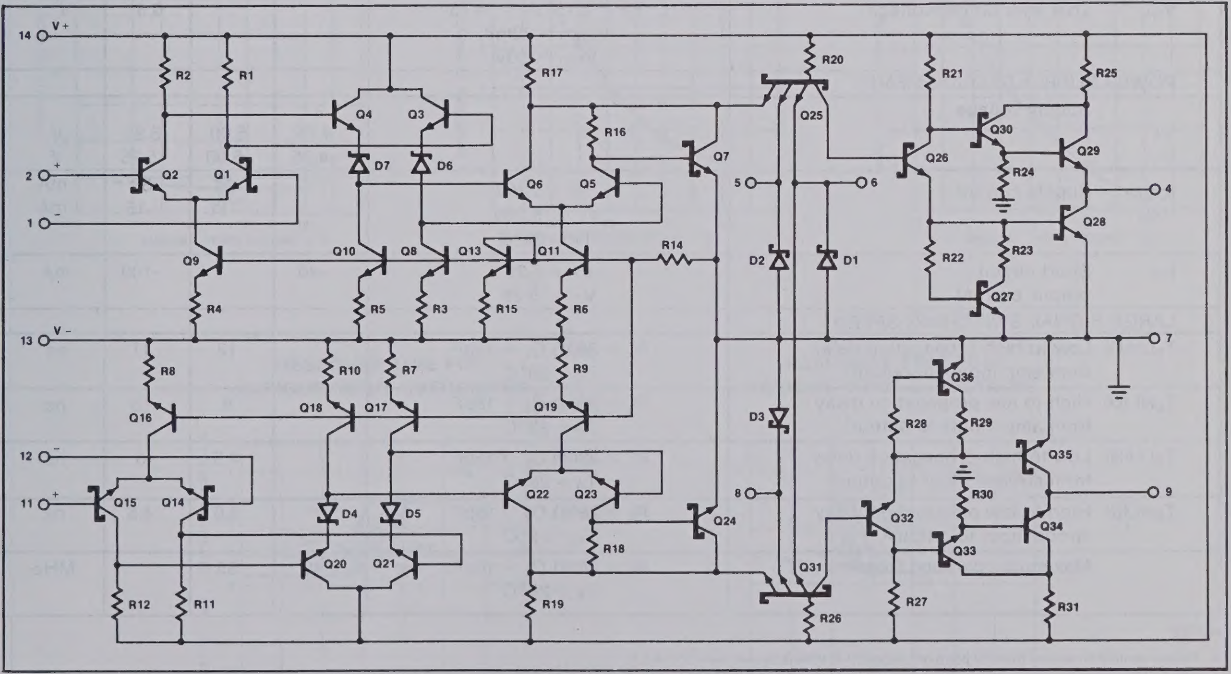

INPUT 1A
1
INPUT 1B
2
NC
3
OUTPUT 1Y
4
STROBE 1G
5
STROBE S
6
GROUND
7
14
V+
13
V−
12
INPUT 2A
11
INPUT 2B
10
NC
9
OUTPUT 2Y
8
STROBE 2G
+
−

ORDER PART NO.
75S207F
75S207N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe/gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature rnage	0 to 70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

EQUIVALENT SCHEMATIC


14
V+
R2
R1
Q4
Q3
R17
R20
R21
R25
2
+
Q2
Q1
D7
D6
R16
Q7
Q25
Q30
Q26
Q29
1
−
Q6
Q5
5
6
R24
4
Q9
Q10
Q8
Q13
Q11
R14
D2
D1
Q28
R4
R5
R3
R15
R6
R22
R23
Q27
13
V−
7
R8
R10
R7
R9
Q36
Q16
Q18
Q17
Q19
D3
R28
R29
12
−
Q35
11
+
Q15
Q14
Q22
Q23
8
R30
9
D4
D5
Q24
Q32
Q34
R18
Q33
Q20
Q21
Q31
R12
R11
R19
R27
R31
R26

DC ELECTRICAL CHARACTERISTICS $V+ = +5.00$, $V- = -5.00$, $T_A = 0$ to 70°C unless otherwise specified.

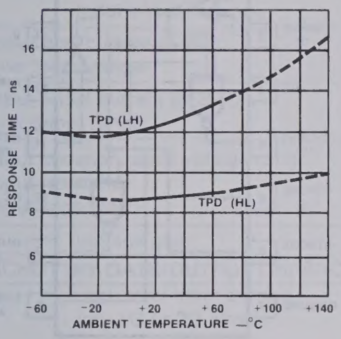
PARAMETER		TEST CONDITIONS	75S207			UNIT
			Min	Typ	Max	
AMPLIFIER INPUT						
	Input offset voltage	$V+ = 4.75$, $V- = -4.75$			10	mV
	Input bias current @ 25°C	$V+ = 5.25$, $V- = -5.25$		7.5	20	µA
	over temp. range	$V+ = 5.25$, $V- = -5.25$			40	µA
	Input offset current @ 25°C	$V+ = 5.25$, $V- = -5.25$		1.0	5	µA
	over temp. range	$V+ = 5.25$, $V- = -5.25$			12	µA
	Input common mode voltage range	$V+ = 4.75$, $V- = -4.75$	±3			V
	Input resistance			4		kΩ
	Input capacitance			3	6	pF
	Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT						
I_{IH}	High level input current into 1G or 2G strobe	$V+ = 5.25$, $V- = -5.25$				
		$V_{IH} = 2.7V$			50	µA
		$V_{IH} = 5.25V$			1	mA
I_{IH}	High level input current into common strobe S	$V+ = 5.25$, $V- = -5.25$				
		$V_{IH} = 2.7V$			100	µA
		$V_{IH} = 5.25V$			2	mA
I_{IL}	Low level input current into 1G or 2G	$V+ = 5.25$, $V- = -5.25$ $V_{IL} = 0.5V$			-2.0	mA
I_{IL}	Low level input current into common strobe S	$V+ = 5.25$, $V- = -5.25$ $V_{IL} = 0.5V$			-4.0	mA
V_{OH}	High level output voltage	$V+ = 4.75$, $V_{I(S)} = 2.0V$ $V- = -4.75$ $I_{LOAD} = -1mA$	2.7	3.4		V
V_{OL}	Low level output voltage	$V+ = 4.75$, $V- = -4.75$ $I_{LOAD} = 20mA$ $V_{I(S)} = 2.0V$			0.5	V
POWER SUPPLY REQUIREMENTS						
	Supply voltage					
V+			4.75	5.00	5.25	V
V-			-4.75	-5.00	-5.25	V
I_{CC+}	Supply current	$V+ = 5.25V$		20	30	mA
I_{CC-}		$V- = -5.25V$		-11	-15	mA
		$T_A = 25°C$				
I_{OS}	Short circuit output current	$V+ = 5.25$ $V- = -5.25$	-40		-100	mA
LARGE SIGNAL SWITCHING SPEED						
$T_pLH(D)$	Low to high propagation delay from amp inputs to output[1]	$R_L = 280\Omega$ $C_L = 15pF$ $T_A = 25°C$		12	17	ns
$T_pHL(D)$	High to low propagation delay from amp inputs to output[1]	$R_L = 280\Omega$ $C_L = 15pF$ $T_A = 25°C$		9	13	ns
$T_pLH(S)$	Low to high propagation delay from strobes input to output[2]	$R_L = 280\Omega$ $C_L = 15pF$ $T_A = 25°C$		4.5	6	ns
$T_pHL(S)$	High to low propagation delay strobe input to output[2]	$R_L = 280\Omega$ $C_L = 15pF$ $T_A = 25°C$		3.0	4.5	ns
	Maximum operating frequency	$R_L = 280\Omega$ $C_L = 15pF$ $T_A = 25°C$	40	55		MHz

NOTES

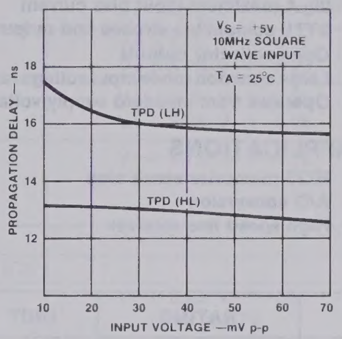
1. Response time measured from 0V point of ±100mV P-P 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

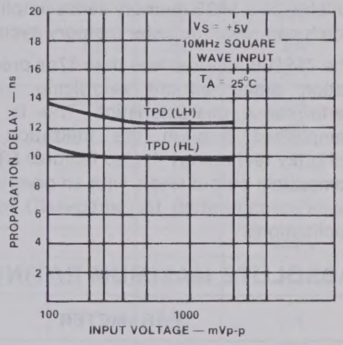
RESPONSE TIME vs TEMPERATURE



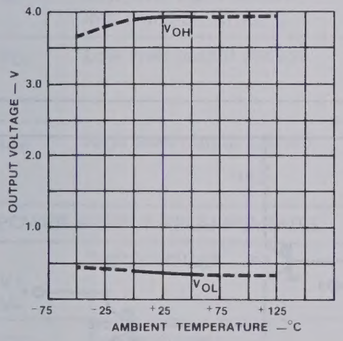
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



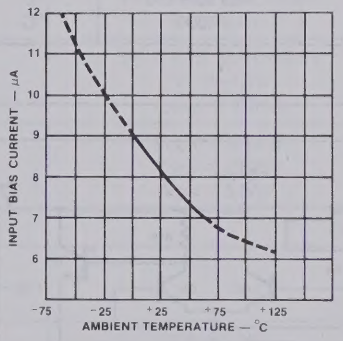
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



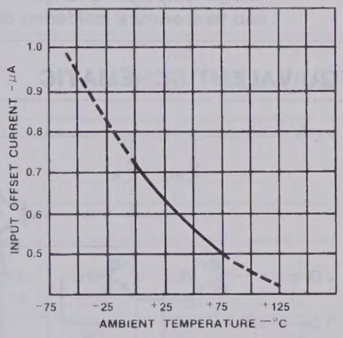
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



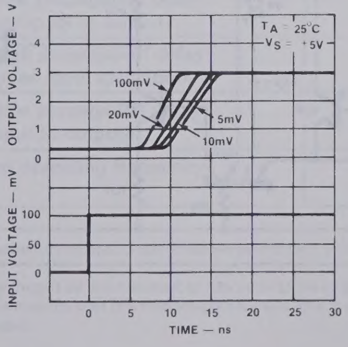
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



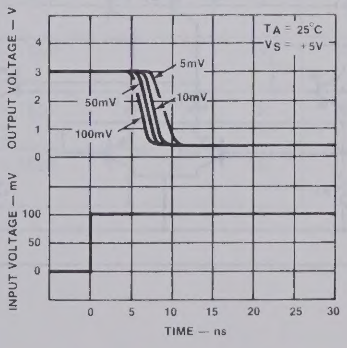
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



HIGH SPEED DUAL SENSE AMPLIFIER FOR MOS MEMORIES 75S208

75S208-F,N

DESCRIPTION

The 75S208 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75208. The improved input sensitivity of ±10mV makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles.

The 75S208 features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

FEATURES

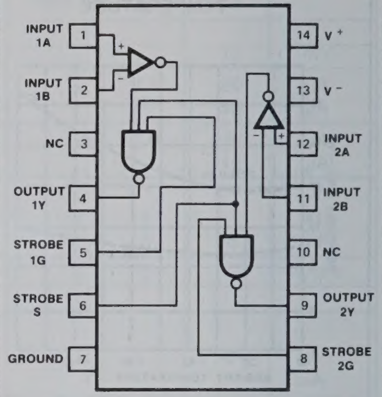
- **Functionally equivalent and pin compatible to 75208**
- **17ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **STTL compatible strobes and outputs**
- **Open collector outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

APPLICATIONS

- **MOS memories sense amp**
- **A/D conversion**
- **High speed line receiver**

PIN CONFIGURATION

F,N PACKAGE



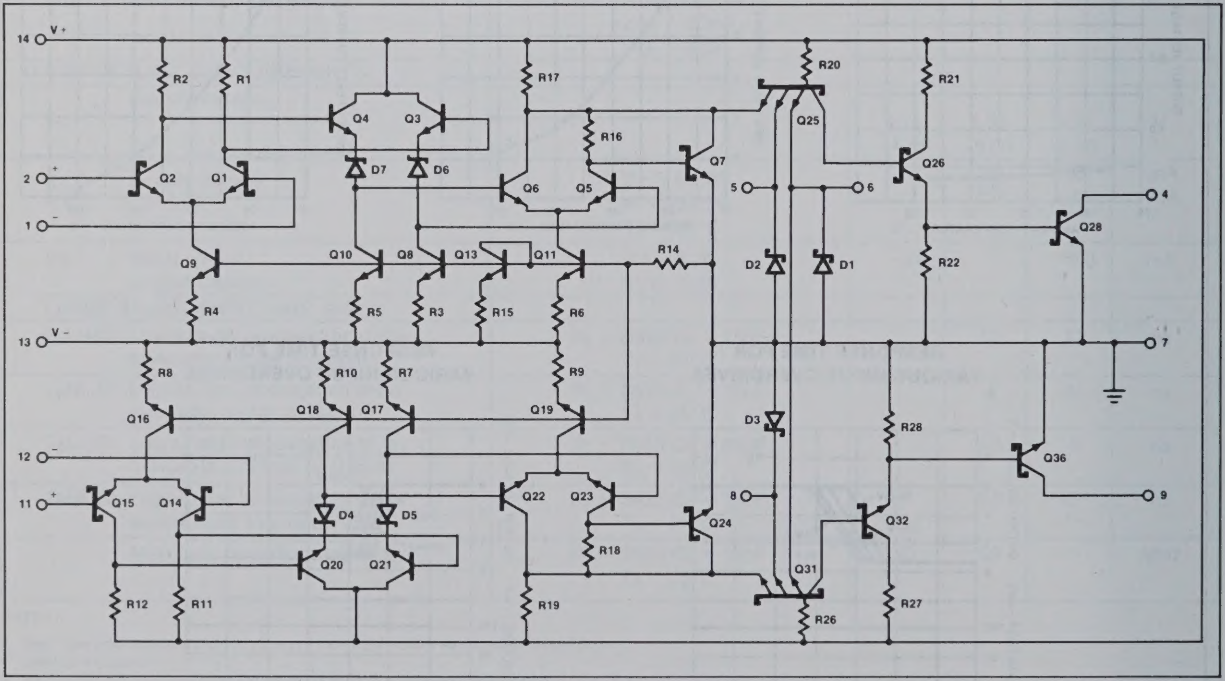
INPUT 1A
1
INPUT 1B
2
NC
3
OUTPUT 1Y
4
STROBE 1G
5
STROBE S
6
GROUND
7
14
V+
13
V−
12
INPUT 2A
11
INPUT 2B
10
NC
9
OUTPUT 2Y
8
STROBE 2G
+
−

ORDER PART NO.
75S208F
75S208N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V−)	-7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe/gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature range	0 to + 70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

EQUIVALENT SCHEMATIC



14 V+
2 +
1 −
13 V−
12 −
11 +
R2
R1
Q4
Q3
Q2
Q1
D7
D6
R17
R16
Q6
Q5
Q7
R20
Q25
R21
Q26
5
6
4
Q28
Q9
Q10
Q8
Q13
Q11
R14
D2
D1
R22
R4
R5
R3
R15
R6
7
R8
R10
R7
R9
Q16
Q18
Q17
Q19
D3
R28
Q36
Q15
Q14
Q22
Q23
8
Q32
9
D4
D5
Q24
R18
Q20
Q21
Q31
R12
R11
R19
R26
R27

DC ELECTRICAL CHARACTERISTICS

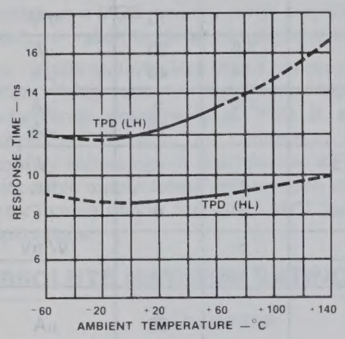
V+ = +5.00, V- = -5.00, T_A = 0 to 70°C unless otherwise specified.

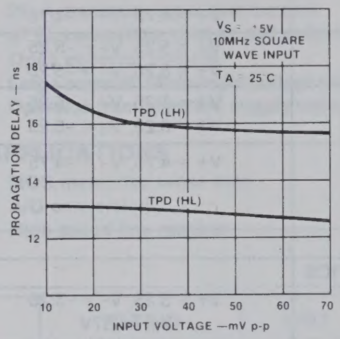
PARAMETER	TEST CONDITIONS	75S208			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT Input offset voltage	V+ = 4.75, V- = -4.75			10	mV
Input bias current @ 25°C over temp. range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		7.5	20 40	µA µA
Input offset current @ 25°C over temp. range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		1.0	5 12	µA µA
Input common mode voltage range Input resistance Input capacitance	V+ = 4.75, V- = -4.75	±3	 4 3	 6	V kΩ pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS					
I_{IH} High level input current into 1G or 2G strobe	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.25V			 50 1	 µA mA
I_{IH} High level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.25V			 100 2	 µA mA
I_{IL} Low level input current into 1G or 2G	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-2.0	mA
I_{IL} Low level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-4.0	mA
V_{OL} Low level output voltage	V+ = 4.75, $V_{I(S)}$ = 2.0V V- = -4.75 I_{LOAD} = 20mA			0.5	V
I_{OH} High level output current	V_{CC}+ = 5.25 V V_{CC}- = -5.25V V_{OH} = 5.25V			250	µA
POWER SUPPLY REQUIREMENTS					
Supply voltage V+ V-		 4.75 -4.75	 5.00 -5.00	 5.25 -5.25	 V V
I_{CC}+ I_{CC}- Supply current	V+ = 5.25V V- = -5.25V T_A = 25°C		20 -11	30 -15	mA mA
LARGE SIGNAL SWITCHING SPEED					
$T_pLH(D)$ Low to high propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		12	17	ns
$T_pHL(D)$ High to low propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		9	13	ns
$T_pLH(S)$ Low to high propagation delay from strobes input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		6	10	ns
$T_pHL(S)$ High to low propagation delay strobe input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		5	8	ns
Maximum operating frequency	R_L = 280Ω C_L = 15pF T_A = 25°C	25	35		MHz

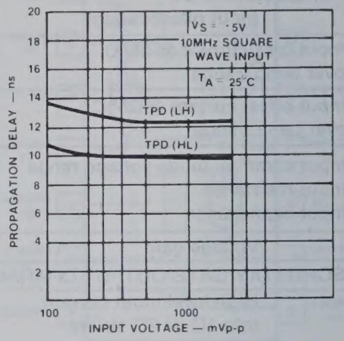
NOTES

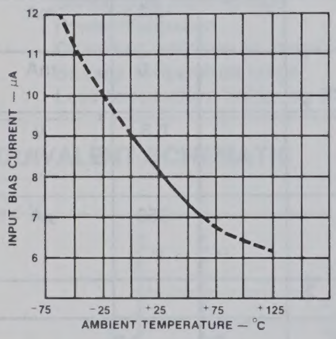
1. Response time measured from 0V point of ±100MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

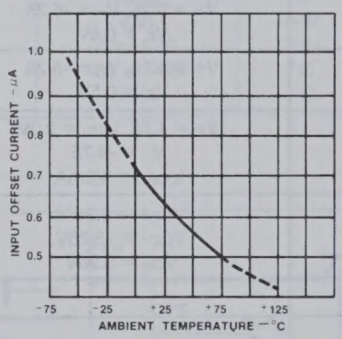
TYPICAL PERFORMANCE CHARACTERISTICS

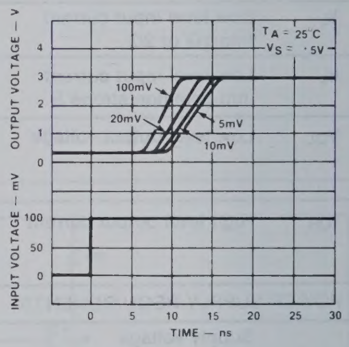

RESPONSE TIME vs TEMPERATURE

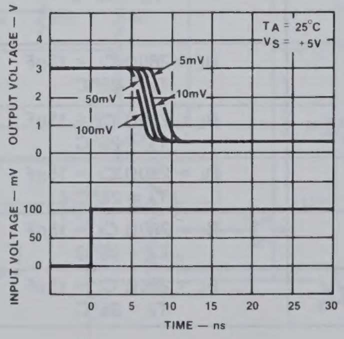

PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE


INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

SECTION 9
DISPLAY DRIVERS

Section 9—DISPLAY DRIVERS

NE582 Hex Universal Driver 273
NE587 LED Decoder/Driver 275
NE589 LED Decoder/Driver 284
NE/SA594 Vacuum Flourescent Display Driver 293

DISPLAY DRIVER DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} $(-V_{CC})$

Supply Voltage. The range of power supply voltage over which the device will operate safely.

LED

Light Emitting Diode

$\overline{XX}$

Negate Bar–when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.

i.e. LE - would require a logic high level to cause a latch enable.

$\overline{LE}$ - would require a logic low level to cause a latch enable.

I_{SEG}

Segment Current. The amount of current supplied to each segment in a display. Current ratios are generally compared to segment 'b'.

BCD

Binary Coded Decimal

$\overline{BI}$/RBO

Blanking Input or Ripple Blanking Output.

$\overline{RBI}$

Ripple Blanking Input. The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

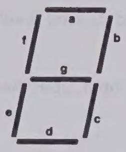
t_{PLH}

Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL}

Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

Segment Identification



t_h

Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s

Setup Time. The interval immediately preceeding the active transition of the timing pulse (usually the clock pulse) or preceeding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_W

Pulse Width. The time between the specified reference points on the leading and trailing edges of a pulse.

t_{rec}

Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

I_{OH}

Output Current Source the device can supply while maintaining a specified voltage output level.

Typical Value

The typical value of a particular parameter determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-

DISPLAY DRIVER DEFINITIONS (Cont'd)

max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

I_S

Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

Duty Cycle

Ratio of time on to time off. Generally expressed in percentage.

V_F

Forward voltage drop of a device at a specified current level.

I_B

Input Bias Current Current into an analog circuit input, specified at a particular voltage level.

CLR

Clear. Clear command will preset all internal circuits to a predetermined state.

CE

Chip Enable.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

$I_{CC}(-I_{CC})$

Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{IH}

Input High Current. The Current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}

Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OL}

Output Low Current. The current flowing into an output when a which is in the Low State.

I_{OS}

Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is short circuit to the ground.

I_{CEX}

Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

HEX UNIVERSAL DRIVER NE582

NE582-N

DESCRIPTION

The NE582 is a general interface device comprising a high current output transistor and drive circuitry in each of 6 elements. Each output transistor is individually capable of sinking 400mA with a typical saturation voltage of 0.5V. Input loading is such that direct interfacing with P-MOS, N-MOS, C-MOS or TTL is possible.

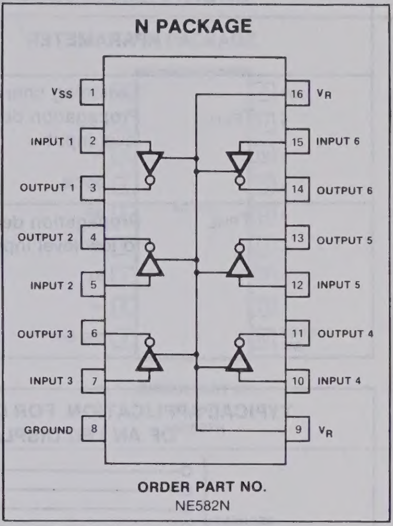
The NE582 has applications as a LED display driver, low voltage relay/lamp drivers and many others where high current capability without speed constraints is required.

The NE582 is supplied in a 16-pin high dissipation dual-in-line plastic package.

FEATURES

- **Low saturation voltage (typically 0.5V) for minimum power dissipation**
- **High output sink current capability—400mA**
- **Low input current loading for MOS compatibility**
- **Low standby power consumption**
- **Suitable for 3 volt battery operation**
- **Inputs/outputs are compatible with 75494**

PIN CONFIGURATION



ORDER PART NO.
NE582N

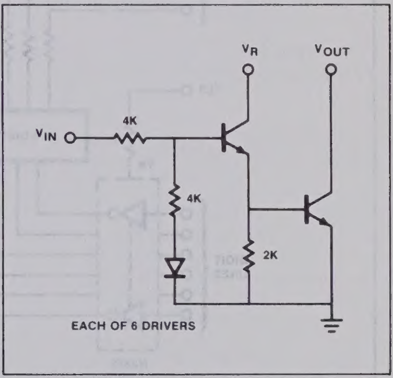
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage range[1]	-12 to V_{SS}	V
Output voltage[2]	10	V
Output to input voltage differential	10	V
Voltage at V_{SS} (pin 1)	10	V
Output current—each output	400	mA
Output current—all outputs	800	mA
Continuous total power dissipation at or below 25°C[3]	800	mW
Current in V_R (pin 9 or 16)	25	mA
Operating free-air temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature 1/16 inch from case for 10sec	260	°C

NOTES

1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above 25°C, derate power dissipation at 6.25mW/°C.

EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS

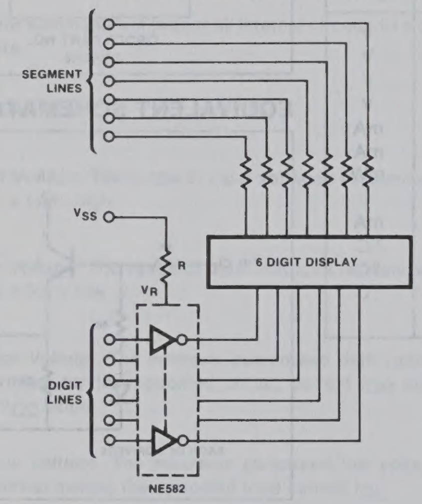
$T_A = 0°C$ to $70°C$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{OL}	Low level output voltage	V_{IN} I_R I_{OL} V mA mA 6.5 12 250 6.5 20 400 $R_{IN} = 1K$ (Series input resistance)		.320 .500	.450 .750	V V
I_{OH}	High level output current	$V_{OH} = 10V$, $I_{IN} = 40\mu A$ $V_{OH} = 10V$, $V_{IN} = 0.5V$			400 400	µA µA
I_{IN}	Input current at maximum Input voltage	$V_{IN} = 10V$, $I_{OL} = 20mA$, $I_R = 2mA$		2.2	3.3	mA
V_R		$V_{IN} = 6.5V$, $I_R = 6mA$, $I_{OL} = 80mA$		.9	1.5	V
I_{SS}	Current into pin 1	$V_{SS} = 10V$			100	µA

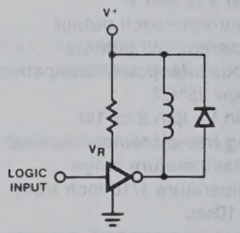
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Switching characteristics					
T_{PLH}	Propagation delay, low to high level input	$R_R = 680\Omega$ $R_L = 39\Omega$ $C_L = 15pF$		300		ns
T_{PHL}	Propagation delay, high to low level input	$V_{IH} = 7.5V$ $V_{IL} = 0V$ $t_r = t_f \leq 10ns$ $t_w = 1\mu s$ PRR = 100kHz		30		ns

TYPICAL APPLICATION FOR DIGIT DRIVING OF AN LED DISPLAY



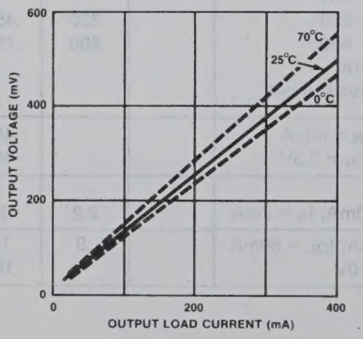
1/6 NE582 AS A RELAY DRIVER



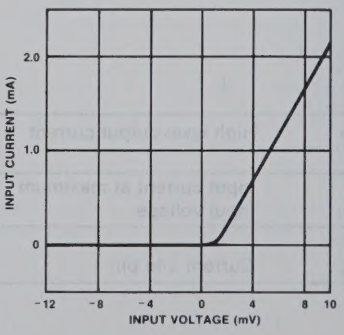
1/6 NE582 AS A RELAY DRIVER

PRELIMINARY SPECIFICATION

OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT, $I_R = 25mA$ $V_{IN} = 6.5$ VOLTS



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE, $I_R = 25mA$, $V_{SS} = 10V$, $T_A = 25°C$



DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

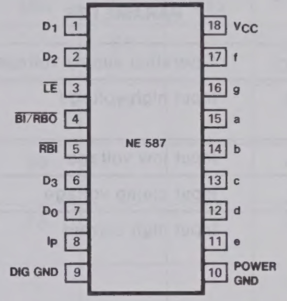
- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

PIN CONFIGURATIONS

F,N PACKAGE



D_1 1
D_2 2
$\overline{LE}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
D_3 6
D_0 7
Ip 8
DIG GND 9
NE 587
18 V_{CC}
17 f
16 g
15 a
14 b
13 c
12 d
11 e
10 POWER GND

ORDER PART NO.
NE587F
NE587N

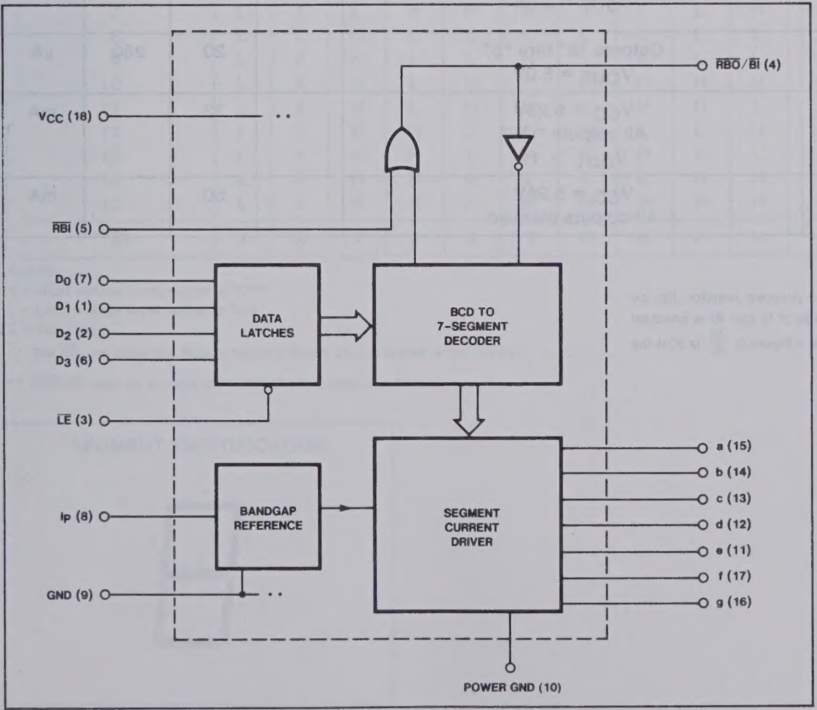
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

BLOCK DIAGRAM



$\overline{RBO}/\overline{BI}$ (4)
V_{CC} (18)
$\overline{RBI}$ (5)
D_0 (7)
D_1 (1)
D_2 (2)
D_3 (6)
DATA LATCHES
BCD TO 7-SEGMENT DECODER
$\overline{LE}$ (3)
a (15)
b (14)
c (13)
d (12)
e (11)
f (17)
g (16)
Ip (8)
BANDGAP REFERENCE
SEGMENT CURRENT DRIVER
GND (9)
POWER GND (10)

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C.
Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (± 1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs D_0-D_3, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V Input $\overline{BI}$ (pin 4) $\overline{RBI}$ = H $V_{IN} = V_{CC}$ = 5.25V		0.1 10		µA µA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs D_0-D_3 $\overline{LE}$, $\overline{RBI}$		−5 −200		µA
		Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{out} = 3.0mA		.2		V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50µA $\overline{RBI}$ = H		4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g" V_{OUT} = 5.0V		20	250	µA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		33		mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		50		mA

NOTE
NE587 PROGRAMMING
The NE587 output current can be programmed, provided a program resistor, Rp, be connected between Ip (pin 8) and Ground (pin 9). The voltage at Ip (pin 8) is constant (≈1.3V). Thus, a current through Rp is $I_p \approx \frac{1.3V}{R_p}$, as shown in Figure 5. $\frac{I_o}{I_p}$ is 20 in the 15 to 50mA output current range.

NE587-F,N

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$ $T_A = 25°C$. $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
$t_{D_{av.}}$	Propagation delay Figure 2	From data to output		85		ns
$t_{D_{av.}}$	Propagation delay Figure 3	From $\overline{LE}$ to output		85		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

NOTE

$t_{D_{av.}} = ½ (t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	LE	RBI	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	•	X	X	X	X	STABLE							••	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	blank
••BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L••	blank

NOTES

H = HIGH voltage level, output is "OFF"

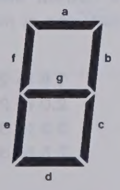
L = LOW voltage level, output is "ON"

X = Don't care

* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

** $\overline{RBO}/\overline{BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$1.40V). A partial schematic of the voltage reference used in the NE587 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

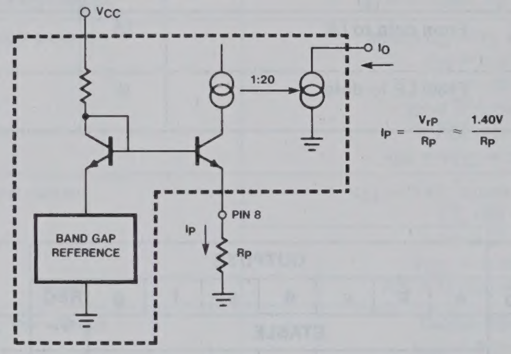


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

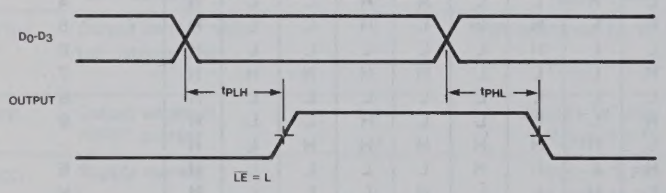


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

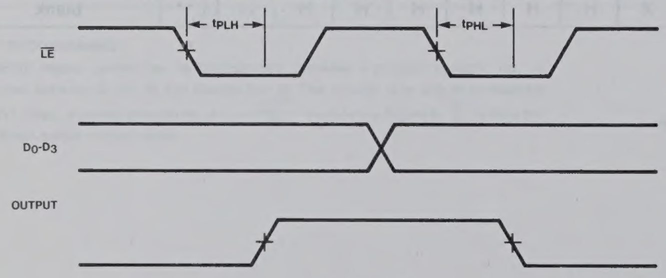


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

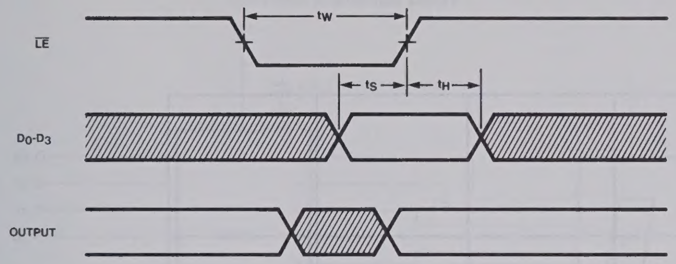


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

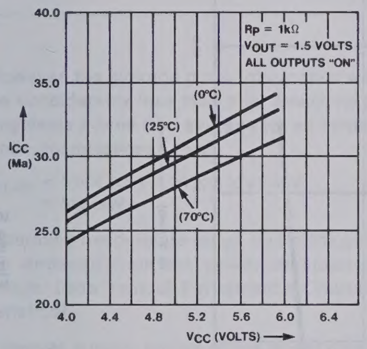
Thus a maximum power dissipation calculation when all segments are on, is:

$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

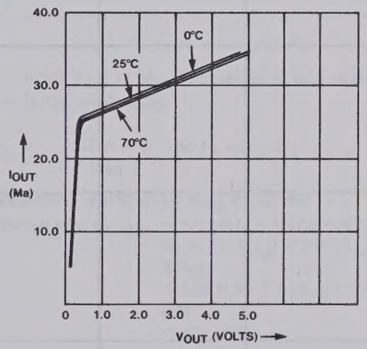
Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$
$P_{d\,max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

TYPICAL PERFORMANCE CURVES

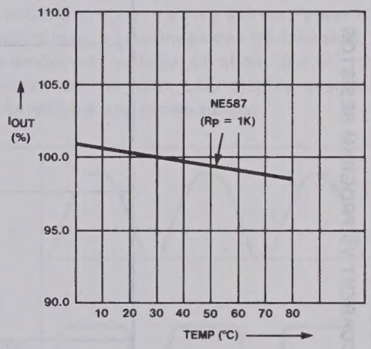
SUPPLY CURRENT VS SUPPLY VOLTAGE NE587



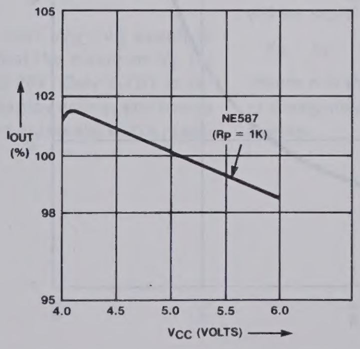
OUTPUT CURRENT VS OUTPUT VOLTAGE NE587 Rp = 1Kohms



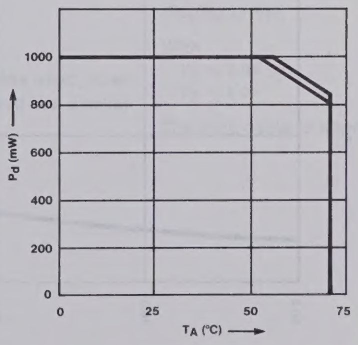
NORMALIZED OUTPUT CURRENT VS TEMPERATURE V_{CC} = 5.0 VOLTS



NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE V_O = 1.5V T_A = 25°C



MAXIMUM POWER DISSIPATION VS TEMPERATURE



TYPICAL PERFORMANCE CURVES (Cont'd)

OUTPUT CURRENT VS PROGRAM RESISTOR

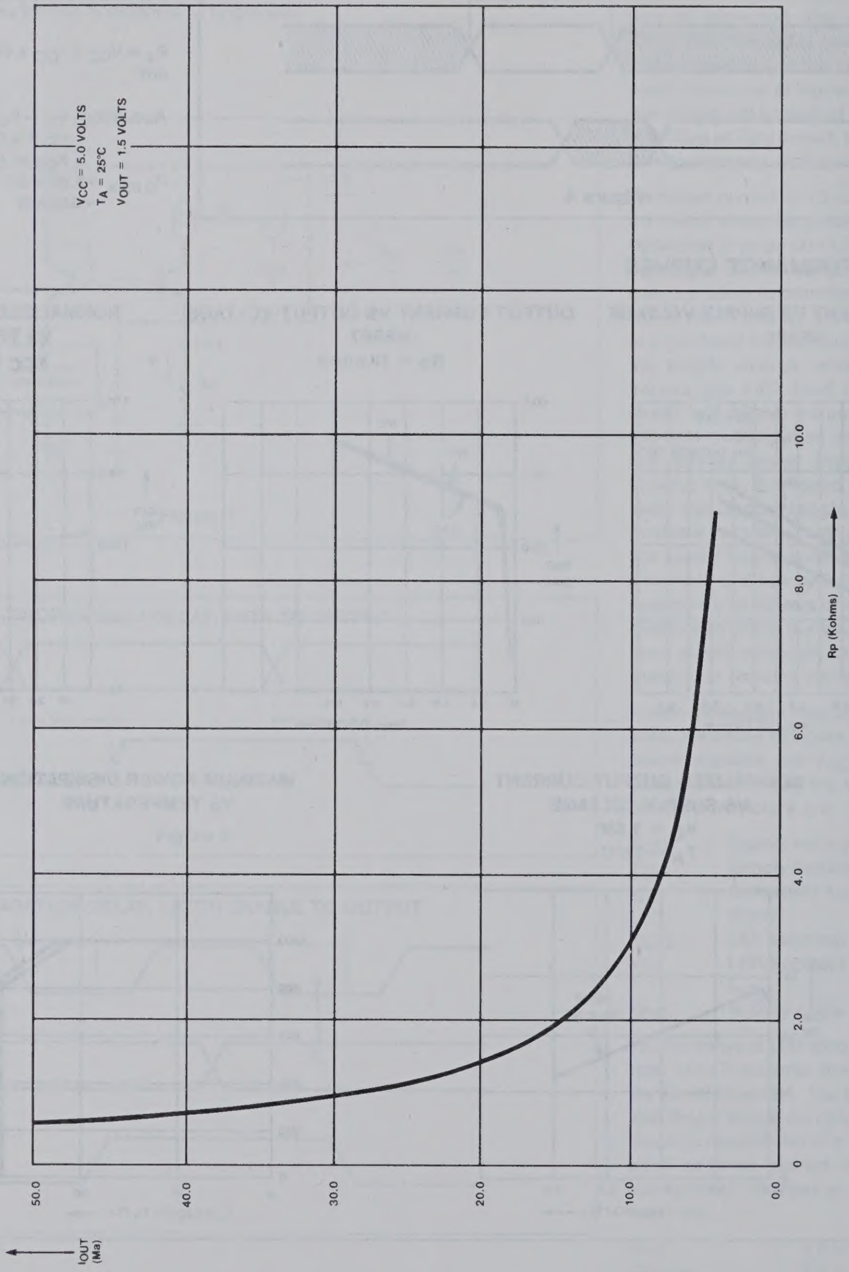
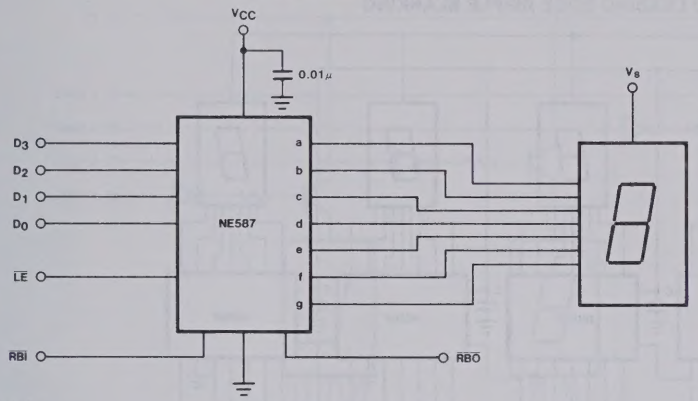


Figure 5

TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 µF ceramic

Figure 6

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\ av} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW} = 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics).

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now
$$P_{d\ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\, I_{seg} \times K_{DC} = 5.25 \times 50 + 1.25 \times 7 \times 30 \text{ mW} = 525 \text{ mW}$$

and
$$P_{d\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306 \text{ mW}$$

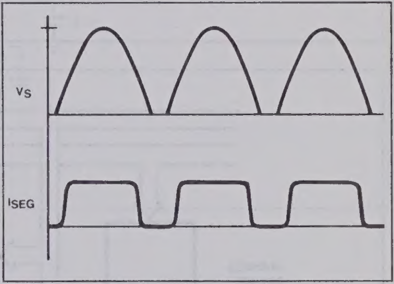
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d\,,\ V_D \simeq 0.8\text{V}$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 9. For example a darlington PNP or NPN emitter follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
V_S = 4.9V pk.
V_F = 2.0V

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING

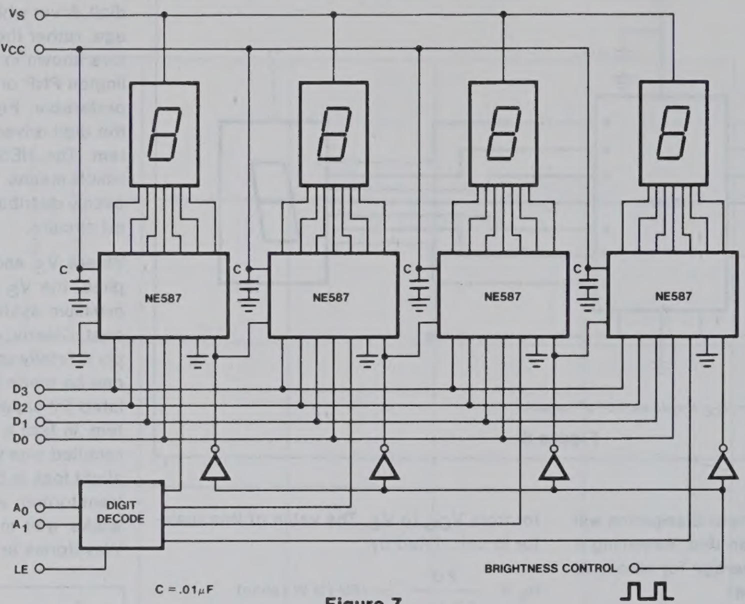

VS
VCC
C
NE587
D3
D2
D1
D0
A0
A1
DIGIT DECODE
LE
C = .01µF
BRIGHTNESS CONTROL

Figure 7

INTERFACING 8-DIGIT LED DISPLAY WITH µP BUS

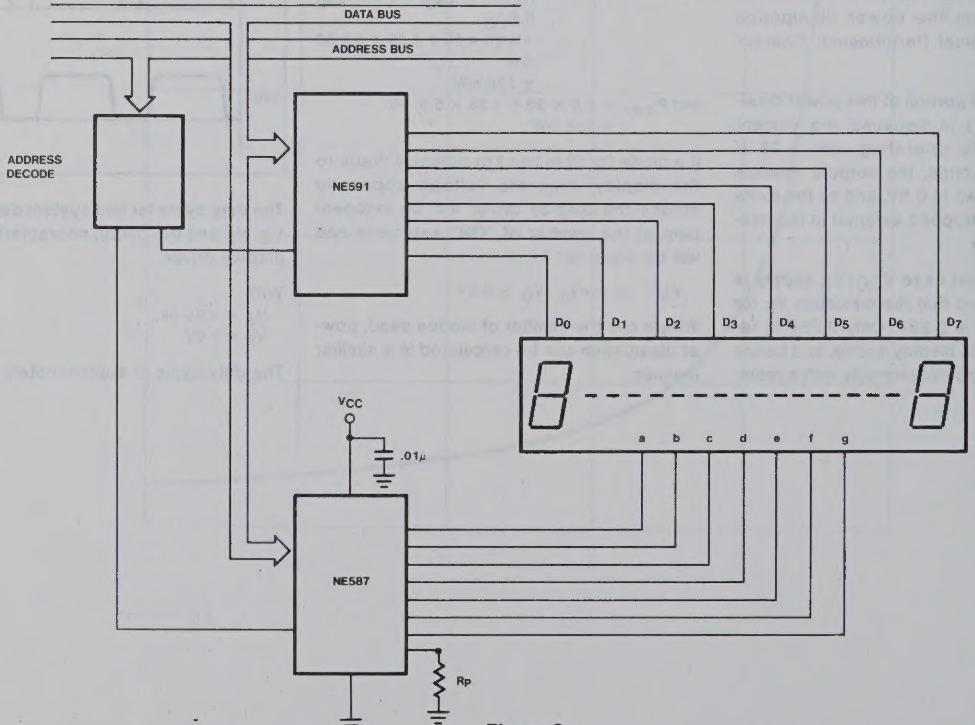

DATA BUS
ADDRESS BUS
ADDRESS DECODE
NE591
D0
D1
D2
D3
D4
D5
D6
D7
a
b
c
d
e
f
g
VCC
.01µ
NE587
Rp

Figure 8

TYPICAL APPLICATIONS (Cont'd)

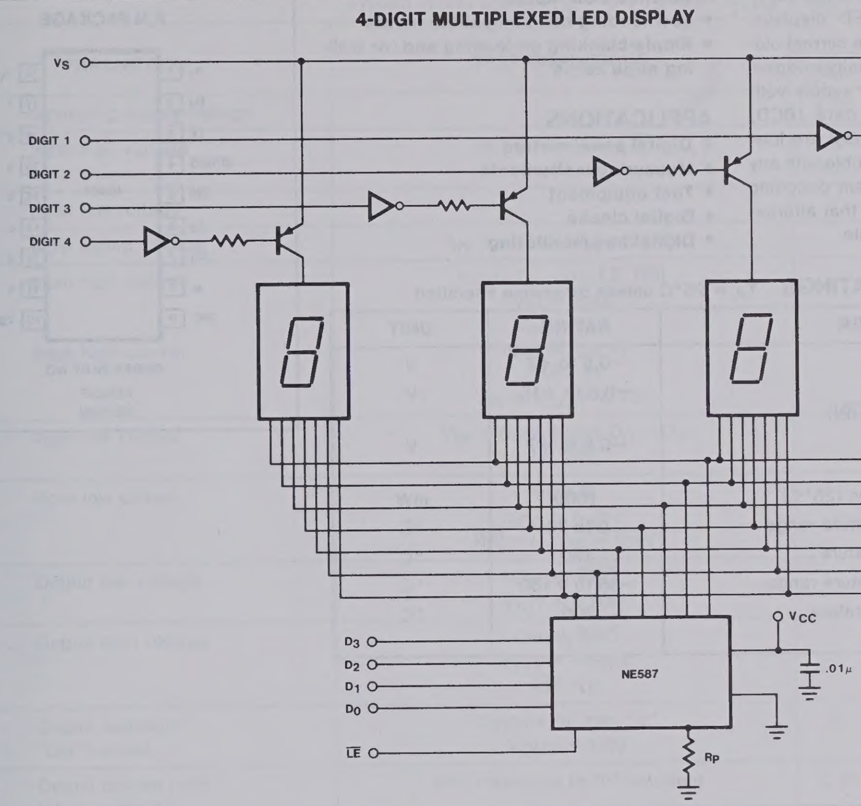

4-DIGIT MULTIPLEXED LED DISPLAY
VS
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
D3
D2
D1
D0
LE
NE587
VCC
.01μ
Rp

Figure 9

DESCRIPTION

The NE589 is a latch/decoder/driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

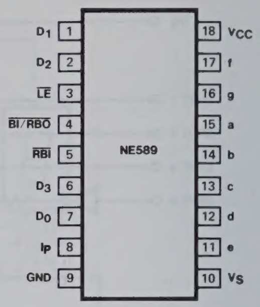
- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading and/or trailing edge zeros

APPLICATIONS

- Digital panel meters
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

PIN CONFIGURATION

F,N PACKAGE


D1 1
D2 2
LE 3
BI/RBO 4
RBI 5
D3 6
D0 7
Ip 8
GND 9
NE589
18 VCC
17 f
16 g
15 a
14 b
13 c
12 d
11 e
10 VS

ORDER PART NO.

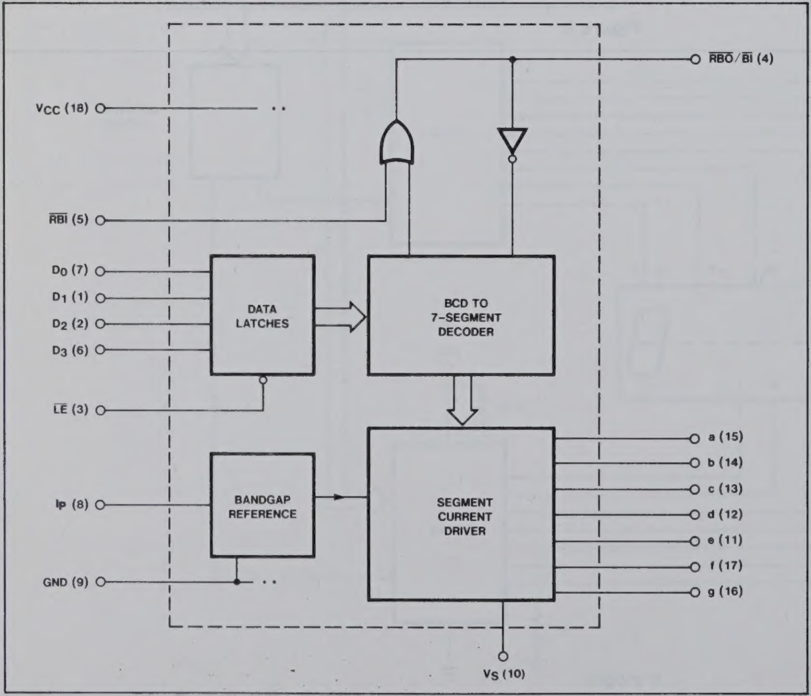
NE589F
NE589N

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}, V_S	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

BLOCK DIAGRAM


RBO/BI (4)
VCC (18)
RBI (5)
D0 (7)
D1 (1)
D2 (2)
D3 (6)
DATA LATCHES
BCD TO 7-SEGMENT DECODER
LE (3)
Ip (8)
BANDGAP REFERENCE
SEGMENT CURRENT DRIVER
GND (9)
a (15)
b (14)
c (13)
d (12)
e (11)
f (17)
g (16)
VS (10)

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C.
Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 6kΩ (±1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE589			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	$I_{IN} = -12mA$, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V		 0.1		 µA µA
I_{IH}	Input high current	Input $\overline{BI}$ (pin 4) $\overline{RBI}$ = H $V_{IN} = V_{CC}$ = 5.25V		10		µA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs $D_0 - D_3$ $\overline{LE}$, $\overline{RBI}$		−5 −200		 µA
I_{IL}	Input low current	Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{OUT} = 3.0mA				V
V_{OH}	Output high voltage	Output $\overline{RBO}$ $I_{OUT} = -50\mu A$ $\overline{RBI}$ = H		4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g"		20	250	µA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		25		mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		30		mA

NOTE:
NE587 PROGRAMMING
The NE587 output current can be programmed, provided a program resistor, Rp, be connected between Ip (pin 8) and Ground (pin 9). The voltage at Ip (pin 8) is constant (≈ 1.3V). Thus, a current through Rp is $Ip \approx \frac{1.3V}{Rp}$, as shown in Figure 10. $\frac{Io}{Ip}$ is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$ $T_A = 25°C$. $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

	PARAMETER	TEST CONDITIONS	NE589			UNIT
			Min	Typ	Max	
$t_{Dav.}$	Propagation delay Figure 2	From data to output		85		ns
$t_{Dav.}$	Propagation delay Figure 3	From $\overline{LE}$ to output		85		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

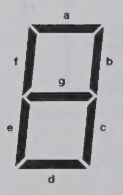
NOTE:
$t_{DAV.} = ½ (t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE								STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	H	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	L	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	c
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	e
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	f
**BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	blank

NOTES
H = HIGH voltage level, output is "ON"
L = LOW voltage level, output is "OFF"
X = Don't care
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO/BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



NE589 PROGRAMMING

NE589 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$1.25V). A partial schematic of the voltage reference used in the NE589 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_p must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

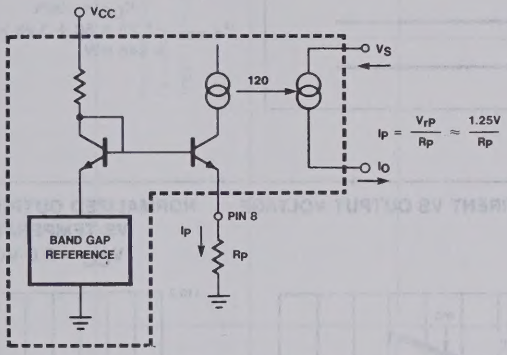


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

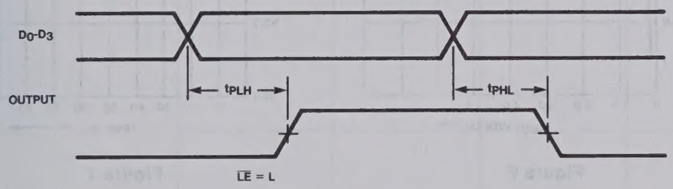


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

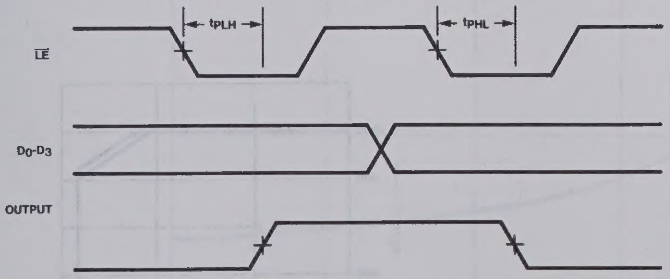


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 12, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

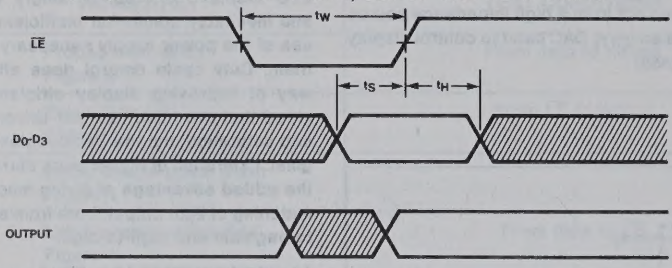


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

$P_{d\ max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

TYPICAL PERFORMANCE CURVES

OUTPUT CURRENT VS OUTPUT VOLTAGE

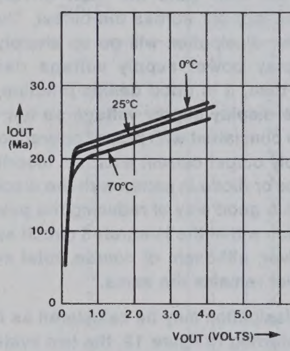


Figure 5

OUTPUT CURRENT VS OUTPUT VOLTAGE

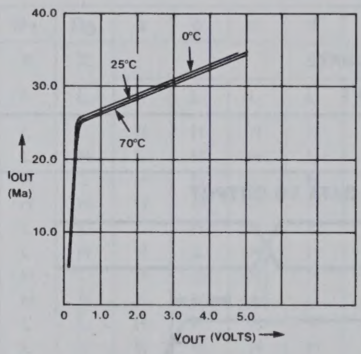


Figure 6

NORMALIZED OUTPUT CURRENT VS TEMPERATURE $V_{CC} = 5.0$ VOLTS

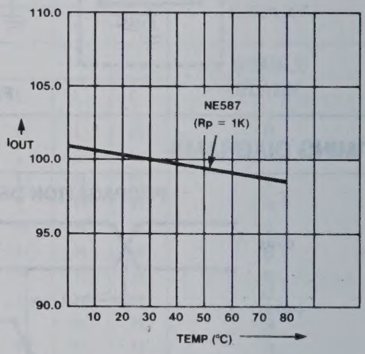


Figure 7

NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE V_{CC}

$V_O = 1.5V$
$T_A = 25°C$

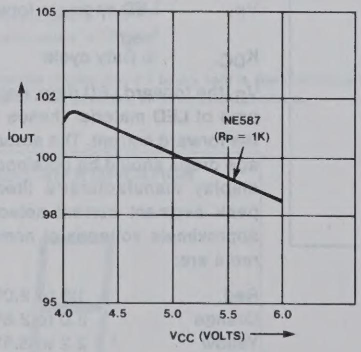


Figure 8

MAXIMUM POWER DISSIPATION VS TEMPERATURE

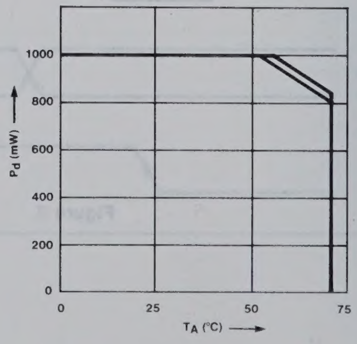


Figure 9

TYPICAL PERFORMANCE CURVES (Cont'd)

OUTPUT CURRENT VS PROGRAM RESISTOR

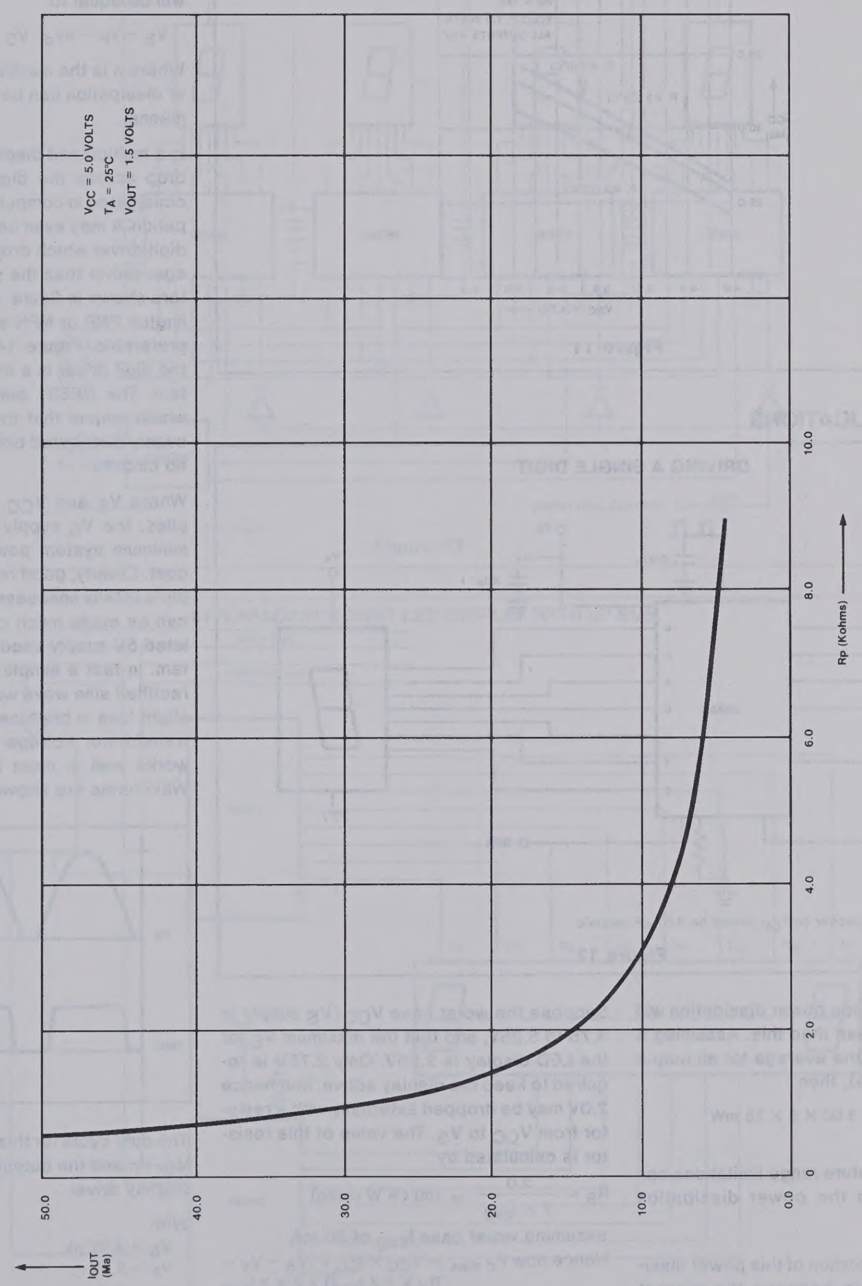


Figure 10

TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY CURRENT VS SUPPLY VOLTAGE NE589

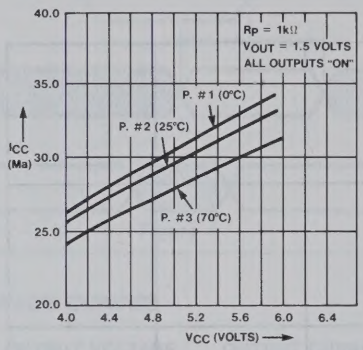
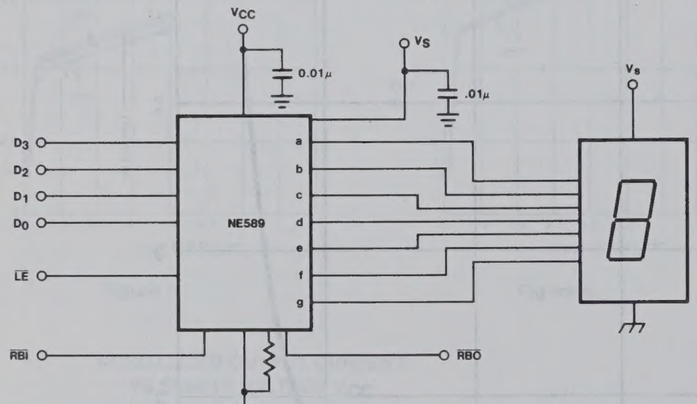


Figure 11

TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 μF ceramic

Figure 12

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\ av} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW}$$
$$= 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph in figure 9.

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\, I_{seg} \times K_{DC}$

$= 5.25 \times 50 + 1.25 \times 7 \times 30$ mW

$= 525$ mW

and $P_{d\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25$

$= 306$ mW

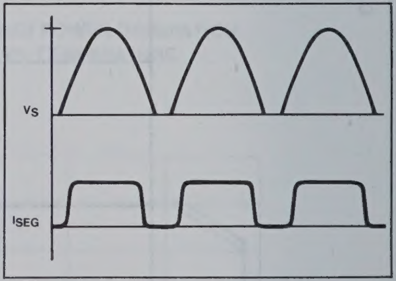
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d\ ,\ V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 15. For example a darlington PNP or NPN emitter follower may be preferable. Figure 14 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With

$V_S = 4.9V$ pk.

$V_F = 2.0V$

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)

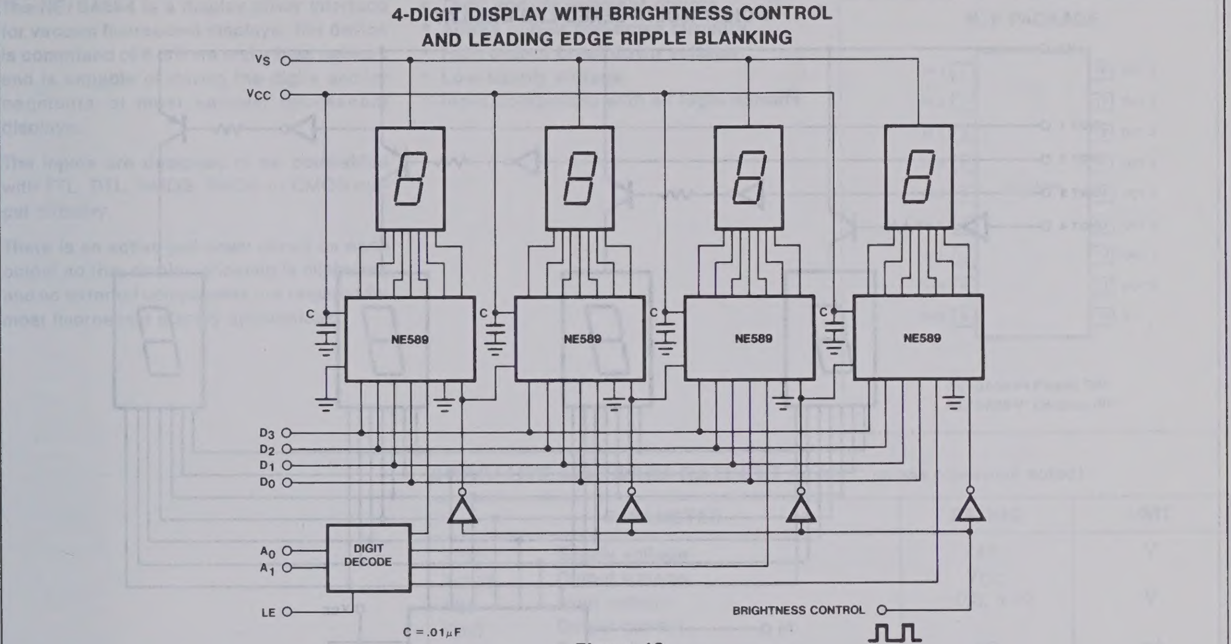

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING
VS
VCC
C
NE589
NE589
NE589
NE589
D3
D2
D1
D0
A0
A1
DIGIT DECODE
LE
C = .01μF
BRIGHTNESS CONTROL

Figure 13

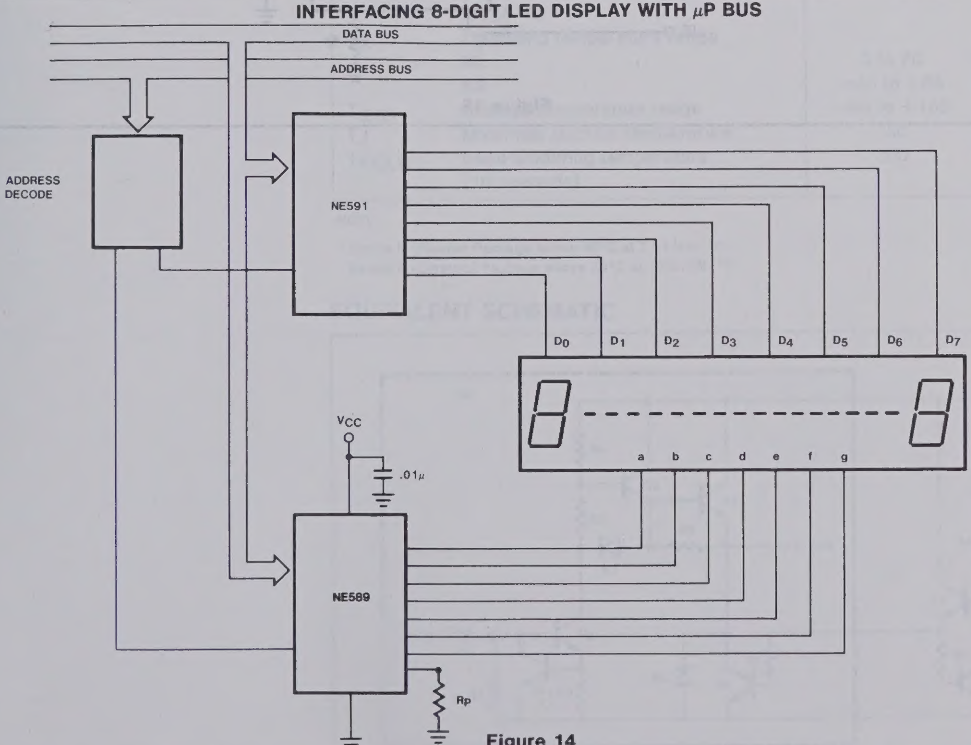

INTERFACING 8-DIGIT LED DISPLAY WITH μP BUS
DATA BUS
ADDRESS BUS
ADDRESS DECODE
NE591
D0
D1
D2
D3
D4
D5
D6
D7
a
b
c
d
e
f
g
VCC
.01μ
NE589
Rp

Figure 14

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

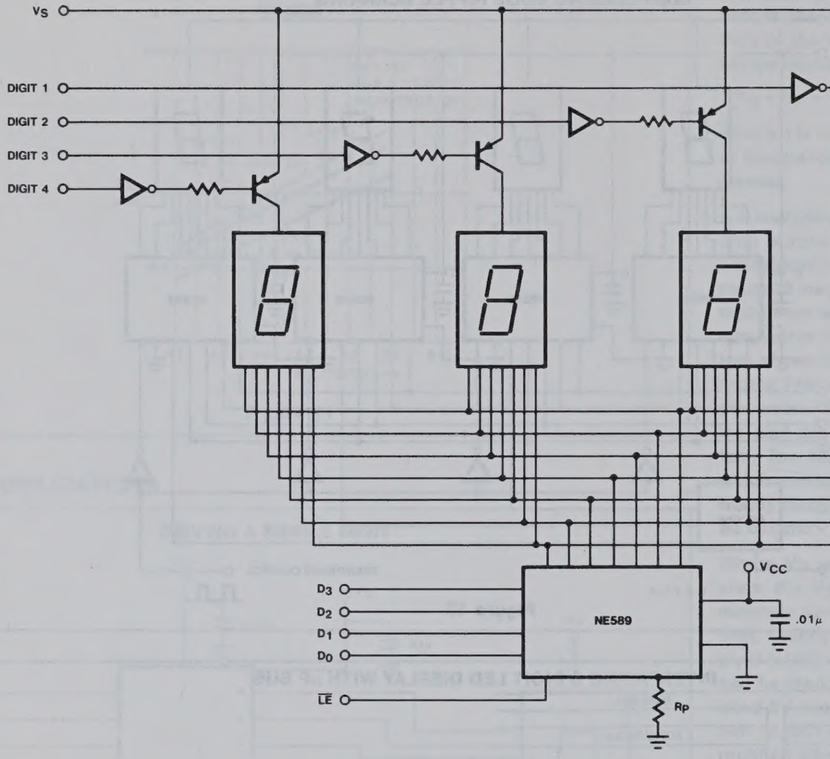

VS
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
VCC
NE589
.01μ
D3
D2
D1
D0
LE
Rp

Figure 15

VACUUM FLUORESCENT DISPLAY DRIVER NE/SA594

NE/SA594-N,F

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

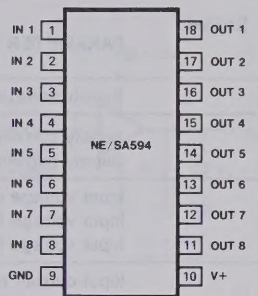
There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

- Digit and/or segment drivers
- Active output pull-down circuitry
- High output breakdown voltage
- Low supply voltage
- Input compatible with all logic outputs

PIN CONFIGURATION

N, F PACKAGE


IN 1 1
IN 2 2
IN 3 3
IN 4 4
IN 5 5
IN 6 6
IN 7 7
IN 8 8
GND 9
18 OUT 1
17 OUT 2
16 OUT 3
15 OUT 4
14 OUT 5
13 OUT 6
12 OUT 7
11 OUT 8
10 V+
NE/SA594

NE/SA594N Plastic DIP
NE/SA594F Ceramic DIP

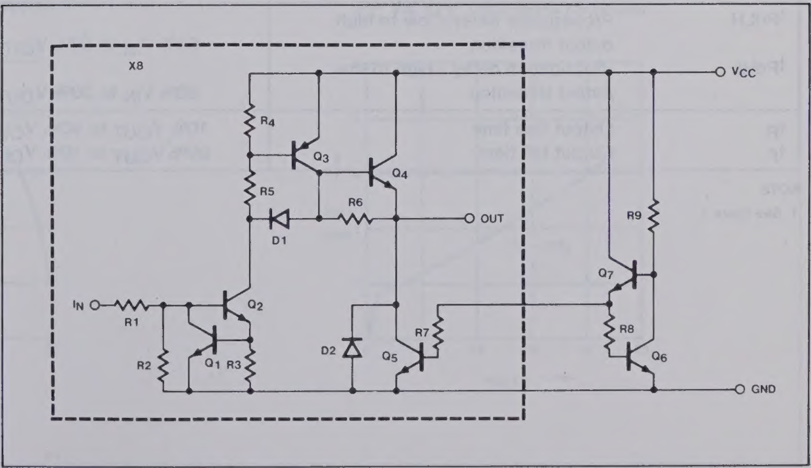
ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	−0.3, +20	V
I_{OUT}	Output current		
	Each output	50	mA
	All outputs	200	mA
Pd	Power dissipation* (at 25°C)	800	mW
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Maximum junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE

*Derate N (Plastic) Package above 38°C at 7.14 mW/°C.
Derate F (Ceramic) Package above 75°C at 10.8 mW/°C.

EQUIVALENT SCHEMATIC


X8
V_{CC}
R4
Q3
Q4
R5
R6
OUT
D1
R9
Q7
I_N
R1
Q2
R2
Q1
R3
D2
Q5
R7
R8
Q6
GND

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.75 to +40V, T_A (NE) = 0 to 70°C, T_A (SA) = −40 to +85°C unless otherwise stated.

SA594	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
V_{CC}	Supply voltage range		4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	V_{CC} = 40V V_{IN} = 3.5V		3	6	mA
I_{CCL}	Supply current (all outputs low)	V_{CC} = 40V V_{IN} = 0.4V		0.4	1	mA
V_{IN}	Input voltage range		0		15	V
V_{IH}	Input voltage to ensure logic '1'		2.6			V
V_{IL}	Input voltage to ensure logic '0'				0.8	V
I_{IH}	Input current to ensure logic '1'		100			µA
I_{IL}	Input current to ensure logic '0'				10	µA
I_{IN}	Input current	V_{IN} = 2.6V		60	130	µA
		V_{IN} = 5.0V		180	330	µA
		V_{IN} = 15.0V		.68	1.3	mA
V_{OH}	Output high voltage	V_{IN} = 3.5V, T_A = 25°C	V_{CC}−1.5	V_{CC}−1.1		V
		I_{OUT} = −25mA, Over Temp.	V_{CC} −2	V_{CC}−1.3		V
		V_{OUT} with respect to V_{CC}				
V_{OH}	Output high, *no load* voltage	V_{IN} = 3.5V I_{OUT} = 0, T_A=25°C V_{OUT} with respect to V_{CC}	V_{CC}−1	V_{CC}−0.8		V
V_{OFF}	Output 'OFF' voltage level	V_{IN} = 0.8V I_{OUT} = 0		10	200	mV
I_{OH}	Available output current	V_{CC} = 35V V_{IN} = 3.5V V_{OUT} = 30V T_A = 25°C	−35			mA
I_{OUT}	Output pulldown current	V_{CC} = V_{OUT} = 35V Inputs open	100	200	400	µA
I_{CEX}	Output leakage current	T_A = 25°C V_{IN} = 0.4V		−1		µA
		V_{CC} = 40V, V_{OUT} = 0V		−1		

AC ELECTRICAL CHARACTERISTICS[1]

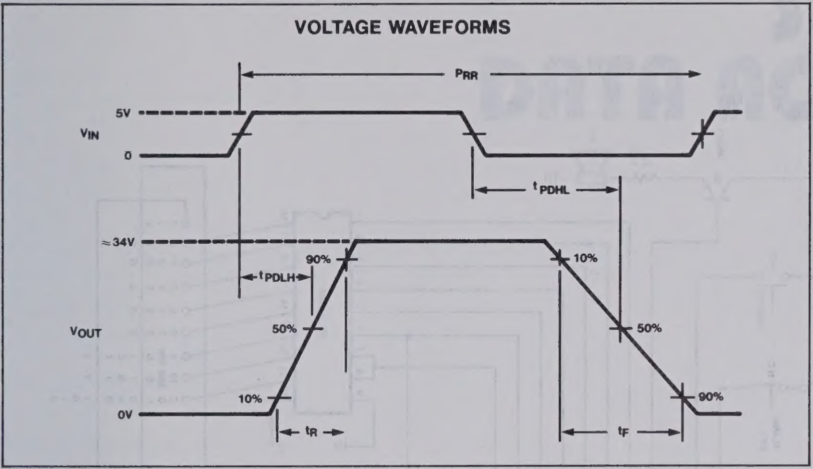
V_{CC} = 35V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	NE/SA594			UNIT
			Min	Typ	Max	
t_{PdLH}	Propagation delay - low to high output transition.	50% V_{IN} to 50% V_{OUT}		1	5	µS
t_{PdHL}	Propagation delay - high to low output transition.	50% V_{IN} to 50% V_{OUT}		3	10	µS
t_R	Output rise time	10% V_{OUT} to 90% V_{OUT}		0.5	3	µS
t_F	Output fall time	90% V_{OUT} to 10% V_{OUT}		1.5	5	µS

NOTE

1. See figure 1

SWITCHING TIMES OF DRIVERS


VOLTAGE WAVEFORMS
PRR
5V
VIN
0
tPDHL
≈34V
90%
10%
tPDLH
VOUT
50%
50%
10%
90%
0V
tR
tF

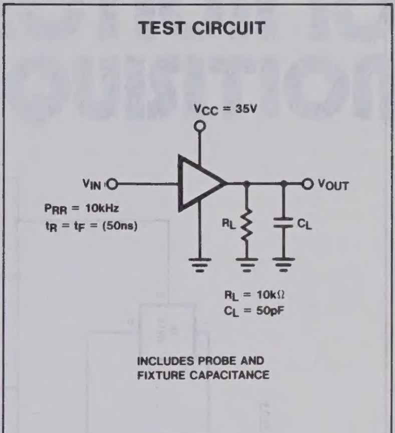
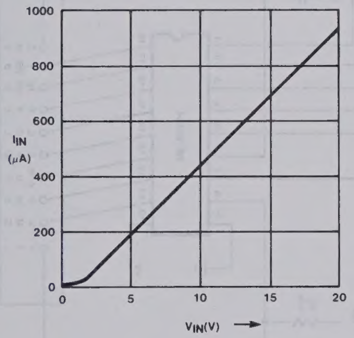
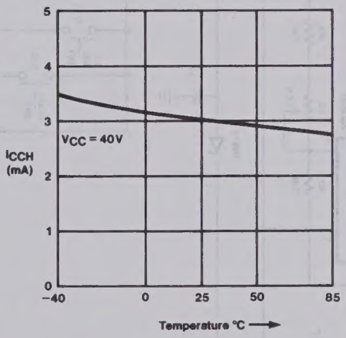
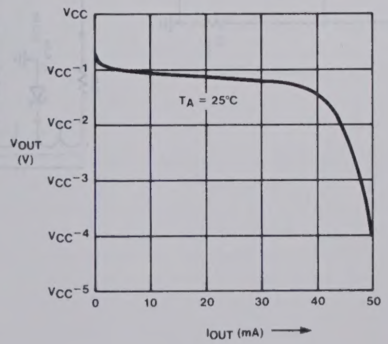

TEST CIRCUIT
VCC = 35V
VIN
VOUT
PRR = 10kHz
tR = tF = (50ns)
RL
CL
RL = 10kΩ
CL = 50pF
INCLUDES PROBE AND FIXTURE CAPACITANCE

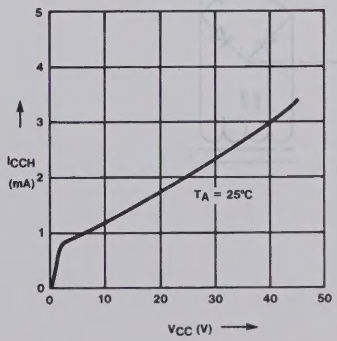
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS


I_{IN} VS V_{IN}


I_{CCH} VS TEMPERATURE


OUTPUT VOLTAGE VS OUTPUT CURRENT


I_{CC} VS V_{CC} (ALL INPUTS HIGH)

TYPICAL APPLICATION
DIGITAL CLOCK WITH ALARM

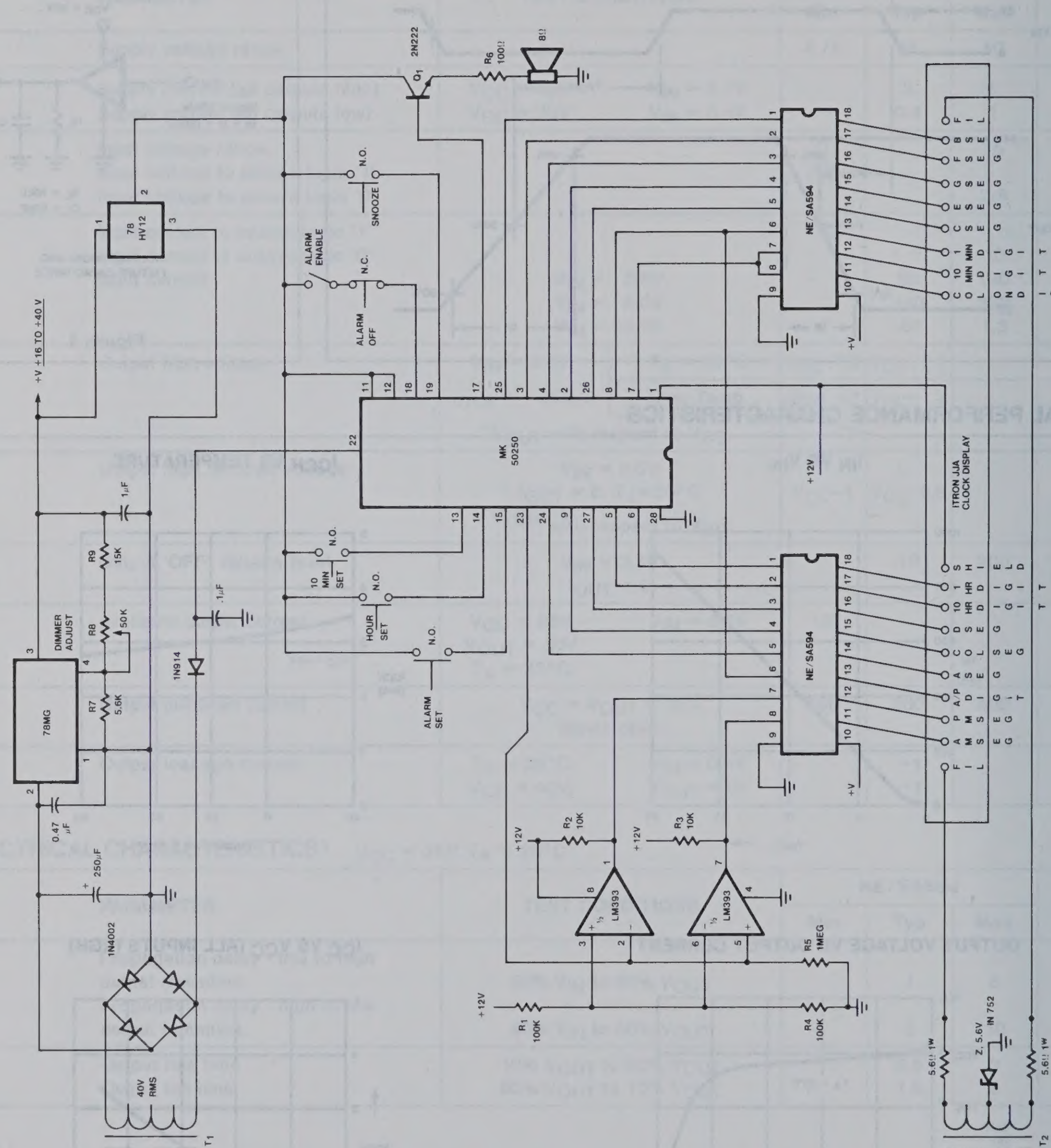

+V +16 TO +40V
78 HV12
78MG
DIMMER ADJUST
R7 5.6K
R8 50K
R9 15K
1µF
.1µF
1N914
0.47 µF
250µF
1N4002
40V RMS
T1
ALARM ENABLE
ALARM OFF
N.O.
N.C.
SNOOZE
10 MIN SET
HOUR SET
ALARM SET
2N222
Q1
R6 100Ω
8Ω
MK 50250
NE/SA594
NE/SA594
+12V
+V
ITRON JJA CLOCK DISPLAY
LM393
R1 100K
R2 10K
R3 10K
R4 100K
R5 1MEG
5.6Ω 1W
Z, 5.6V IN 752
T2
FIL
AM
PM
A/P SEG
COLON DIG
10 MIN DIG
1 MIN DIG
10 HR DIG
1 HR DIG
SEG A
SEG B
SEG C
SEG D
SEG E
SEG F
SEG G
DIG IT
FIL

Figure 2

SECTION 10
DATA ACQUISITION

Section 10—DATA ACQUISTION

DAC-08 SERIES 8-Bit High Speed Multiplying D/A Converter 313
LF398 Monolithic Sample and Hold Circuits 303
MC1508-8/1408-8/1408-7 8-Bit Multiplying D/A Converter 307
NE5007/5008/SE5008 8-Bit High Speed Multiplying D/A Converter 313
NE/SE5009 8-Bit High Speed Multiplying D/A Converter 318
NE/SE5018 8-Bit Microprocessor-Compatible D/A Converter 325
NE/SE5019 8-Bit Microprocessor-Compatible D/A Converter 330
NE/SE5118 8-Bit Microprocessor-Compatible D/A Converter-Current Output 335
NE/SE5119 8-Bit Microprocessor-Compatible D/A Converter-Current Output 339
NE5020 10-Bit Microprocessor-Compatible D/A Converter 343
NE/SE5537 Sample and Hold Amplifier 351

A/D–D/A CONVERTERS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low
1 is logic level high
X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Accuracy

The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination.

Monotonicity

For a 1 LSB increase of input code, the output either increases or remains the same.

Differential Linearity

The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero.

Absolute Accuracy

Error of a D/A converter output is the difference between the analog output expected and the actual output with a given code applied. Error of an A/D converter is the difference between the theoretical analog output required to produce a given output code and the actual input required to produce a given output code and the actual input required to produce that same code. The actual input is a range and the measured value is the midpoint of the measured band and the theoretical midpoint.

Resolution

The number of bits on the input or output of an A/D or D/A converter. The number of discrete steps or states is equal to 2^n when n is the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Quantizing Error

In an A/D converter, there is an infinite number of possible input voltages, but only 2^n output codes (n = number of bits). Therefore, there will be an error as great as 1/2LSB because of this quantizing effect and the greatest error will occur at the transition voltage where the output changes state.

No Missing Codes

This is a property of an A/D converter that is related to, but is more stringent than monotonicity. If a converter is guaranteed to have no missing codes, there will be no output digital state that will be skipped when the input voltage is varied over the entire range.

Most Significant Bit (MSB)

The highest-order bit or the bit with the greatest weight.

Least Significant Bit (LSB)

The lowest-order bit or the bit with the least weight.

Gain Error

The error in the input-to-output ratio, usually expressed in percent.

Offset Error

This is an error in the reference point of the transfer function. It appears as a constant amplitude error signal at a D/A output or an A/D input. It also appears as a constant frequency shift in the output of a V/F converter. It is nulled prior to adjusting gain error by setting the input to the most-negative input and adjusting the output to the proper value.

Settling Time

The time delay between a change of input signal value and the effected change in the output signal. It is usually expressed in terms of how long it takes the output to arrive at, and remain within, a certain error band around the final value and is often given for several different magnitudes of input step change.

Conversation Time

Time required for a complete measurement by an A/D converter. Conversion times are a function of the number of bits (resolution) and the clock frequency.

Switching Time

The time it takes for a multiplexer to change from one channel to the next with the new output signal being within a certain percentage of its final value. It is expressed for a maximum voltage transition.

Throughput Rate

An A/D converter or a data acquisition system has a finite number of points that it can convert in any given time. Throughput rate is an expression of that quantity. It is dependent on the time it takes to make a conversion and the time required to set up to make the next conversion. In a data acquisition system this time includes the composite delay due to switching and settling times of the mux, settling time of the amplifier and acquisition time of the sample-and-hold.

Full Scale Tempco

The change in DAC full scale current with change in temperature expressed in ppm/°C.

Differential Non-Linearity Tempco

The non-linearity specification over a specified range of temperatures. This specification generally appears as the range of temperatures that the device is monotonic (DAC) or has no missing codes (ADC).

Leakage Current

Multiplexer input current that does not flow through to the output but is shunted internally. It is also current that flows from OFF channels into the ON channel. In a current output D/A converter, there is a digital input code that ideally yields zero output current. If current flows with that input code, it is called leakage current. It is analogous to output voltage offset in a voltage-output D/A converter.

Power Supply Sensitivity

The change in DAC output current with changes in power supply voltage.

Output Voltage Compliance

The range of allowable voltage levels the output pins can assume without a major effect on circuit performance.

Compliance Voltage Range

For a current source the maximum range of terminal voltage for which the current source will maintain its specified values.

NOTE
Refer to Section 5 (Interface Circuits) of the 1979 Analog Applications Manual for an in-depth explanation of Converters and their applications

SIGNETICS D/A CONVERTER SELECTION GUIDE

			OUTPUT			INT.	INT.	PACKAGE		TEMPERATURE RANGE		RELIABILITY	
PRODUCT	# BITS	ACC. %	V	I	T	REF.	LATCH	N	F	Coml.	Mil	SURE II	SUPR II
MC1408-6	8	.78		X				X	X	X		X	
MC1408-7	8	.39		X				X	X	X		X	X
MC1408-8	8	19		X				X	X	X		X	X
MC1508-8	8	.19		X					X		X	X	X
NE5007	8	.39		X	X			X	X	X		X	X
NE5008	8	.19		X	X			X	X	X		X	X
NE5009	8	.1		X	X			X	X	X		X	X
SE5008	8	.19		X	X				X		X	X	X
SE5009	8	.1		X	X				X		X	X	X
NE5018	8	.19	X			X	X	X	X	X		X	X
NE5019	8	.1	X			X	X	X	X	X		X	X
SE5018	8	.19	X			X	X		X		X	X	X
SE5019	8	.1	X			X	X		X		X	X	X
NE5118	8	.19		X		X	X	X	X	X		X	
NE5119	8	.1		X		X	X	X	X	X		X	
SE5118	8	.19		X		X	X		X		X	X	
SE5119	8	.1		X		X	X		X		X	X	
NE5020	10	.1	X			X	X	X	X	X		X	

SIGNETICS REPLACEMENT STANDARDS

SE/NE 5018 DAC

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD Analog Devices Datel Fairchild Harris Precision National	8	Resolution (Bits)	8 Bits	NE5018 SE5018 NE5019 SE5019	Yes Yes Yes Yes	Yes Yes Yes Yes	*Not pin for pin replacement. Do not have total capability of the NE5018 μP compatible series.
	.19	Linearity	0.1 %				
	2-300 μ sec	Settling Time ½ LSB	2 μsec				
	10-50	Gain TC	20 PPM/°C				
	0-4	Current (Output)	mA	NE/SE 5118 NE/SE 5119	Yes Yes	Yes Yes	
	−10 to +18	Voltage (Output)	0-10 ±5 Volts	NE5018 SE5019	Yes Yes	Yes Yes	

DAC-08/08A

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD Analog Devices Datel Motorola National	8	Resolution	8 Bits	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	
	.19	Linearity	19 %FS	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	
	85-300	Settling time	135 nsec	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	
	48-500	Power supply regulator	48 mW	NE/SE5008 NE/SE5009	Yes Yes	Yes Yes	

DESCRIPTION

The Signetics LF398 is a monolithic sample and hold circuit which utilizes high-voltage Ion-Inplant JFET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.004% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF398 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

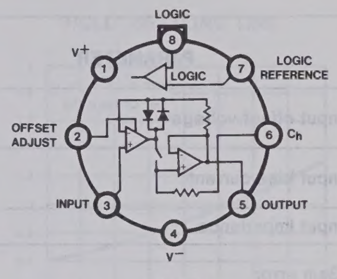
Logic inputs on the LF398 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF398 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package or an 8-pin plastic DIP.

FEATURES

- **Operates from ±5V to ±18V supplies**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at C_h = 0.01μF**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change**
  - **during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**
- **The LF398 is ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup.**

PIN CONFIGURATION

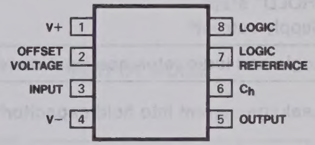
H PACKAGE



TOP VIEW

ORDER PART NO. LF398H,N

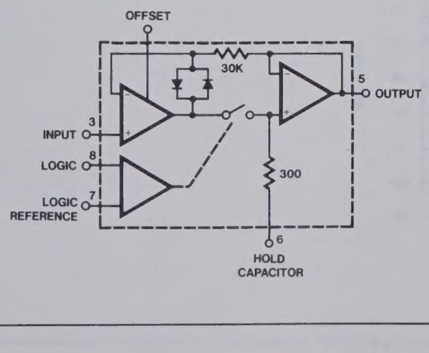
N PACKAGE



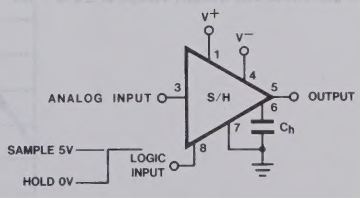
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range LF398	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = OV and logic voltage = 2.5V.

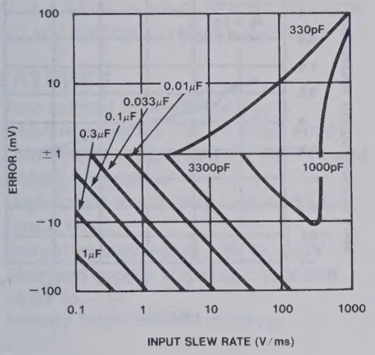
PARAMETER	TEST CONDITIONS	LF398 Min	LF398 Typ	LF398 Max	UNIT
Input offset voltage[6]	$T_j = 25°C$ Full temperature range		2	7 10	mV mV
Input bias current[6]	$T_j = 25°C$ Full temperature range		10	50 100	nA nA
Input impedance	$T_j = 25°C$		10^{10}		Ω
Gain error	$T_j = 25°C$, $R_L = 10K$ Full temperature range		0.004	0.01 0.02	% %
Feedthrough attenuation ratio at 1kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	80	90		dB
Output impedance	$T_j = 25°C$, "HOLD" mode Full temperature range		0.5	4 6	Ω Ω
"HOLD" step[4]	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		1.0	2.5	mV
Supply current[6]	$T_j \geq 25°C$		4.5	6.5	mA
Logic and logic reference input current	$T_j = 25°C$		2	10	μA
Leakage current into hold capacitor[6]	$T_j = 25°C$[5] Hold mode		30	200	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4 20		μs μs
Hold capacitor charging current	$V_{IN}-V_{OUT} = 2V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_j = 25°C$	0.8	1.4	2.4	V

NOTES

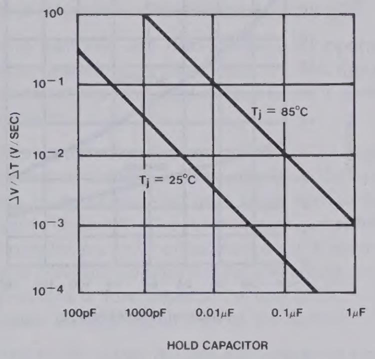
1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θjA) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k$. Logic reference voltage = OV and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. The parameters guaranteed over a supply voltage of ±5 to ±18V.

TYPICAL AC PERFORMANCE CHARACTERISTICS (cont'd)

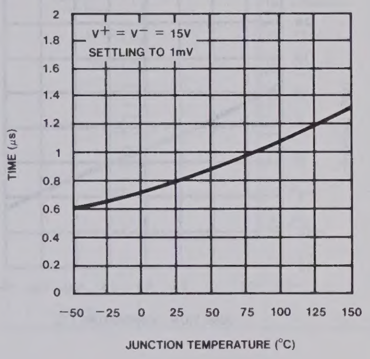
DYNAMIC SAMPLING ERROR



OUTPUT DROOP RATE

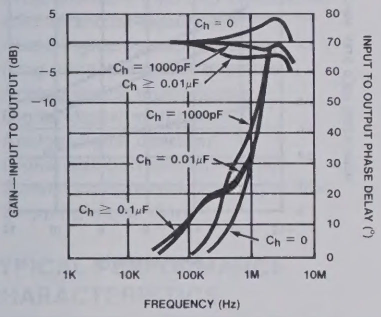


"HOLD" SETTLING TIME

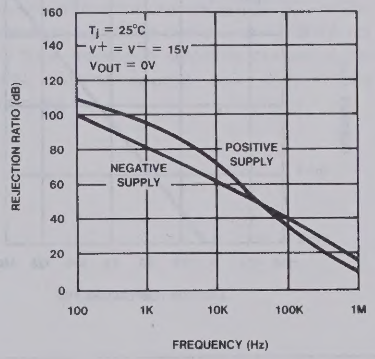


PHASE AND GAIN

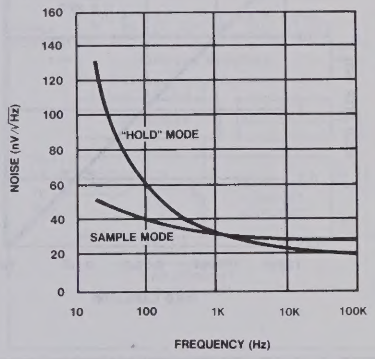
(INPUT TO OUTPUT, SMALL SIGNAL)



POWER SUPPLY REJECTION

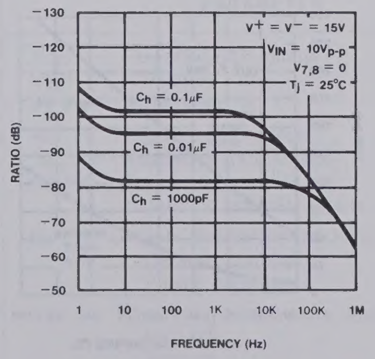


OUTPUT NOISE

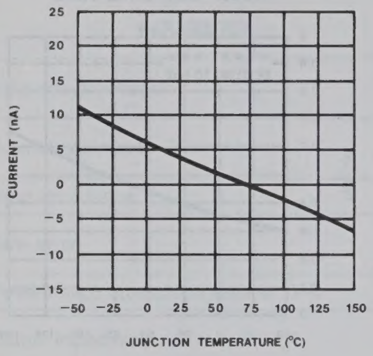


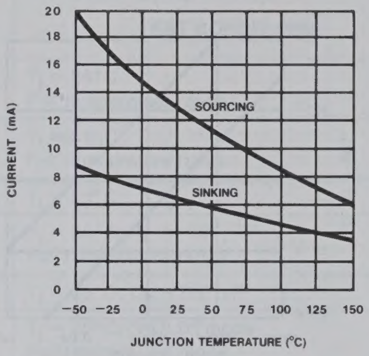
FEEDTHROUGH REJECTION RATIO

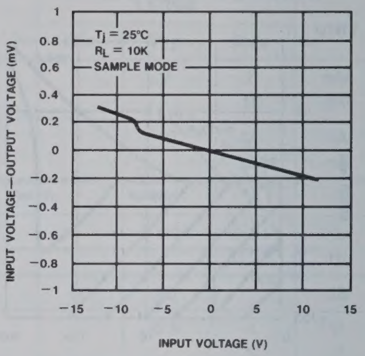
(HOLD MODE)

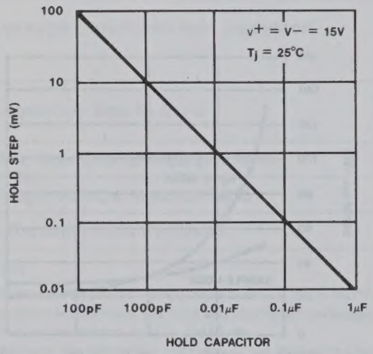


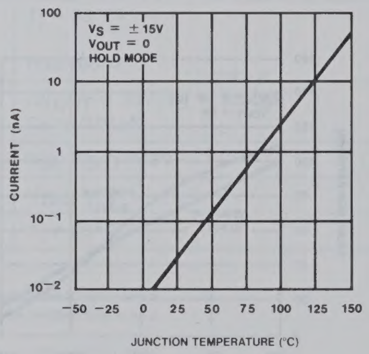
TYPICAL DC PERFORMANCE CHARACTERISTICS

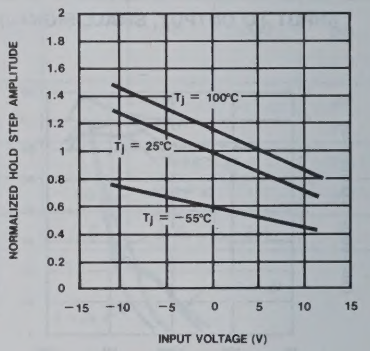

INPUT BIAS CURRENT


OUTPUT SHORT CIRCUIT CURRENT

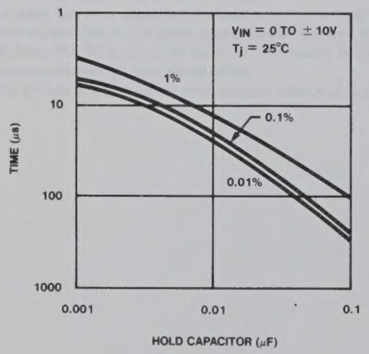

GAIN ERROR

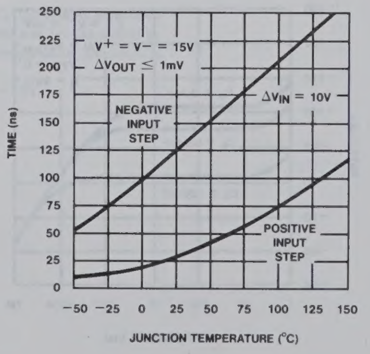

HOLD STEP

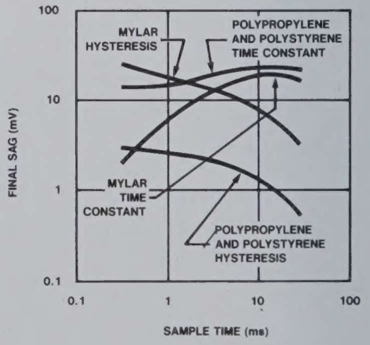

LEAKAGE CURRENT INTO HOLD CAPACITOR


HOLD STEP INPUT VOLTAGE

TYPICAL AC PERFORMANCE CHARACTERISTICS


ACQUISITION TIME


APERTURE TIME


CAPACITOR HYSTERESIS

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

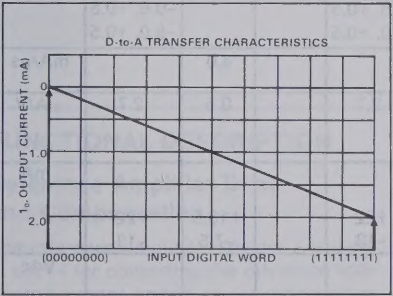
FEATURES

- **Fast settling time—300ns (typ)**
- **Relative accuracy ±0.19% (max error)**
- **Non-inverting digital inputs are TTL and CMOS compatible**
- **High speed multiplying rate 4.0mA/μs (input slew)**
- **Output voltage swing +.5V to -5.0V**
- **Standard supply voltages + 5.0V and -5.0V to -15V**
- **Military qualifications pending**

APPLICATIONS

- **Tracking A-to-D converters**
- **2½-digit panel meters and DVM's**
- **Waveform synthesis**
- **Sample and hold**
- **Peak detector**
- **Programmable gain and attenuation**
- **CRT character generation**
- **Audio digitizing and decoding**
- **Programmable power supplies**
- **Analog-digital multiplication**
- **Digital-digital multiplication**
- **Analog-digital division**
- **Digital addition and subtraction**
- **Speech compression and expansion**
- **Stepping motor drive**

TYPICAL PERFORMANCE CHARACTERISTICS



CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, and R-2R ladder, and 8 high speed current switches. For many applications, only a reference resistor and reference voltage need be added.

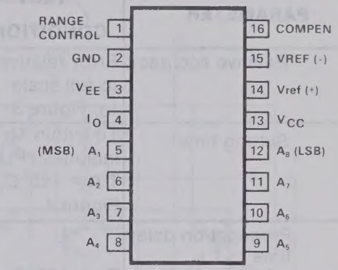
The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

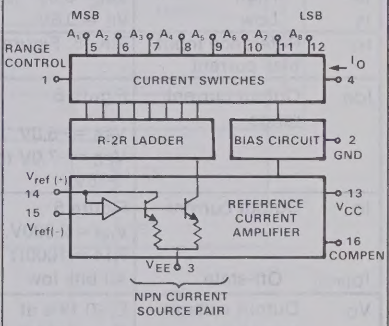
PIN CONFIGURATION

F,N PACKAGE*



*N = Plastic DIP
F = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATNGS

$T_A = +25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage		V
V_{EE}	Positive	+5.5	
V_5-V_{12}	Negative	-16.5	
V_O	Digital input voltage	+5.5, 0	V
I_{14}	Applied output voltage	+0.5, -5.2	V
V_{14},V_{15}	Reference current	5.0	mA
	Reference amplifier inputs	V_{CC}, V_{EE}	V
P_D	Power dissipation (package limitation)		mW
	Ceramic package	1000	
	Plastic package	800	
T_A	Operating temperature range		°C
	MC1508	-55 to +125	
	MC1408	0 to +75	
T_{stg}	Storage temperature range	-65 to +70	°C

DC ELECTRICAL CHARACTERISTICS[1]

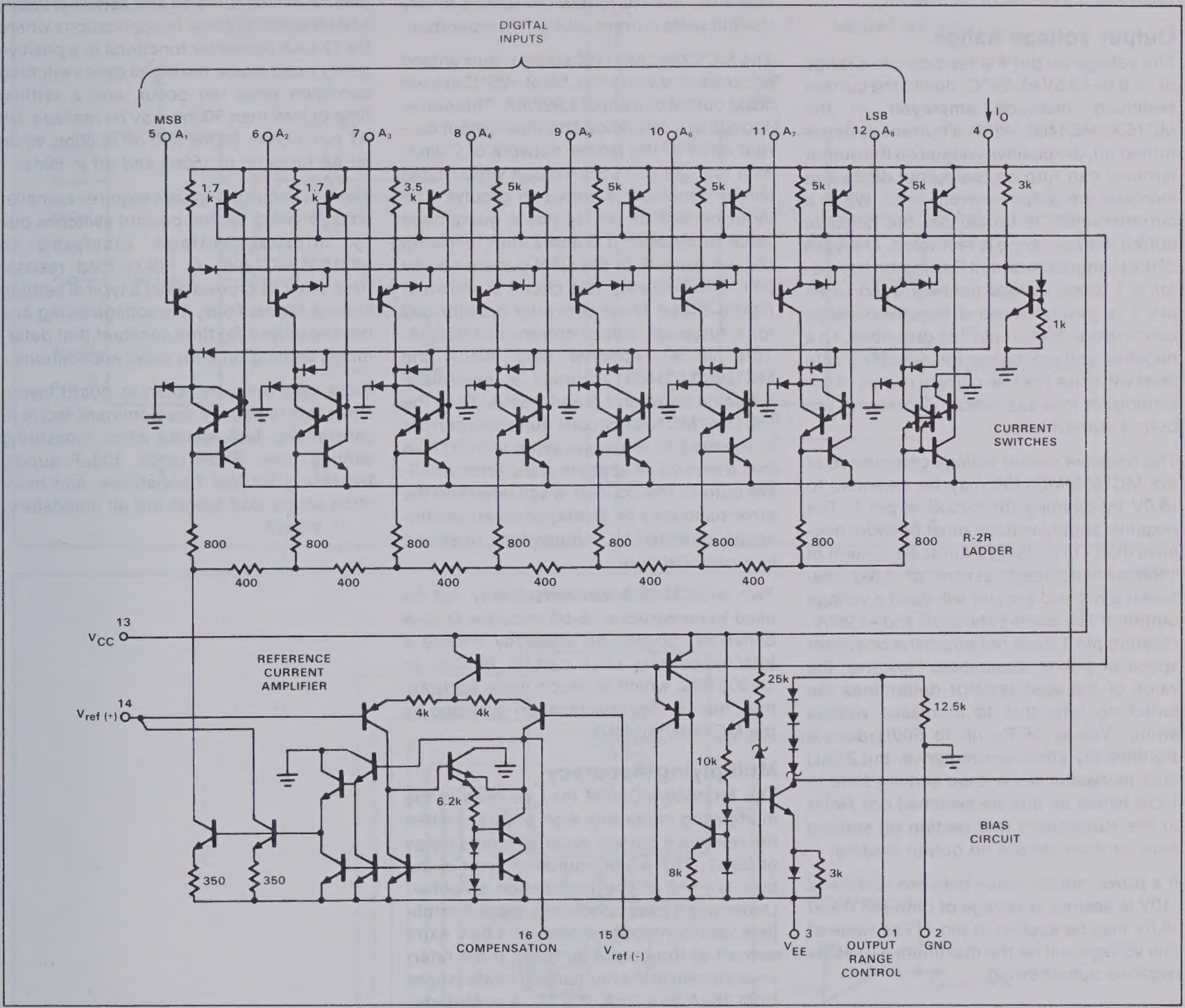
Pin 3 must be 3V more negative than the potential to which R_{15} is returned. $V_{CC} = +5.0Vdc$, $V_{EE} = -15Vdc$, $\frac{V_{ref}}{R_{14}} = 2.0mA$ unless otherwise specified.
MC1508: $T_A = -55°C$ to $125°C$. MC1408: $T_A = 0°C$ to $70°C$

PARAMETER		TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy	Error relative to full scale I_O, Figure 3			±0.19			±0.19			±0.39	%
t_s	Setting time[1]	To within 1/2 LSB, includes t'_{PLH}, $T'_A = +25°C$, Figure 4		300			300			300		ns
	Propagation delay time											ns
t_{PLH} t_{PHL}	Low-to-high High-to-low	$T_A = +25°C$, Figure 4		30	100		30	100		30	100	
TCI_O	Output full scale current drift			-20			-20			-20		PPM/°C
	Digital input logic level (MSB)											Vdc
V_{IH}	High	Figure 5	2.0			2.0			2.0			
V_{IL}	Low				0.8			0.8			0.8	
	Digital input current (MSB)	Figure 5										mA
I_{IH}	High	$V_{IH} = 5.0V$		0	0.04		0	0.04		0	0.04	
I_{IL}	Low	$V_{IL} = 0.8V$		-0.4	-0.8		-0.4	-0.8		-0.4	-0.8	
I_{15}	Reference input bias current	Pin 15, Figure 5		-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	µA
I_{OR}	Output current range	Figure 5										mA
		$V_{EE} = -5.0V$	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	
		$V_{EE} = -7.0V$ to $-15V$	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
I_O	Output current	Figure 5 $V_{ref} = 2.000V$, $R14 = 1000\Omega$	1.9	1.99	2.1	1.9	1.99	2.1	1.9	1.99	2.1	mA
$I_{O(min)}$	Off-state	All bits low		0	4.0		0	4.0		0	4.0	µA
V_O	Output voltage compliance	$E_r \leq 0.19\%$ at $T_A = +25°C$, Figure 5										Vdc
		$V_{EE} = -5V$			-0.6, +0.5			-0.6, +0.5			-0.6, +0.5	
		V_{EE} below -10V			-5.0, +0.5			-5.0, +0.5			-5.0, +0.5	
SRI_{ref}	Reference current slew rate	Figure 6		4.0			4.0			4.0		mA/µs
$PSRR_{(-)}$	Output current power supply sensitivity	$I_{ref} = 1mA$		0.5	2.7		0.5	2.7		0.5	2.7	µA/V
	Power supply current											mA
I_{CC}	Positive	All bits low,		+13.5	+22		+13.5	+22		+13.5	+22	
I_{EE}	Negative	Figure 5		-7.5	-13		-7.5	-13		-7.5	-13	
	Power supply voltage range											Vdc
V_{CCR}	Positive	$T_A = +25°C$,	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	
V_{EER}	Negative	Figure 5	-4.5	-15	-16.5	-4.5	-15	-16.5	-4.5	-15	-16.5	
P_D	Power dissipation	All bits low, Figure 5										mW
		$V_{EE} = -5.0Vdc$		105	170		105	170		105	170	
		$V_{EE} = -15Vdc$		190	305		190	305		190	305	
		All bits high, Figure 5										
		$V_{EE} = -5.0Vdc$		90			90			90		
		$V_{EE} = -15Vdc$		160			160			160		

NOTES

1. All bits switched

EQUIVALENT CIRCUIT SCHEMATIC


DIGITAL INPUTS
MSB
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
LSB
12 A8
4 IO
1.7 k
1.7 k
3.5 k
5k
5k
5k
5k
5k
3k
1k
CURRENT SWITCHES
800
800
800
800
800
800
800
800
R-2R LADDER
400
400
400
400
400
400
13
VCC
REFERENCE CURRENT AMPLIFIER
14
Vref (+)
4k
4k
25k
12.5k
6.2k
10k
8k
3k
BIAS CIRCUIT
350
350
16 COMPENSATION
15 Vref (-)
3 VEE
1 OUTPUT RANGE CONTROL
2 GND

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current (I_{14}) must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown in Figure 2. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the 2 resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high inpedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.6 to +0.5V at -24°C, due to the current switching methods employed in the MC1508/MC1408. When a current switch is turned off, the positive voltage on the output terminal can turn on the output diode and increase the output current level. When a current switch is turned on, the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is 1 diode voltage below ground when pin 1 is grounded, so a negative voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508/MC1408 may be extended to -5.0V by opening the circuit at pin 1. The negative supply voltage must be more negative than -10V. Using a full scale current of 1.992mA and load resistor of 2.5kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but 2.5kΩ load increases worst case settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section on settling time for more details on output loading.

If a power supply value between -5.0V and -10V is desired, a voltage of between 0 and -5.0V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than -7.0V, due to the increased voltage drop across the 350Ω resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508/MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1508/MC1408 has a very low full scale current drift with temperature.

The MC1508/±MC1408 series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of 1 LSB = 8.0μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the MC1508/MC1408 accuracy is essentially the same between 1.5 and 2.5mA. Then the MC1508/MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total error ±1/2 of 1 part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1508/MC1408.

Multiplying Accuracy

The MC1508/MC1408 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under worst case conditions, these 8 amplifiers can contribute a total of 1.6μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the 1.6μA contributes an error of 0.1 LSB. This is well within 8-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508/MC1408 in monotonic for all values of reference current above 0.5mA. The recommended range for operation with a dc reference current is 0.5 to 4.0mA.

Settling Time

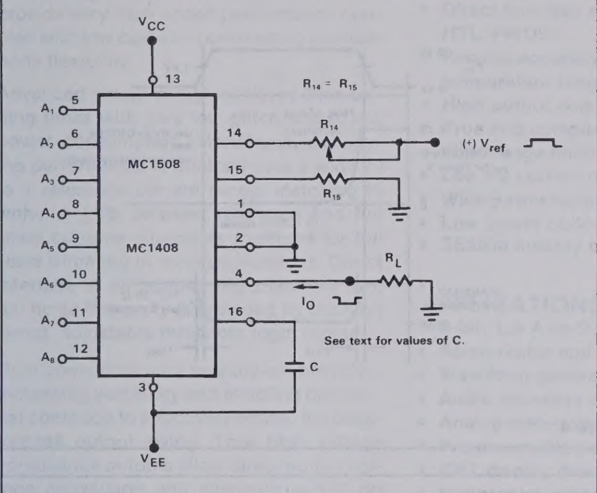
The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all bits. This time is typically 300ns for settling to within ±1/2 LSB for 8-bit accuracy and 200ns to 1/2 LSB for 7-bit accuracy. The turnoff is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and C_O 25pF.

The slowest single switch is the least significant bit, which turns on and settles in 250ns and truns off in 80ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst case switching condition does not occur, and a settling time of less than 300ns may be realized. Bit A7 turns on in 200ns and off in 80ns, while bit A6 turns on in 150ns and off in 80ns.

The test circuit of Figure 4 requires a smaller voltage swing for the current switches due to internal voltage clamping in MC1508/MC1408. A 1.0kΩ load resistor from pin 4 to ground gives a typical settling time of 400ns. Thus, it is voltage swing and not the output R_C time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

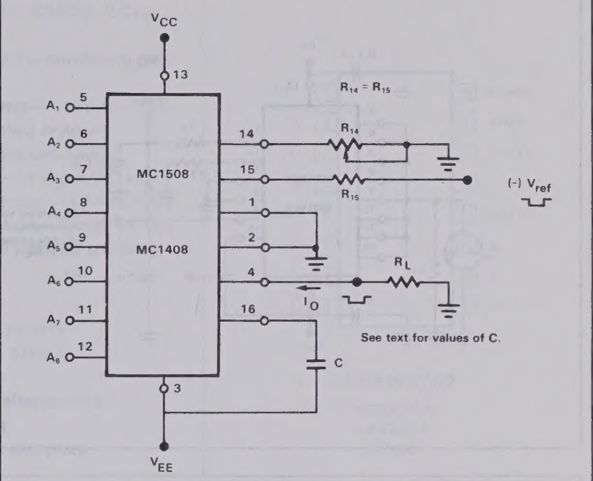
TEST CIRCUITS


POSITIVE Vref

VCC
13
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
MC1508
MC1408
R14 = R15
R14
R15
14
15
1
2
4
16
3
(+) Vref
RL
IO
C
VEE

See text for values of C.

Figure 1


NEGATIVE Vref

VCC
13
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
MC1508
MC1408
R14 = R15
R14
R15
14
15
1
2
4
16
3
(-) Vref
RL
IO
C
VEE

See text for values of C.

Figure 2

RELATIVE ACCURACY

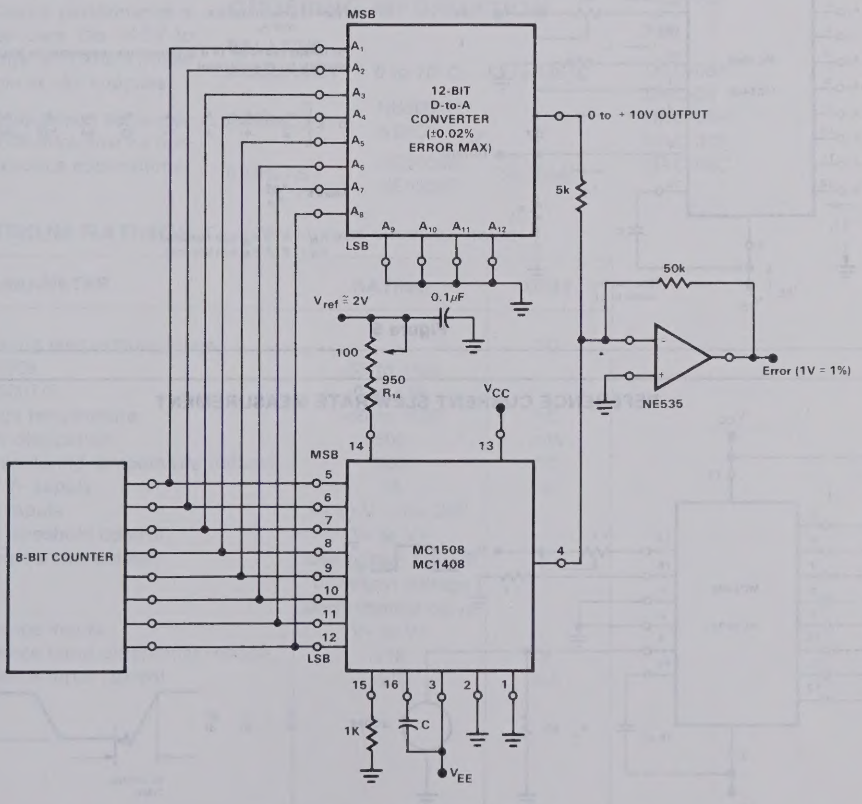

MSB
A1
A2
A3
A4
A5
A6
A7
A8
LSB
A9
A10
A11
A12
12-BIT D-to-A CONVERTER (±0.02% ERROR MAX)
0 to +10V OUTPUT
5k
50k
Vref ≅ 2V
0.1μF
100
950 R14
VCC
14
13
MSB
5
6
7
8
9
10
11
12
LSB
8-BIT COUNTER
MC1508
MC1408
4
NE535
Error (1V = 1%)
15
16
3
2
1
1K
C
VEE

Figure 3

TEST CIRCUITS (Cont'd)

TRANSIENT RESPONSE AND SETTLING TIME

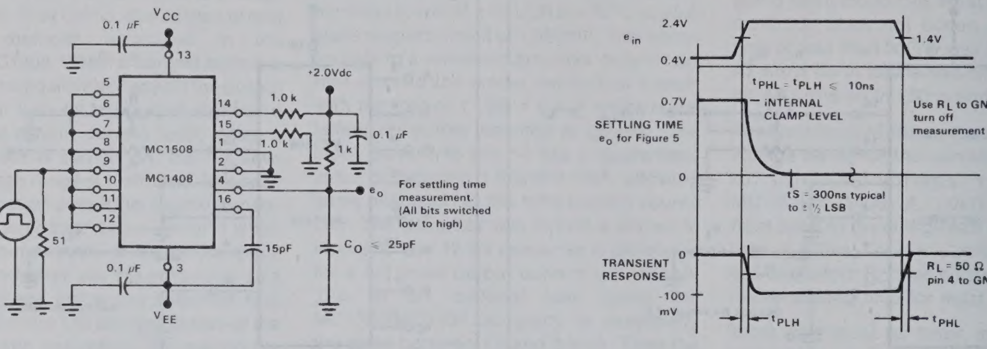
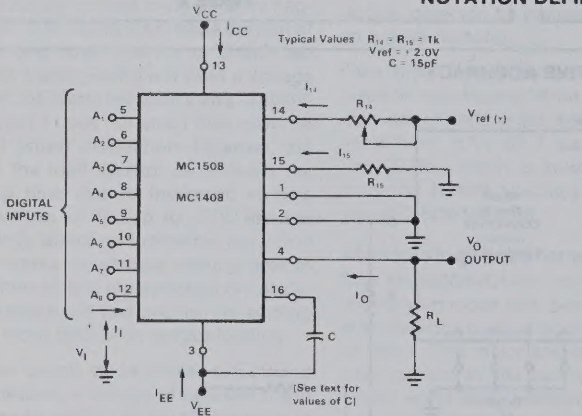

V_CC
0.1 μF
13
5
6
7
8
9
10
11
12
MC1508
MC1408
14
15
1
2
4
16
+2.0Vdc
1.0 k
1.0 k
0.1 μF
1 k
e_o
For settling time measurement. (All bits switched low to high)
e_in
51
0.1 μF
3
V_EE
15pF
C_O ≤ 25pF
2.4V
e_in
0.4V
1.4V
t_PHL = t_PLH ≤ 10ns
0.7V
INTERNAL CLAMP LEVEL
Use R_L to GND for turn off measurement (see text).
SETTLING TIME e_o for Figure 5
0
tS = 300ns typical to ± ½ LSB
TRANSIENT RESPONSE
0
R_L = 50 Ω pin 4 to GND
-100 mV
t_PLH
t_PHL

Figure 4

NOTATION DEFINITIONS


V_CC
I_CC
Typical Values R_14 = R_15 = 1k
V_ref = + 2.0V
C = 15pF
13
I_14
A_1 5
14
R_14
V_ref (+)
A_2 6
A_3 7
15
I_15
MC1508
R_15
A_4 8
MC1408
1
DIGITAL INPUTS
A_5 9
2
A_6 10
V_O OUTPUT
4
A_7 11
A_8 12
16
I_O
R_L
I_I
C
V_I
3
I_EE
V_EE
(See text for values of C)

V_I and I_I apply to inputs A_1 thru A_8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{128}+\frac{A_8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R_{14}}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

Figure 5

REFERENCE CURRENT SLEW RATE MEASUREMENT

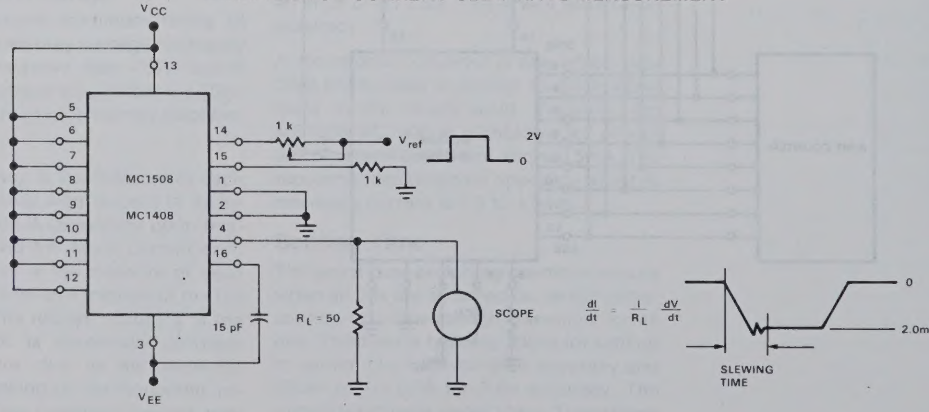

V_CC
13
5
6
7
8
9
10
11
12
MC1508
MC1408
14
15
1
2
4
16
1 k
V_ref
2V
0
1 k
15 pF
R_L = 50
SCOPE
3
V_EE
dI/dt = 1/R_L · dV/dt
0
2.0mA
SLEWING TIME

Figure 6

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER NE5007/5008/SE5008

NE5007/5008-F,N
SE5008-F

DESCRIPTION

The 5007/5008 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All 5007/5008 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the 5007/5008 attractive for portable and military/aerospace applications.

FEATURES

- **Fast settling output current—85ns**
- **Full scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance—-10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift—±10ppm/°C**
- **Wide power supply range—±4.5V to ±18V**
- **Low power consumption—33mW at ±5V**
- **SE5008 military qualifications pending**

APPLICATIONS

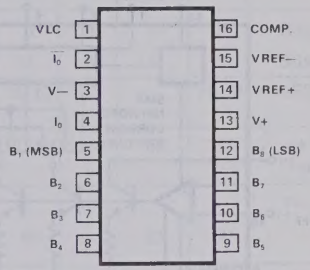
- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	-55 to 125°C
0.39% FS	NE5007N NE5007F	–
0.19% FS	NE5008N NE5008F	SE5008F

PIN CONFIGURATION

F,N PACKAGE



ORDER PART NO.

NE5007F,N
NE5008F,N
SE5008F

CROSS REFERENCE

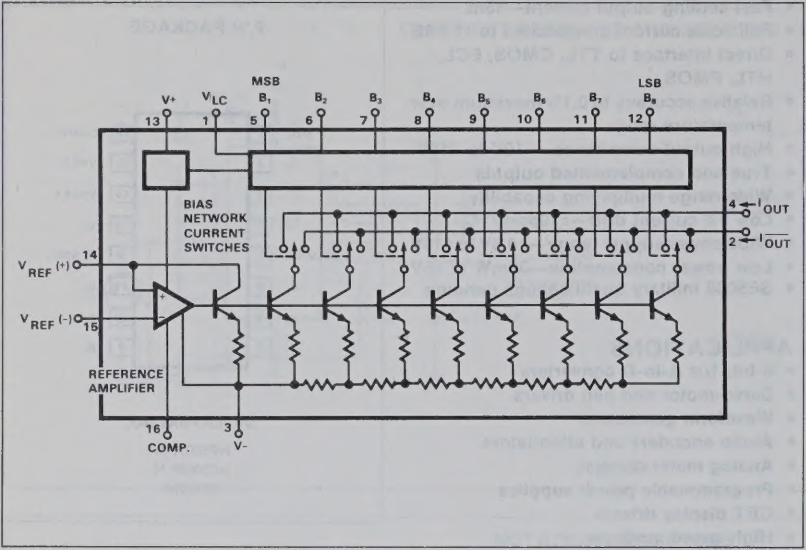
The 5007/5008 series are pin and functionally compatible with the DAC-08 series of devices.

PMI	SIGNETICS
DAC-08A	SE5009
DAC-08	SE5008
DAC-08H	NE5009
DAC-08E	NE5008
DAC-08C	NE5007

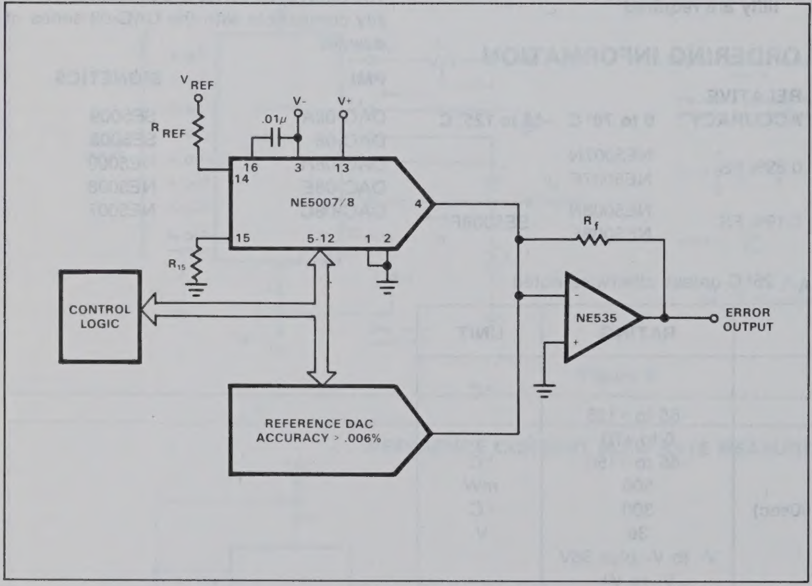
ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

	PARAMETER	RATING	UNIT
T_A	Operating temperature range		°C
	SE5008	-55 to +125	
	NE5007/8	0 to +70	
t_{stg}	Storage temperature	-65 to +150	°C
P_D	Power dissipation	500	mW
	Lead soldering temperature (60sec)	300	°C
	V+ to V- supply	36	V
	Logic inputs	V- to V- plus 36V	
V_{LC}	Logic threshold control	V- to V+	
	Analog current outputs	See output current or output voltage performance curve	
V_{14}, V_{15}	Reference inputs	V- to V+	
V_{14} to V_{15}	Reference input differential voltage	±18	V
I_{14}	Reference input current	5.0	mA

BLOCK DIAGRAM


MSB
LSB
V+
V_{LC}
B_1
B_2
B_3
B_4
B_5
B_6
B_7
B_8
13
1
5
6
7
8
9
10
11
12
BIAS NETWORK
CURRENT SWITCHES
4
I_{OUT}
2
$\overline{I_{OUT}}$
V_{REF} (+)
14
V_{REF} (-)
15
REFERENCE AMPLIFIER
16
COMP.
3
V-

TEST CIRCUIT


V_{REF}
R_{REF}
.01μ
V-
V+
16
3
13
14
NE5007/8
4
15
5-12
1
2
R_{15}
R_1
CONTROL LOGIC
NE535
ERROR OUTPUT
REFERENCE DAC ACCURACY > .006%

ELECTRICAL CHARACTERISTICS

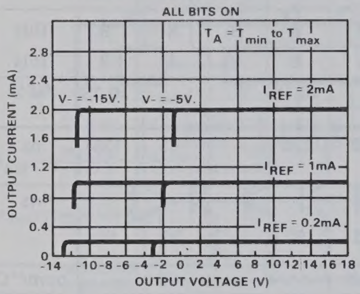
Pin 3 must be 3V more negative than the potential to which R_{15} is returned. $V_S = \pm15V$, $I_{REF} = 2.0mA$, Output characteristics refer to both IOUT and $\overline{IOUT}$ unless otherwise noted. NE5008: $T_A = 0°C$ to $70°C$. SE5008: $T_A = -55°C$ to $125°C$.

PARAMETER		TEST CONDITIONS	NE5007			NE5008			SE5008			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity*		8	8	8	8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19			±0.19	%FS
t_S	Settling time	To ±½ LSB, all bits switched on or off, T_A=25°C		85	135		85	135		85	135	ns
	Propagation delay											ns
t_{PLH}	Low-to-high	T_A=25°C, each bit.										
t_{PHL}	High-to-low	All bits switched		35	60		35	60		35	60	
TCI_{FS}	Full scale tempco			±10			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full scale current change <½ LSB	-10		+18	-10		+18	-10		+18	V
I_{FS4}	Full scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ, T_A=25°C	1.94	1.99	2.04	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full scale symmetry	$I_{FS4}-I_{FS2}$		±2.0	±16		±1.0	±8.0		±1.0	±8.0	μA
I_{ZS}	Zero scale current			0.2	4.0		0.2	2.0		0.2	2.0	μA
I_{FSR}	Output current	V−=−5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V−=−7.0V to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
	Logic input levels											V
V_{IL}	Low	V_{LC}=0V			0.8			0.8			0.8	
V_{IH}	High		2.0			2.0			2.0			
	Logic input current	V_{LC}=0V										μA
I_{IL}	Low	V_{IN}=−10V to +0.8V		-2.0	-10		-2.0	-10		-2.0	-10	
I_{IH}	High	V_{IN}=2.0V to 18V		0.002	10		0.002	10		0.002	10	
V_{IS}	Logic input swing	V−=−15V	-10		+18	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
dI/dt	Reference input slew rate	Figures 1, 3	4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
	Power supply sensitivity	I_{REF}=1mA										%FS/%VS
$PSSI_{FS+}$	Positive	V+=4.5 to 5.5V, V−=−15V; V+=13.5 to 16.5V, V−=−15V		0.0003	0.01		0.0003	0.01		0.0003	0.01	
$PSSI_{FS-}$	Negative	V−=−4.5 to −5.5V, V+=+15V; V−=−13.5 to −16.5, V+=+15V		0.002	0.01		0.002	0.01		0.002	0.01	
	Power supply current											mA
I+	Positive	V_S=±5V, IREF=1.0mA		2.3	3.8		2.3	3.8		2.3	3.8	
I−	Negative			-4.3	-5.8		-4.3	-5.8		-4.3	-5.8	
I+	Positive	V_S=+5V, −15V, I_{REF}=2.0mA		2.4	3.8		2.4	3.8		2.4	3.8	
I−	Negative			-6.4	-7.8		-6.4	-7.8		-6.4	-7.8	
I+	Positive	V_S=±15V, I_{REF}=2.0mA		2.5	3.8		2.5	3.8		2.5	3.8	
I−	Negative			-6.5	-7.8		-6.5	-7.8		-6.5	-7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA		33	48		33	48		33	48	mW
		+5V, −15V, I_{REF}=2.0mA		108	136		108	136		108	136	
		±15V, I_{REF}=2.0mA		135	174		135	174		135	174	

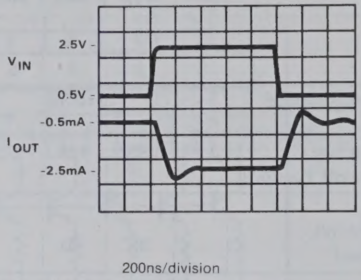
NOTE *NE5007 must have a minimum reference current of .8μA.

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

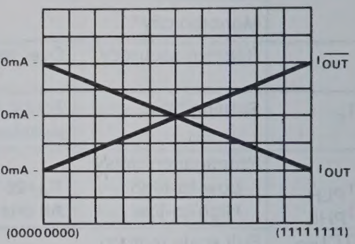


FAST PULSED REFERENCE OPERATION

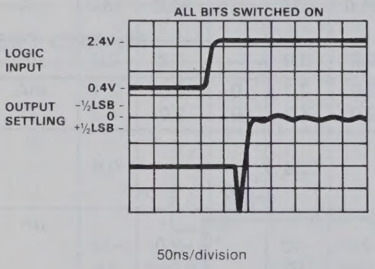


$R_{EQ} = 200\Omega$, $R_L = 100\Omega$, CC = O

TRUE AND COMPLEMENTARY OUTPUT OPERATION

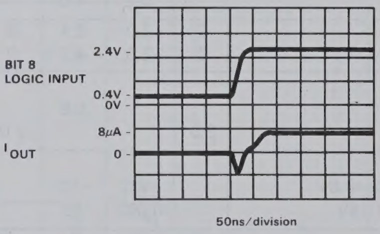


FULL SCALE SETTLING TIME

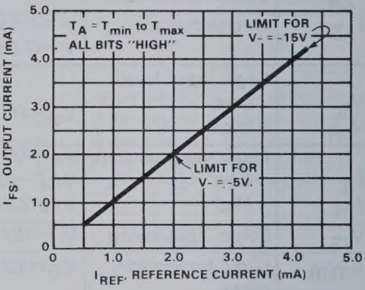


IFS = 2mA, $R_L = 1k\Omega$ 1/2 LSB = 4μA

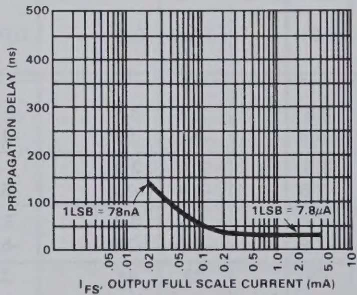
LSB SWITCHING



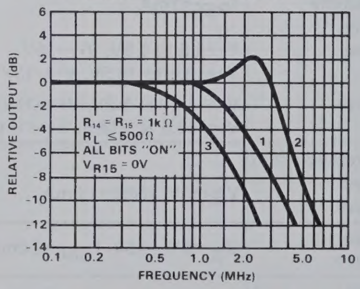
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



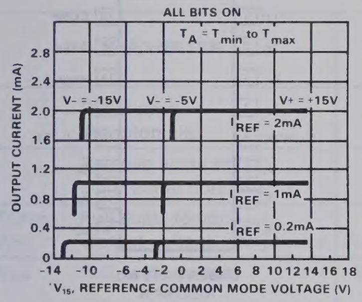
REFERENCE INPUT FREQUENCY RESPONSE



Curve 1: CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.
Curve 2: CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.
Curve 3: CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14}.

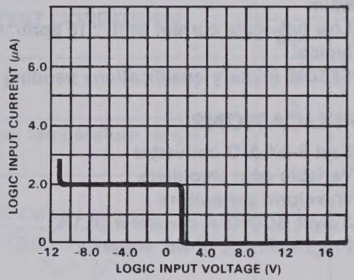
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REFERENCE AMP COMMON MODE RANGE

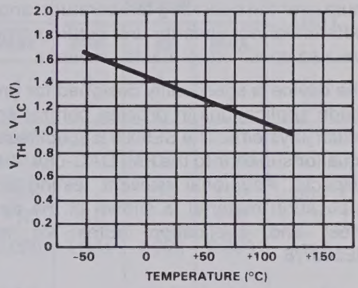


Positive common mode range is always (V+) – 1.5V

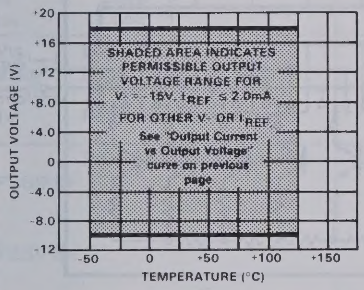
LOGIC INPUT CURRENT vs INPUT VOLTAGE



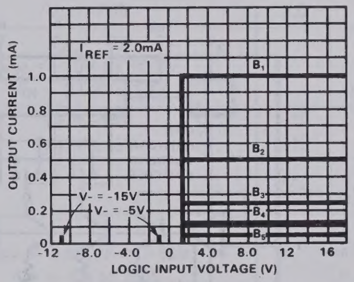
$V_{TH} - V_{LC}$ vs TEMPERATURE



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



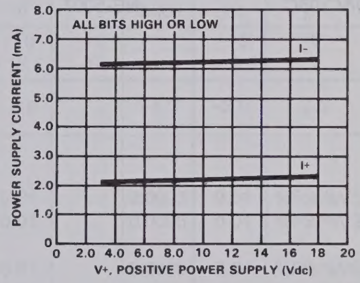
BIT TRANSFER CHARACTERISTICS



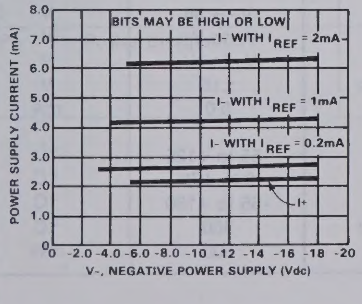
NOTE

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than ½ LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 volts over the operating temperature range (VLC = 0.0V).

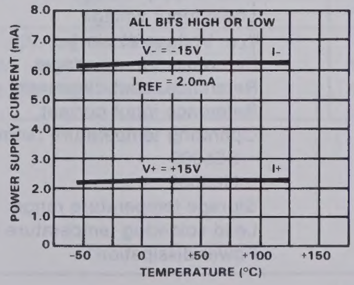
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V-

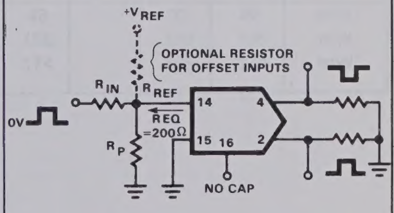


POWER SUPPLY CURRENT vs TEMPERATURE



TYPICAL APPLICATION

PULSED REFERENCE OPERATION



TYPICAL VALUES

R_{IN} = 5K
$+V_{IN}$ = 10V

NE5009-F,N • SE5009-F

DESCRIPTION

The 5009 monolithic 8-bit digital-to-analog converter is an electrical selection of the 5007/8 series of 8-bit D/A converters. Relative accuracy is specified to ±1/4 LSB maximum over the operating temperature range. Differential nonlinearity and settling times are also specified to maximum limits.

The device is specifically designed for precision applications in process control and military systems. The SE5009 is specified as equal or superior to the PMI DAC-08A in all respects. Additional relevant testing and application material is shown in the data sheet and application notes for the NE5007/8.

CROSS REFERENCE

The 5009 series are pin and functionally compatible with the DAC-08 series of devices.

PMI	SIGNETICS
DAC-08A	SE-5009
DAC-08	SE-5008
DAC-08H	NE-5009
DAC-08E	NE-5008
DAC-08C	NE-5007

FEATURES

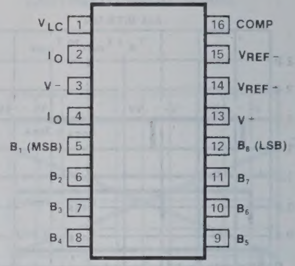
- **Fast settling output current—60ns typical, 135ns maximum**
- **Relative accuracy— ±0.1% maximum**
- **Differential nonlinearity—±0.19% maximum**
- **Low full-scale current drift, ±10 ppm/°C typical**
- **SE5009 military qualifications pending**

APPLICATIONS

- **Fast 8-bit A/D converter**
- **Variable gain amplifiers**
- **Waveform generators**
- **3 digit BCD D/A converter (0.1%)**
- **Programmable power supplies**

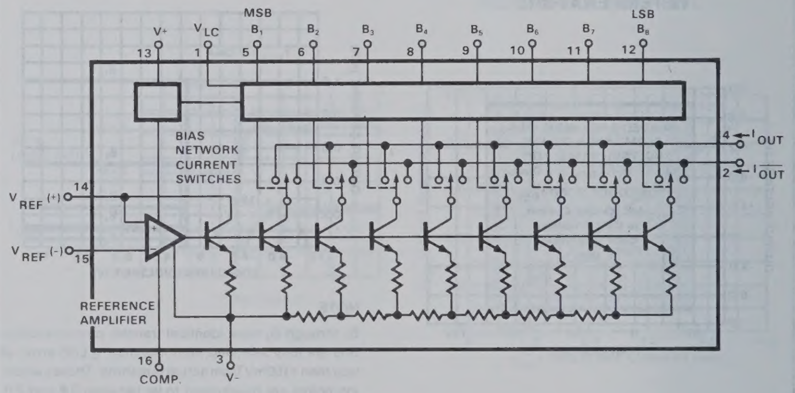
PIN CONFIGURATION

F,N PACKAGE*


V_{LC} 1
I_O 2
V- 3
I_O 4
B_1 (MSB) 5
B_2 6
B_3 7
B_4 8
16 COMP
15 V_{REF} -
14 V_{REF} +
13 V+
12 B_8 (LSB)
11 B_7
10 B_6
9 B_5

ORDER PART NO.
NE5009F,N
SE5009F

EQUIVALENT SCHEMATIC


MSB
LSB
V+
V_{LC}
B_1
B_2
B_3
B_4
B_5
B_6
B_7
B_8
13
1
5
6
7
8
9
10
11
12
BIAS NETWORK CURRENT SWITCHES
4 I_{OUT}
2 $\overline{I_{OUT}}$
V_{REF} (+) 14
V_{REF} (-) 15
REFERENCE AMPLIFIER
16 COMP.
3 V-

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Total supply voltage (V+ - V-)	36	V
Logic input voltage	V- + 36	V
V_{LC} Voltage at pin 1	V- to V+	V
Reference input voltage	V- to V+	V
Reference input differential voltage	±18	V
Reference input current	5.0	mA
Operating temperature range		
SE5009	-55 to +125	°C
NE5009	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead soldering temperature (10sec)	300	°C
Power dissipation*	500	mW

NOTE

*Derate F package at 10mW/°C above 100°C.

DC ELECTRICAL CHARACTERISTICS

Pin 3 must be 3V more negative than the potential to which R_{15} is returned.
These specs apply for $V_S = \pm 15V$, $I_{REF} = 2mA$,
T_A for NE5009 0° to 70°C, T_A for SE5009 -55° to +125°C.
Output characteristic for both I_{OUT} and $\overline{I_{OUT}}$.

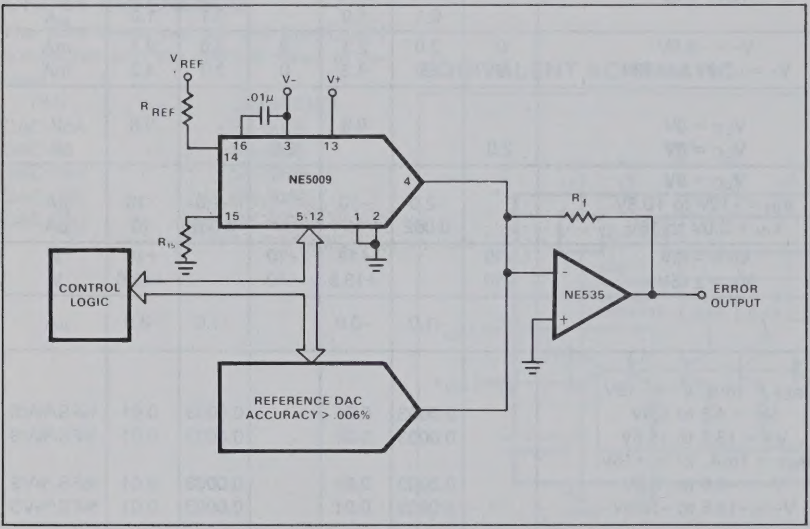
	PARAMETER	TEST CONDITIONS	NE5009			SE5009			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	bits
	Monotonicity		8	8	8	8	8	8	bits
	Relative accuracy	Over temperature range			±0.1			±0.1	% FS
	Differential nonlinearity			±0.1	±0.19		±0.1	±0.19	% FS
TCI_{FS}	Full scale tempco			±10	±50		±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full scale current change < 1/2 LSB	-10		+18	-10		+18	V
I_{FS4}	Full scale current	$V_{REF} = 10.000V$, $R_{14} \cdot R_{15} = 5.000K$ $T_A = 25°C$	1.984	1.992	2.000	1.984	1.992	2.000	mA
I_{FSS}	Full scale symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±0.5	±4.0	μA
I_{ZS}	Zero scale current			0.1	1.0		0.1	1.0	μA
I_{FSR}	Output current range	$V- = -5.0V$	0	2.0	2.1	0	2.0	2.1	mA
		$V- = -7.0V$ to $-18V$	0	2.0	4.2	0	2.0	4.2	mA
	Logic input levels								
V_{IL}	Logic "0"	$V_{LC} = 0V$			0.8			0.8	V
V_{IH}	Logic "1"	$V_{LC} = 0V$	2.0			2.0			V
	Logic input current	$V_{LC} = 0V$							
I_{IL}	Logic "0"	$V_{IN} = -10V$ to $+0.8V$		-2.0	-10		-2.0	-10	μA
I_{IH}	Logic "1"	$V_{IN} = 2.0V$ to $18V$		0.002	10		0.002	10	μA
V_{IS}	Logic input swing	$V- = -15V$	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	$V_S = \pm 15V$	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0	μA
	Power supply sensitivity								
PSSIFS+		$I_{REF} = 1mA$, $V- = -15V$:							
		$V+ = 4.5$ to $5.5V$		0.0003	0.01		0.0003	0.01	%FS/%VS
		$V+ = 13.5$ to $16.5V$		0.0003	0.01		0.0003	0.01	%FS/%VS
PSSIFS-		$I_{REF} = 1mA$, $V+ = +15V$:							
		$V- = -4.5$ to $-5.5V$		0.0003	0.01		0.0003	0.01	%FS/%VS
		$V- = -13.5$ to $-16.5V$		0.0003	0.01		0.0003	0.01	%FS/%VS
	Power supply current	$V_S = \pm 15V$, $I_{REF} = 1.0mA$							
I+				2.3	3.8		2.3	3.8	mA
I-				-4.3	-5.8		-4.3	-5.8	mA
	Power supply current	$V_S = +5V, -15V$; $I_{REF} = 2.0mA$							
I+				2.4	3.8		2.4	3.8	mA
I-				-6.4	-7.8		-6.4	-7.8	mA
	Power supply current	$V_S = \pm 15V$, $I_{REF} = 2.0mA$							
I+				2.5	3.8		2.5	3.8	mA
I-				-6.5	-7.8		-6.5	-7.8	mA
P_D	Power dissipation	$\pm 5V$, $I_{REF} = 1.0mA$		33	48		33	48	mW
		$+5V, -15V$, $I_{REF} = 2.0mA$		108	136		108	136	mW
		$\pm 15V$, $I_{REF} = 2.0mA$		135	174		135	174	mW

AC ELECTRICAL CHARACTERISTICS

These specs apply for $V_S = \pm 15V$, $I_{REF} = 2mA$, Output characteristic for both I_{OUT} and $\overline{I_{OUT}}$.

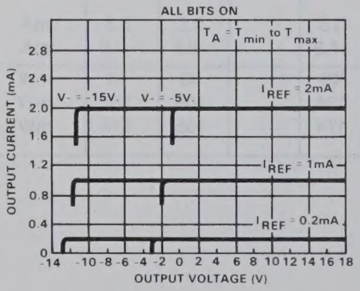
PARAMETER		TEST CONDITIONS	SE/NE5009			UNIT
			Min	Typ	Max	
t_s	Settling time	To ±1/2 LSB all bits switched ON or OFF, $T_A = 25°C$		60	135	ns
	Major carry transition	To 90% complete, $T_A = 25°C$		20		ns
t_{PLH}, t_{PHL}	Propagation delay	$T_A = 25°C$				
	Each bit			35	60	ns
	All bits switched			35	60	ns
di/dt	Reference input slew rate		4.0	8.0		mA=μS

TEST CIRCUIT

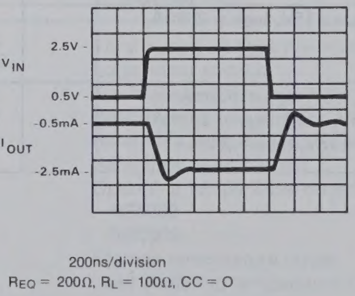

V_{REF}
R_{REF}
V-
V+
.01μ
16
14
3
13
NE5009
4
15
5-12
1 2
R_{15}
CONTROL LOGIC
R_1
NE535
ERROR OUTPUT
REFERENCE DAC ACCURACY > .006%

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



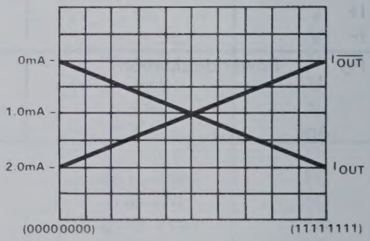
FAST PULSED REFERENCE OPERATION



200ns/division

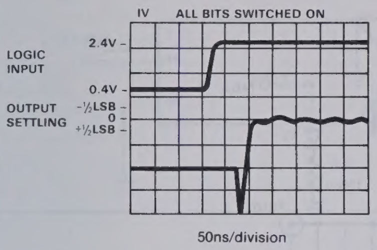
$R_{EQ} = 200\Omega$, $R_L = 100\Omega$, CC = O

TRUE AND COMPLEMENTARY OUTPUT OPERATION



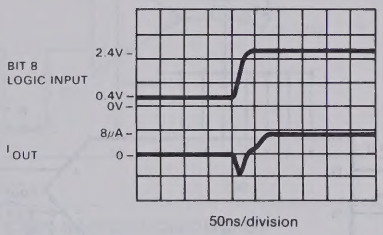
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

FULL SCALE SETTLING TIME

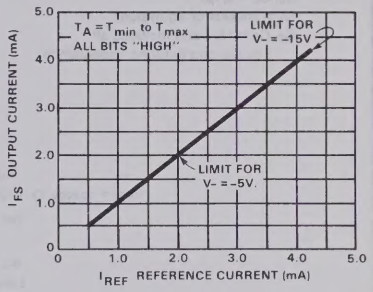


See Figure 13 for settling time fixture

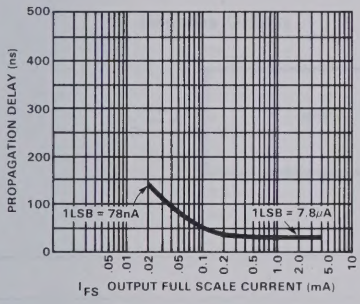
LSB SWITCHING



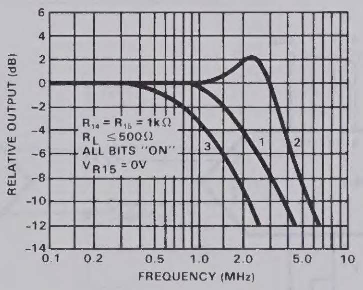
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS

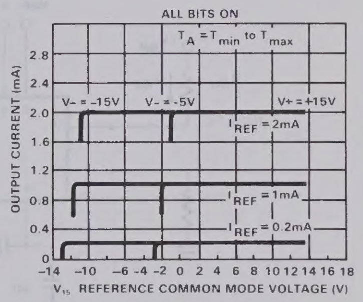


REFERENCE INPUT FREQUENCY RESPONSE



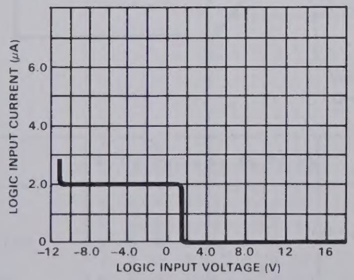
Curve 1:CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.
Curve 2:CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.
Curve 3:CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14}.

REFERENCE AMP COMMON MODE RANGE

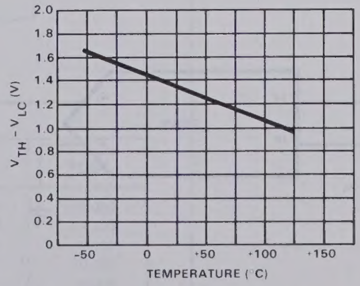


Positive common mode range is always (V+) – 1.5V

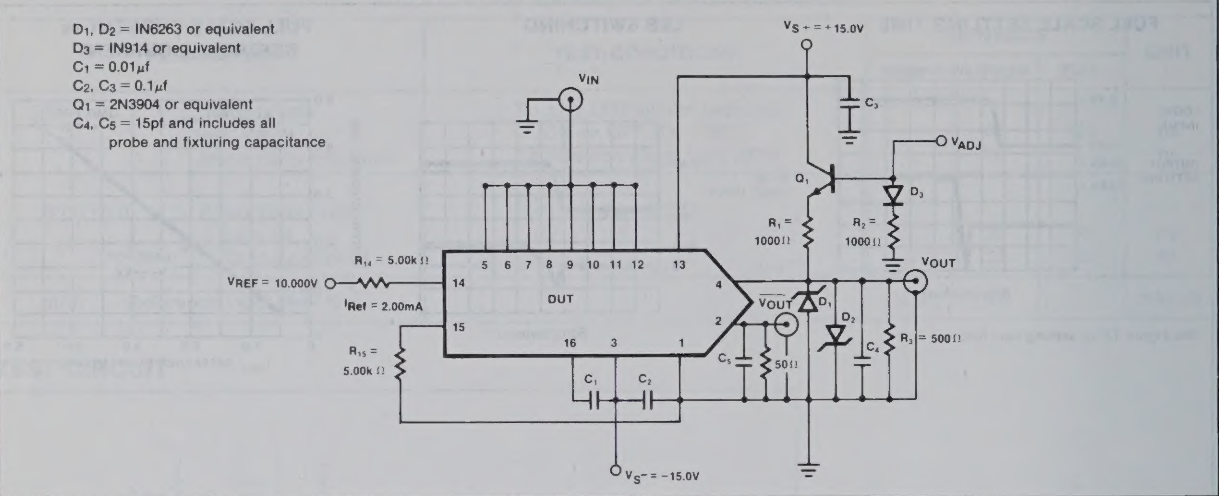
LOGIC INPUT CURRENT vs INPUT VOLTAGE



V_{TH}-V_{LC} vs TEMPERATURE

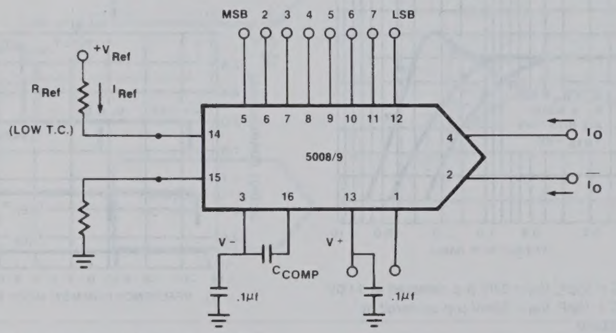


SETTLING TIME AND PROPAGATION DELAY


$V_{S+} = +15.0V$
V_{IN}
C_3
V_{ADJ}
Q_1
D_3
$R_1 = 1000\Omega$
$R_2 = 1000\Omega$
V_{OUT}
$R_{14} = 5.00k\Omega$
$V_{REF} = 10.000V$
$I_{Ref} = 2.00mA$
$R_{15} = 5.00k\Omega$
5 6 7 8 9 10 11 12 13
14
15
DUT
16 3 1
4
2
$\overline{V_{OUT}}$
D_1
D_2
C_4
$R_3 = 500\Omega$
C_5
50Ω
C_1
C_2
$V_{S-} = -15.0V$

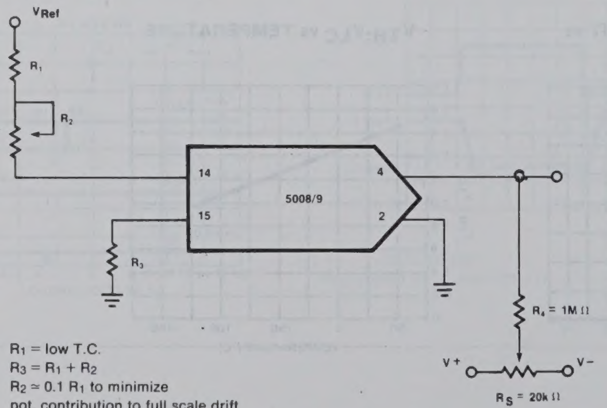
D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01µf
C_2, C_3 = 0.1µf
Q_1 = 2N3904 or equivalent
C_4, C_5 = 15pf and includes all probe and fixturing capacitance

BASIC 5008/5009 CONFIGURATION


MSB 2 3 4 5 6 7 LSB
$+V_{Ref}$
R_{Ref}
I_{Ref}
(LOW T.C.)
5 6 7 8 9 10 11 12
14
15
5008/9
3 16 13 1
4
2
I_O
$\overline{I_O}$
V −
C_{COMP}
V +
.1µf
.1µf

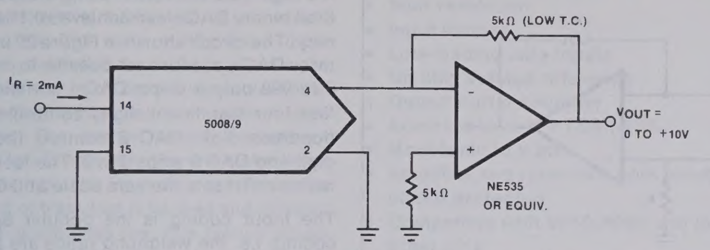
$I_{FS} \approx \frac{+V_{Ref}}{R_{Ref}} \times \frac{255}{256}$; $I_O + \overline{I}_O = I_{FS}$ for all logic states

RECOMMENDED FULL SCALE AND ZERO SCALE ADJ.


V_{Ref}
R_1
R_2
14
15
5008/9
4
2
R_3
$R_4 = 1M\Omega$
V+
V−
$R_S = 20k\Omega$

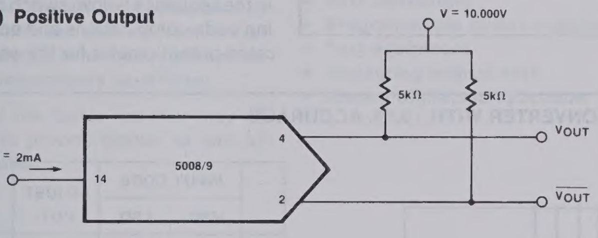
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \simeq 0.1\ R_1$ to minimize pot. contribution to full scale drift

UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT

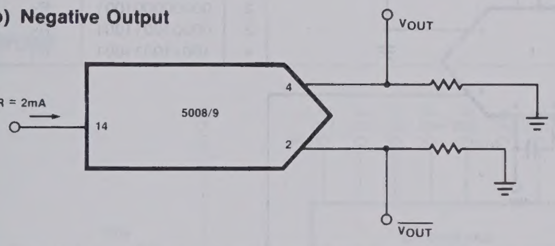

5kΩ (LOW T.C.)
I_R = 2mA
14
15
5008/9
4
2
-
+
V_OUT = 0 TO +10V
5kΩ
NE535 OR EQUIV.

UNIPOLAR VOLT OUTPUT FOR HIGH IMPEDANCE OUTPUT

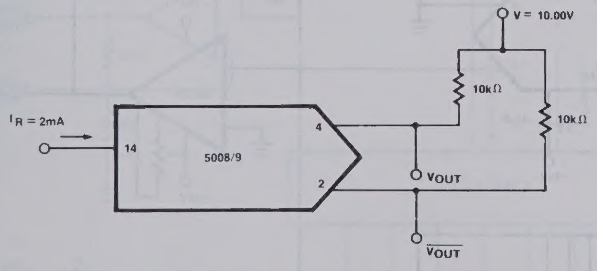
a) Positive Output


V = 10.000V
5kΩ
5kΩ
I_R = 2mA
14
5008/9
4
2
V_OUT
$\overline{V_{OUT}}$

b) Negative Output


V_OUT
I_R = 2mA
14
5008/9
4
2
$\overline{V_{OUT}}$

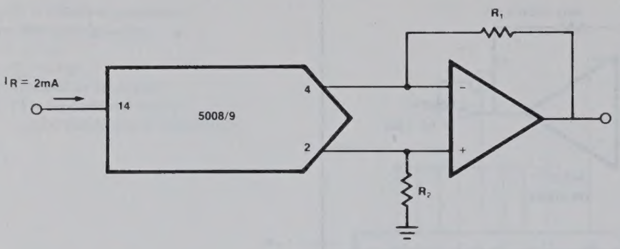
BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)


V = 10.00V
10kΩ
10kΩ
I_R = 2mA
14
5008/9
4
2
V_OUT
$\overline{V_{OUT}}$

CODE CHART

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
POS full scale	1	1	1	1	1	1	1	1	- 9.920V	+10.000
POS f.s. - 1LSB	1	1	1	1	1	1	1	0	- 9.840V	+9.920
+ Zero scale + 1LSB	1	0	0	0	0	0	0	1	- 0.080V	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Neg full scale - 1LSB	0	0	0	0	0	0	0	1	+ 9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

SYMMETRICAL OFFSET BINARY (BIPOLAR)



R1
IR = 2mA
14
5008/9
4
2
R2

VOUT = 0 to ±V*

±V *Range:
±5V for $R_1 = R_2 = 2.5K$
±10V for $R_1 = R_2 = 5.0K$

3 DIGIT BCD CONVERTER

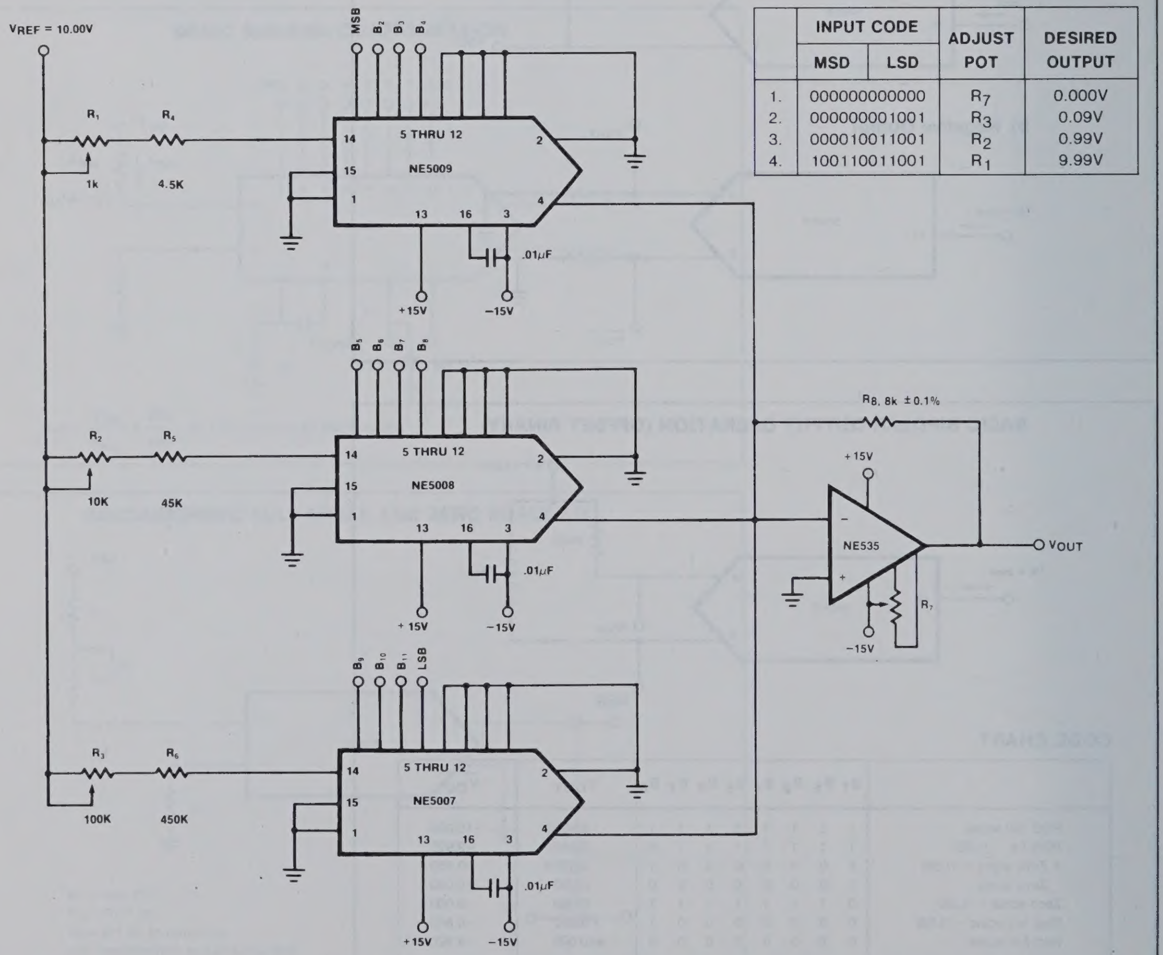
A 3 digit BCD converter, using inexpensive 8-bit binary DACs, can achieve ±0.1% accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9. The feedback resistor (R_7) sets the zero scale at 0.00V.

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are 8, 4, 2 and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.

In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.

3 DIGIT BCD CONVERTER WITH ±0.1% ACCURACY



VREF = 10.00V
MSB
B2
B3
B4
R1
R4
1k
4.5K
14
15
1
5 THRU 12
NE5009
2
4
13
16
3
.01μF
+15V
−15V
B5
B6
B7
B8
R2
R5
10K
45K
NE5008
B9
B10
B11
LSB
R3
R6
100K
450K
NE5007
R8, 8k ±0.1%
+15V
NE535
R7
−15V
VOUT

	INPUT CODE		ADJUST POT	DESIRED OUTPUT
	MSD	LSD		
1.	000000000000		R_7	0.000V
2.	000000001001		R_3	0.09V
3.	000010011001		R_2	0.99V
4.	100110011001		R_1	9.99V

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

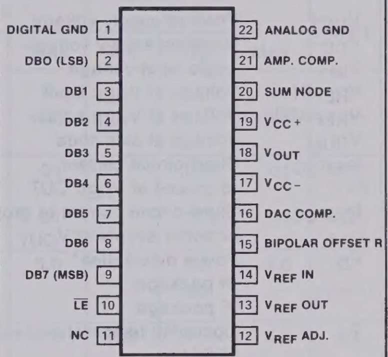
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/2 LSB (.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 2650,8080 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

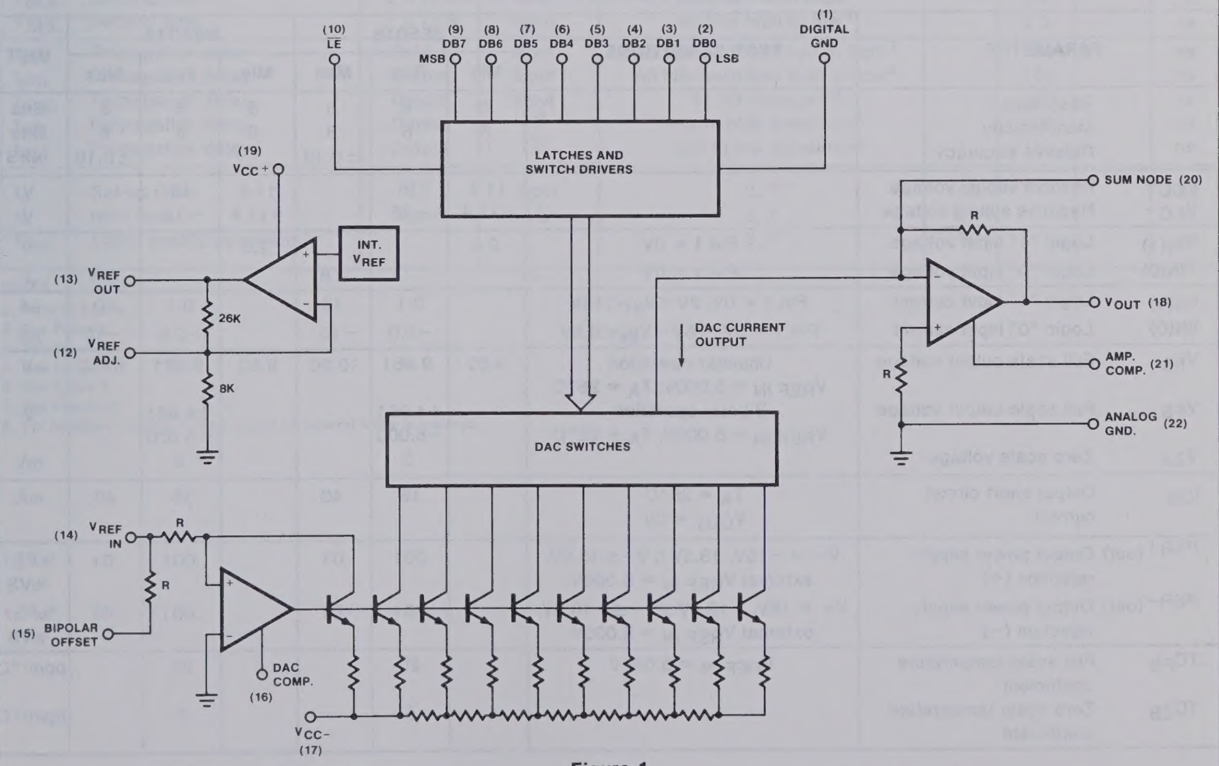
PIN CONFIGURATION

F,N PACKAGE


DIGITAL GND 1
DBO (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
LE 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 VCC+
18 VOUT
17 VCC−
16 DAC COMP.
15 BIPOLAR OFFSET R
14 VREF IN
13 VREF OUT
12 VREF ADJ.

SE5018 available in F package only.

BLOCK DIAGRAM


(10) LE
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(1) DIGITAL GND
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(13) VREF OUT
26K
(12) VREF ADJ.
8K
DAC CURRENT OUTPUT
SUM NODE (20)
R
VOUT (18)
AMP. COMP. (21)
R
ANALOG GND. (22)
DAC SWITCHES
(14) VREF IN
R
R
(15) BIPOLAR OFFSET
DAC COMP. (16)
VCC− (17)

All R values equal 5KΩ and are thermally matched.

Figure 1

SE/NE5018 F,N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation* -N package -F package	 800 1000	 mW mW
T_A	Operating temperature range SE5018 NE5018	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	µA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$		+4.961 −5.000			+4.961 −5.000		V
V_{ZS}	Zero scale voltage			5			5		mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE/5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.5	5.0	5.5	4.5	5.0	5.5	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$ $T_A = 25°C$		60			60		ppm/°C
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$	4.0	5.0	6.0	4.0	5.0	6.0	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

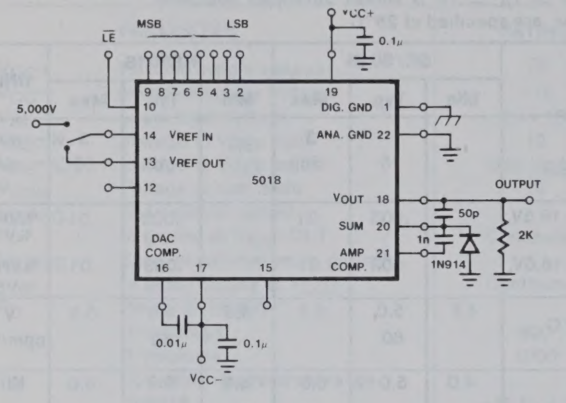
AC ELECTRICAL CHARACTERISTICS[2]

$V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	±½ LSB	Input	All bits low to high[3]		1.8		µs
T_{SHL}	Settling time	±½ LSB	Input	All bits high to low[4]		2.3		µs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

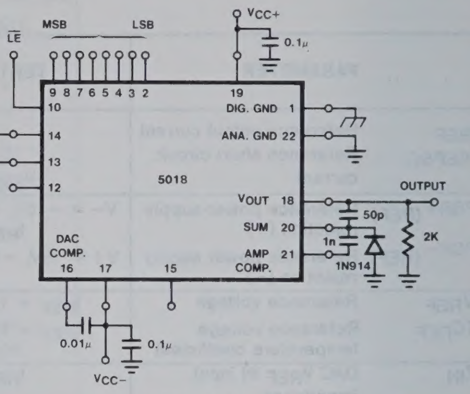
NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.


DC PARAMETRIC TEST CONFIGURATION

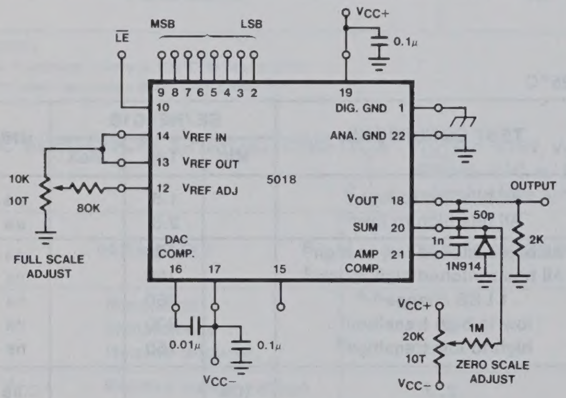
LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
5,000V
10
14 VREF IN
13 VREF OUT
12
19
DIG. GND 1
ANA. GND 22
5018
OUTPUT
VOUT 18
SUM 20
AMP COMP. 21
50p
1n
2K
1N914
DAC COMP.
16
17
15
0.01μ
0.1μ
VCC−

Figure 2


AC PARAMETRIC TEST CONFIGUTATION

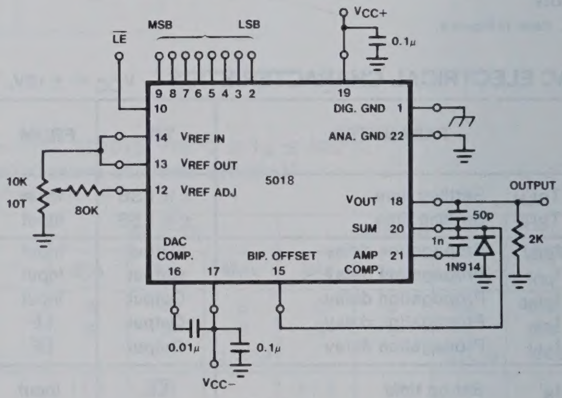
LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
14
13
12
19
DIG. GND 1
ANA. GND 22
5018
OUTPUT
VOUT 18
SUM 20
AMP COMP. 21
50p
1n
2K
1N914
DAC COMP.
16
17
15
0.01μ
0.1μ
VCC−

Figure 3


FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

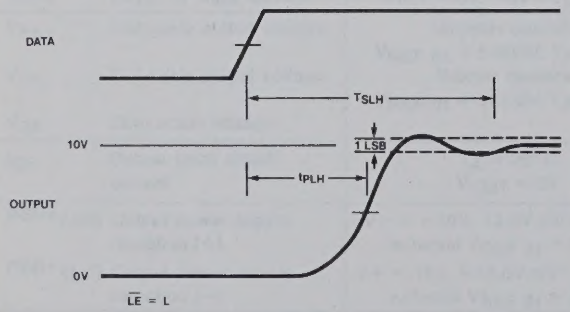
LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
14 VREF IN
13 VREF OUT
12 VREF ADJ
19
DIG. GND 1
ANA. GND 22
5018
10K
10T
80K
FULL SCALE ADJUST
OUTPUT
VOUT 18
SUM 20
AMP COMP. 21
50p
1n
2K
1N914
DAC COMP.
16
17
15
0.01μ
0.1μ
VCC−
VCC+
20K
10T
1M
VCC−
ZERO SCALE ADJUST

Figure 4


BIPOLAR OUTPUT OPERATION (−5 to +5V)

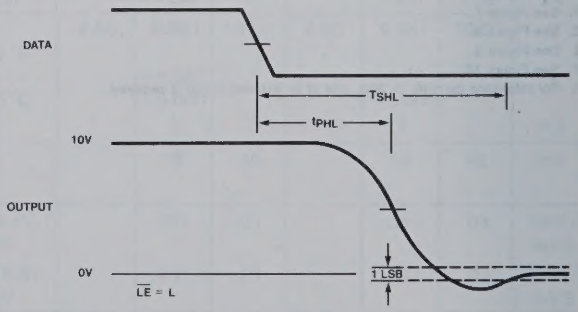
LE
MSB
LSB
VCC+
0.1μ
9 8 7 6 5 4 3 2
10
14 VREF IN
13 VREF OUT
12 VREF ADJ
19
DIG. GND 1
ANA. GND 22
5018
10K
10T
80K
OUTPUT
VOUT 18
SUM 20
AMP COMP. 21
50p
1n
2K
1N914
DAC COMP.
16
17
BIP. OFFSET 15
0.01μ
0.1μ
VCC−

Figure 5


SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

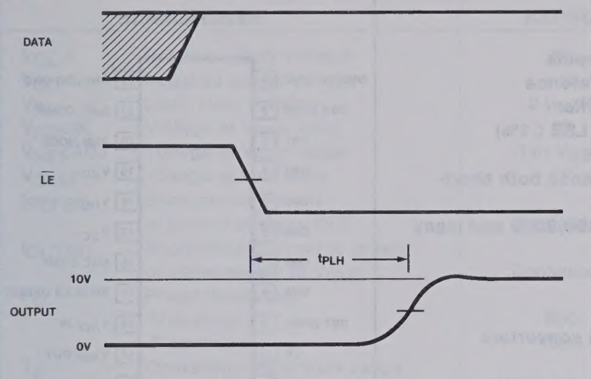
DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
LE = L

Figure 6


SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
LE = L

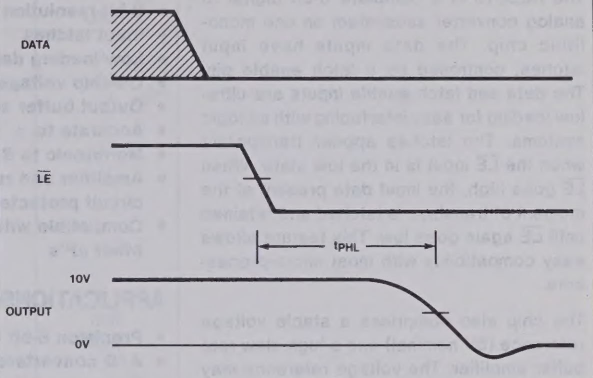
Figure 7



PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

DATA
LE
t_{PLH}
10V
OUTPUT
0V

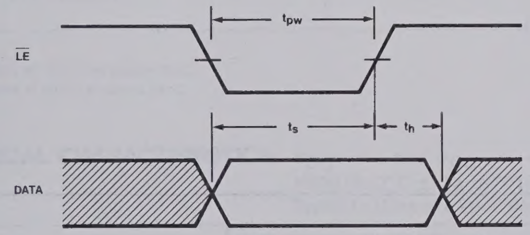
Figure 8



PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

DATA
LE
t_{PHL}
10V
OUTPUT
0V

Figure 9



LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

t_{PW}
LE
t_s
t_h
DATA

Figure 10

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

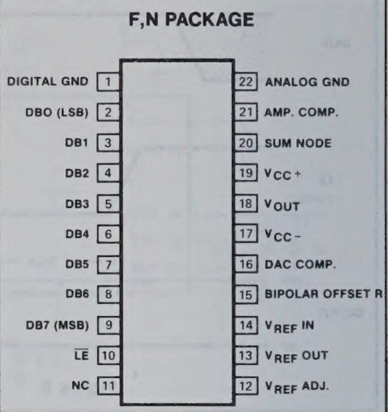
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 2650,8080 and many other µP's**

APPLICATIONS

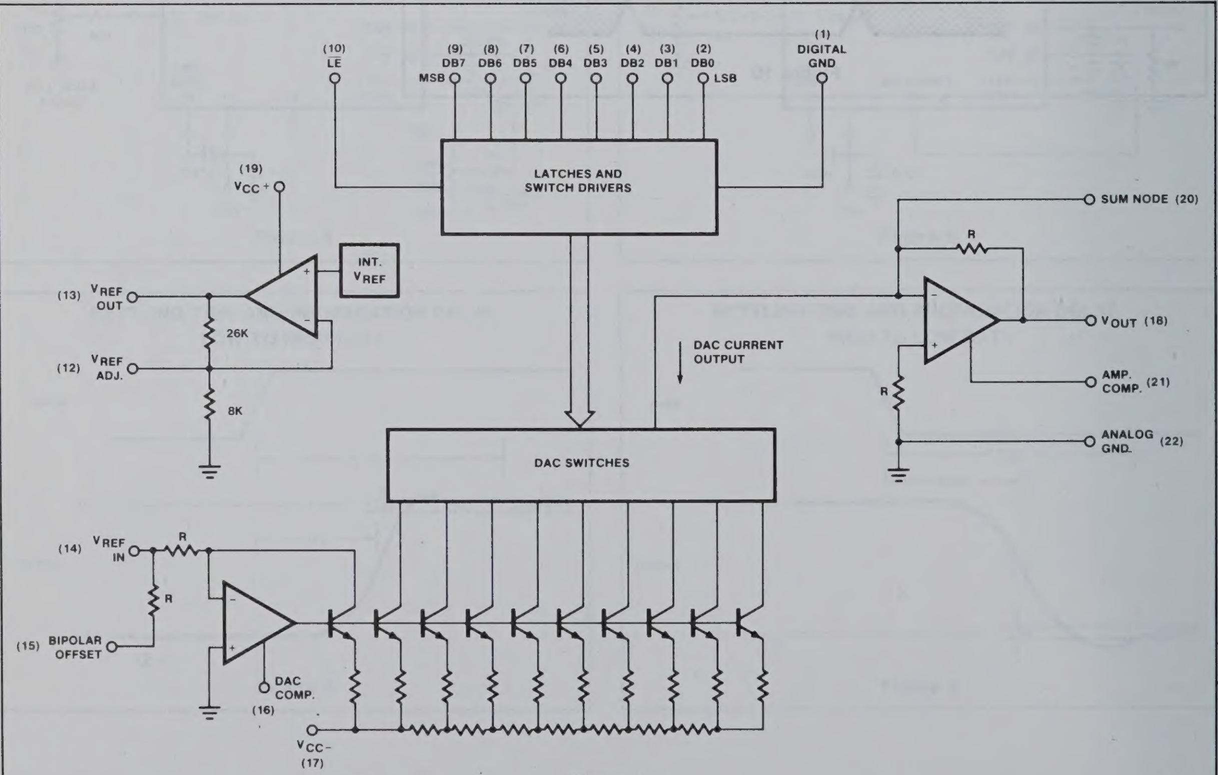
- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION


F,N PACKAGE
DIGITAL GND 1
DBO (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{LE}$ 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 $V_{CC}+$
18 V_{OUT}
17 $V_{CC}-$
16 DAC COMP.
15 BIPOLAR OFFSET R
14 V_{REF} IN
13 V_{REF} OUT
12 V_{REF} ADJ.

SE5019 available in F package only.

BLOCK DIAGRAM


(10) $\overline{LE}$
(9) DB7 MSB
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0 LSB
(1) DIGITAL GND
LATCHES AND SWITCH DRIVERS
(19) $V_{CC}+$
INT. V_{REF}
(13) V_{REF} OUT
26K
(12) V_{REF} ADJ.
8K
DAC CURRENT OUTPUT
SUM NODE (20)
R
V_{OUT} (18)
AMP. COMP. (21)
R
ANALOG GND. (22)
DAC SWITCHES
(14) V_{REF} IN
R
R
(15) BIPOLAR OFFSET
DAC COMP. (16)
$V_{CC}-$ (17)

All R values equal 5KΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
V_{REF}^{IN}	Voltage at V_{REF} input	12	V
V_{REF}^{ADJ}	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5019	−55 to +125	°C
	NE5019	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$		+4.961 −5.000			+4.961 −5.000		V
V_{ZS}	Zero scale voltage			5			5		mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

NOTE
1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.5	5.0	5.5	4.5	5.0	5.5	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $V_{REF}IN$ input impedance	$I_{REF} = 1.0mA$	4.0	5.0	6.0	4.0	5.0	6.0	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{\text{LE}}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{\text{LE}}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{\text{LE}}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{\text{LE}}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

DC PARAMETRIC TEST CONFIGURATION

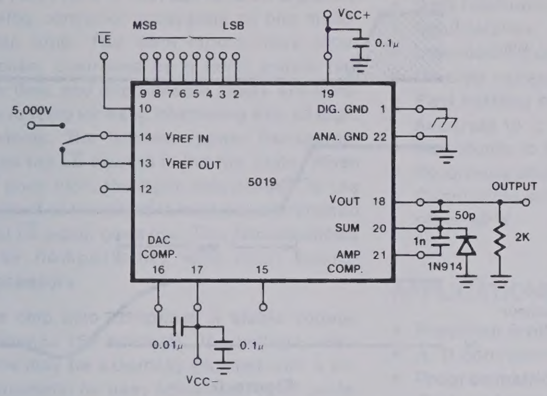

MSB
LSB
LE
VCC+
0.1μ
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
5,000V
14 VREF IN
ANA. GND 22
13 VREF OUT
5019
12
OUTPUT
VOUT 18
50p
SUM 20
1n
2K
DAC COMP.
AMP COMP. 21
1N914
16 17 15
0.01μ
0.1μ
VCC−

Figure 2

AC PARAMETRIC TEST CONFIGUTATION

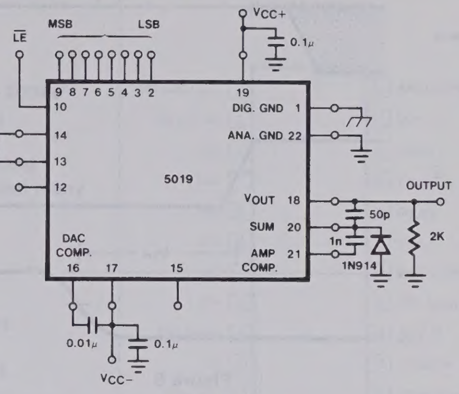

MSB
LSB
LE
VCC+
0.1μ
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
14
ANA. GND 22
13
5019
12
OUTPUT
VOUT 18
50p
SUM 20
1n
2K
DAC COMP.
AMP COMP. 21
1N914
16 17 15
0.01μ
0.1μ
VCC−

Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

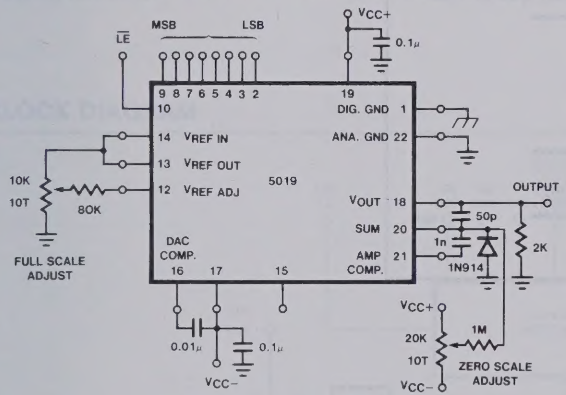

MSB
LSB
LE
VCC+
0.1μ
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
12 VREF ADJ
80K
5019
FULL SCALE ADJUST
OUTPUT
VOUT 18
50p
SUM 20
1n
2K
DAC COMP.
AMP COMP. 21
1N914
16 17 15
0.01μ
0.1μ
VCC−
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−

Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

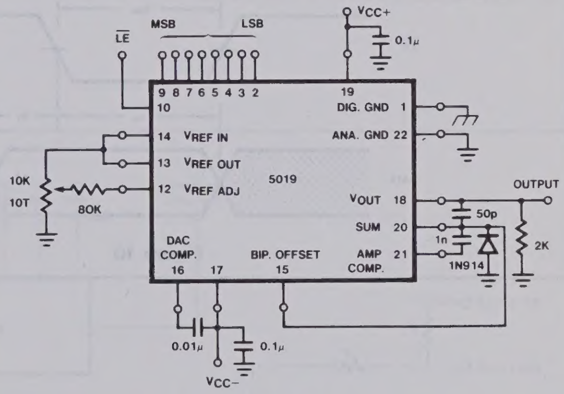

MSB
LSB
LE
VCC+
0.1μ
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
12 VREF ADJ
80K
5019
OUTPUT
VOUT 18
50p
SUM 20
1n
2K
DAC COMP.
BIP. OFFSET 15
AMP COMP. 21
1N914
16 17
0.01μ
0.1μ
VCC−

Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

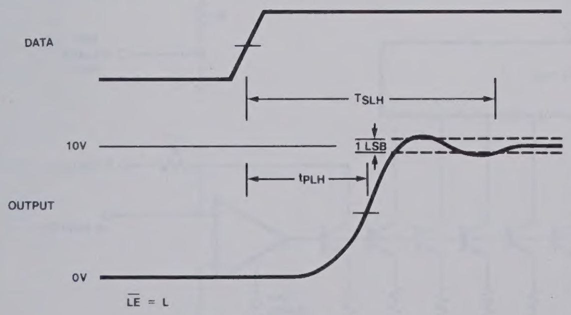

DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
LE = L

Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

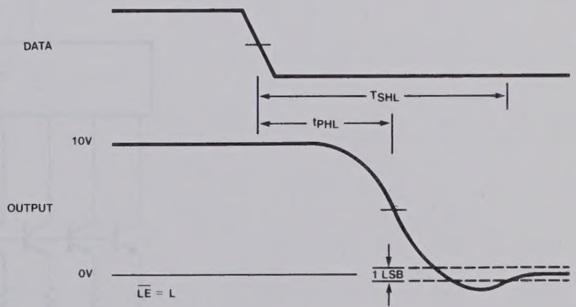

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
LE = L

Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

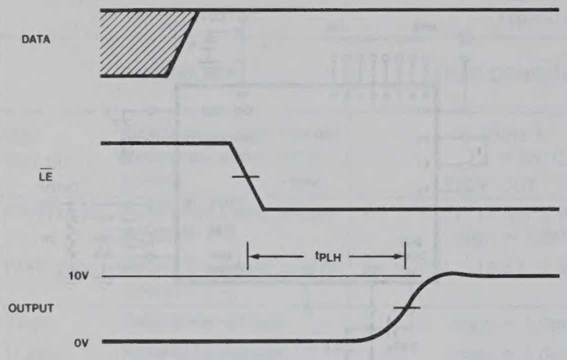

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V

Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

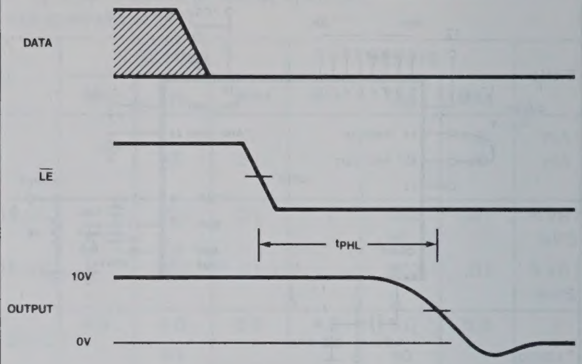

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V

Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

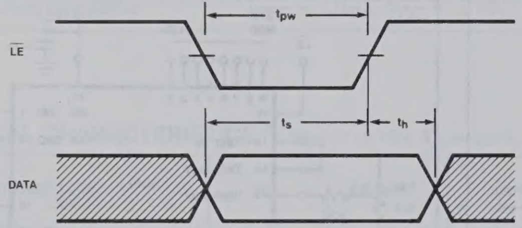

t_{pw}
$\overline{LE}$
t_s
t_h
DATA

Figure 10

8-BIT µP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT SE/NE5118

SE5118-F • NE5118-N

DESCRIPTION

The NE5118 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{\text{LE}}$ input is in the low state. When $\overline{\text{LE}}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{\text{LE}}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

FEATURES

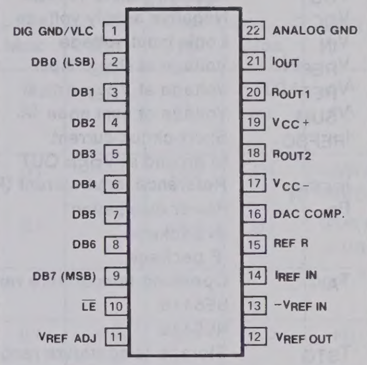
- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Fast settling output current—200ns
- Accurate to ± 1/2 LSB (.19%)
- Monotonic to 8 bits
- Reference short-circuit protected
- Compatible with 2650, 8080 and many other µP's

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication
- CRT display drivers
- High-speed modems

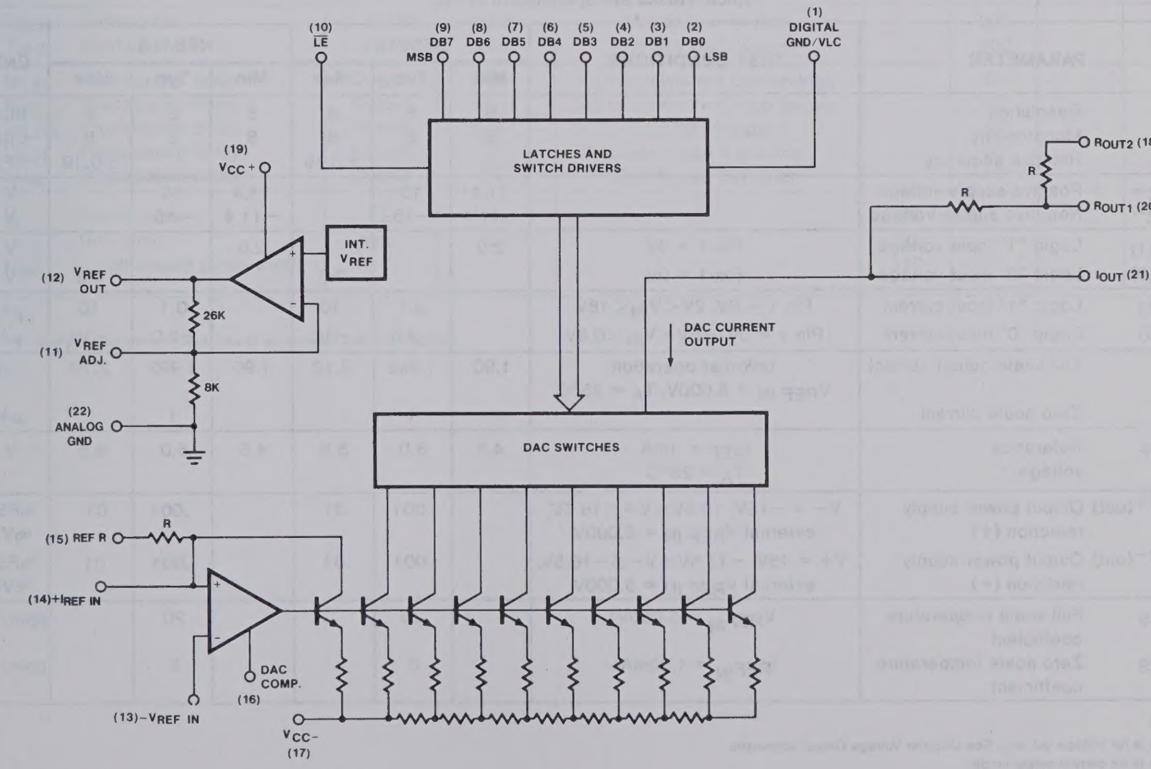
PIN CONFIGURATION

F,N PACKAGE


DIG GND/VLC 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{\text{LE}}$ 10
VREF ADJ 11
22 ANALOG GND
21 IOUT
20 ROUT1
19 VCC+
18 ROUT2
17 VCC−
16 DAC COMP.
15 REF R
14 IREF IN
13 −VREF IN
12 VREF OUT

SE5118 available in F package only.

BLOCK DIAGRAM


(10) $\overline{\text{LE}}$
(9) DB7 MSB
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0 LSB
(1) DIGITAL GND/VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
26K
(11) VREF ADJ.
8K
(22) ANALOG GND
ROUT2 (18)
R
R
ROUT1 (20)
IOUT (21)
DAC CURRENT OUTPUT
DAC SWITCHES
(15) REF R
R
(14)+IREF IN
DAC COMP. (16)
(13)−VREF IN
VCC− (17)

All R values equal 5kΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at R_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{REFIN}	Reference input current (Pin 14)	3	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5118	−55 to +125	°C
	NE5118	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \leq T_A \leq 125°C$, NE5118. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current			1			1		μA
V_{REF}	Reference voltage	$I_{REF} = 1mA$ $T_A = 25°C$	4.5	5.0	5.5	4.5	5.0	5.5	V
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF_{IN}} = 5.000V$[1]		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient	$I_{REF_{IN}} = 1.00mA$[2]		5			5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic.
2. This is for current output mode.

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \leq T_A \leq 125°C$,
NE5118. $0°C \leq T_A \leq 70°C$ unless otherwise specified.
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 1			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF}IN$ input impedance		4.0	5.0	6.0	4.0	5.0	6.0	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS

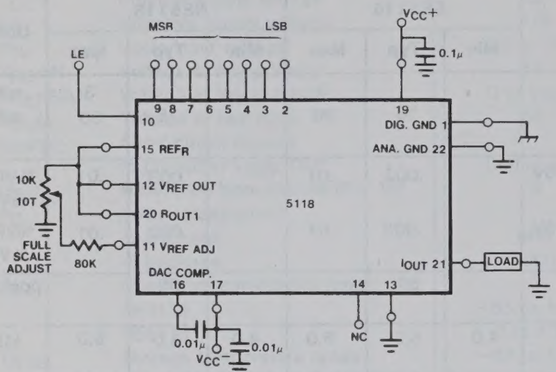
$V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5118			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s	Set-up time	$\overline{LE}$	Input		100			ns
t_h	Hold time	Input	$\overline{LE}$		50			ns
t_{pw}	Latch enable pulse width				150			ns

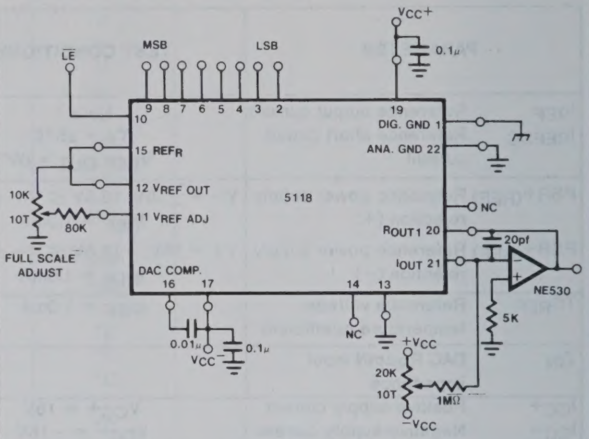
NOTES

1. For reference currents > 3mA, use of an external buffer is required.

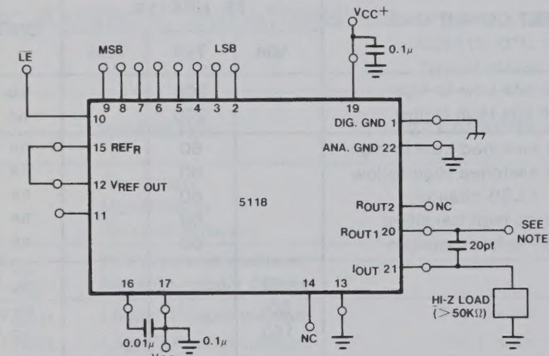
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)


MSB
LSB
LE
Vcc+
0.1μ
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
20 ROUT1
11 VREF ADJ
5118
10K
10T
FULL SCALE ADJUST
80K
DAC COMP.
16 17
14 13
IOUT 21
LOAD
NC
0.01μ
0.01μ
VCC−

UNIPOLAR VOLTAGE OUTPUT (0 →+10V)


Vcc+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118
10K
10T
80K
FULL SCALE ADJUST
NC
ROUT1 20
20pf
IOUT 21
NE530
DAC COMP.
16 17
14 13
NC
5K
0.01μ
0.1μ
VCC−
+VCC
20K
10T
1MΩ
−VCC

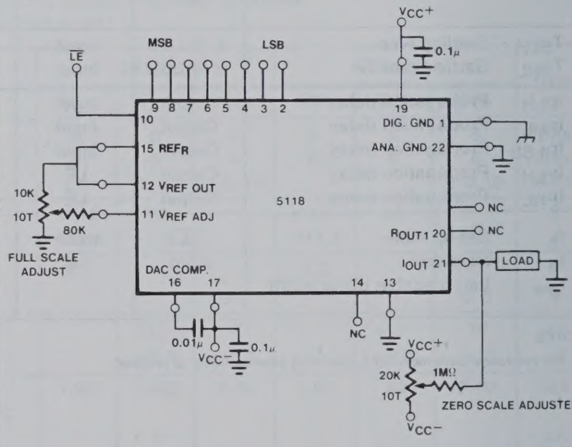
FAST VOLTAGE OUTPUT


VCC+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11
5118
ROUT2
NC
ROUT1 20
SEE NOTE
20pf
IOUT 21
HI-Z LOAD (>50KΩ)
16 17
14 13
NC
0.01μ
0.1μ
VCC−

NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 →−2mA)


VCC+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118
10K
10T
80K
FULL SCALE ADJUST
NC
NC
ROUT1 20
IOUT 21
LOAD
DAC COMP.
16 17
14 13
NC
0.01μ
0.1μ
VCC−
VCC+
20K
10T
1MΩ
ZERO SCALE ADJUSTER
VCC−

SE5119-F • NE5119-N

DESCRIPTION

The NE5119 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

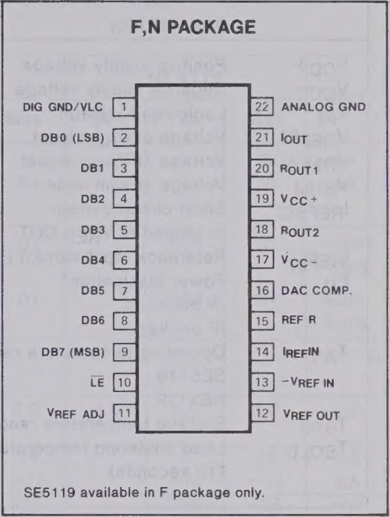
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ±1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 2650, 8080 and many other µP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION


F,N PACKAGE
DIG GND/VLC 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
LE 10
VREF ADJ 11
22 ANALOG GND
21 IOUT
20 ROUT1
19 VCC+
18 ROUT2
17 VCC−
16 DAC COMP.
15 REF R
14 IREFIN
13 −VREF IN
12 VREF OUT
SE5119 available in F package only.

BLOCK DIAGRAM

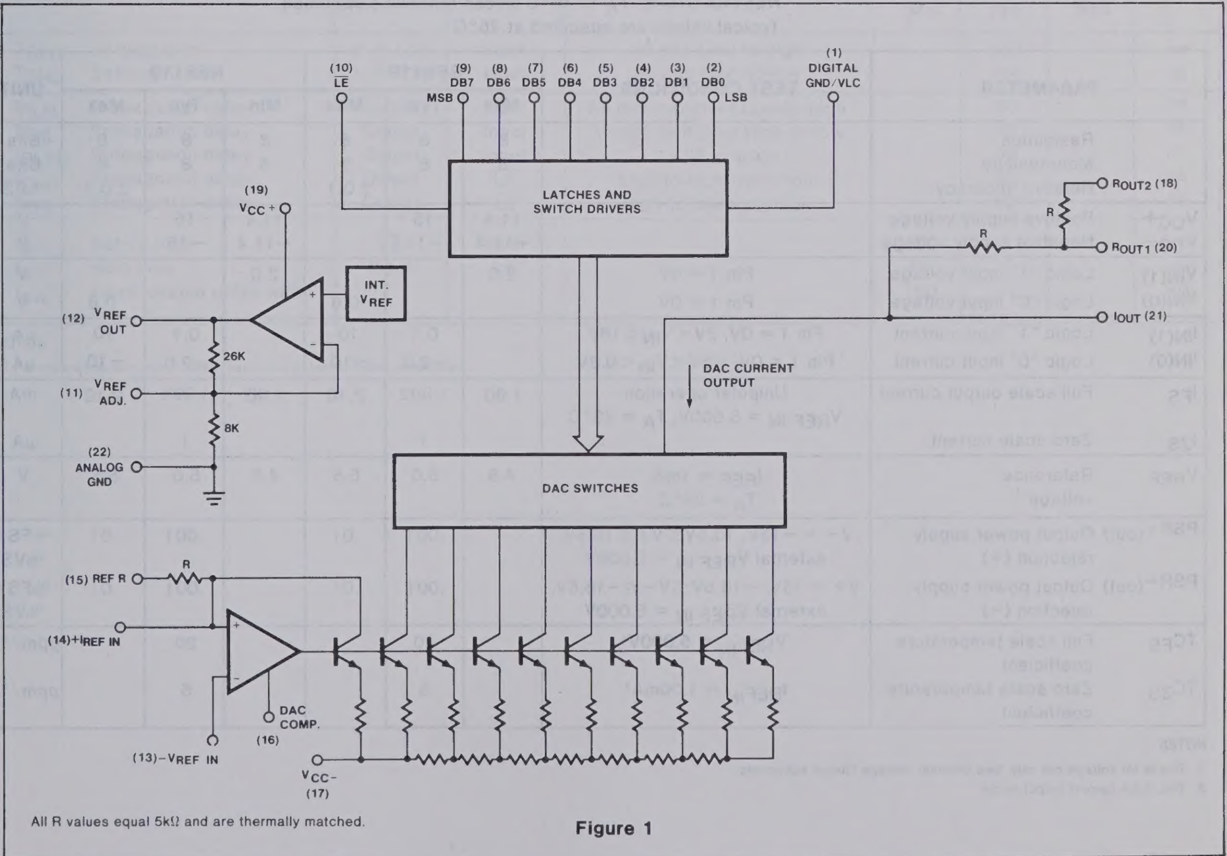

(10) LE
(9) DB7 MSB
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0 LSB
(1) DIGITAL GND/VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
26K
(11) VREF ADJ.
8K
(22) ANALOG GND
ROUT2 (18)
R
R
ROUT1 (20)
IOUT (21)
DAC CURRENT OUTPUT
DAC SWITCHES
(15) REF R
R
(14)+IREF IN
DAC COMP. (16)
(13)−VREF IN
VCC− (17)
All R values equal 5kΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at R_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{REFIN}	Reference input current (Pin 14)	3	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5119	−55 to +125	°C
	NE5119	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V<V_{IN}<18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V<V_{IN}<0.8V$		−2.0	−10		−2.0	−10	μA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current			1			1		μA
V_{REF}	Reference voltage	$I_{REF} = 1mA$ $T_A = 25°C$	4.5	5.0	5.5	4.5	5.0	5.5	V
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REFIN} = 5.000V^1$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient	$I_{REFIN} = 1.00mA^2$		5			5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic
2. This is for current output mode

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT
		Min	Typ	Max	Min	Typ	Max	
I_{REF} Reference output current	Note 1			3			3	mA
I_{REFSC} Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$ Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$ Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
TC_{REF} Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN} DAC $R_{REF}IN$ input impedance		4.0	5.0	6.0	4.0	5.0	6.0	kΩ
$I_{CC}+$ Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$ Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

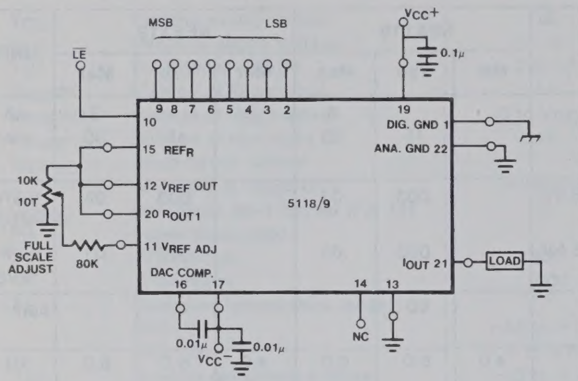
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5119			UNIT
				Min	Typ	Max	
T_{SLH} Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL} Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH} Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL} Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB} Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH} Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL} Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s Set-up time	$\overline{LE}$	Input		100			ns
t_h Hold time	Input	$\overline{LE}$		50			ns
t_{pw} Latch enable pulse width				150			ns

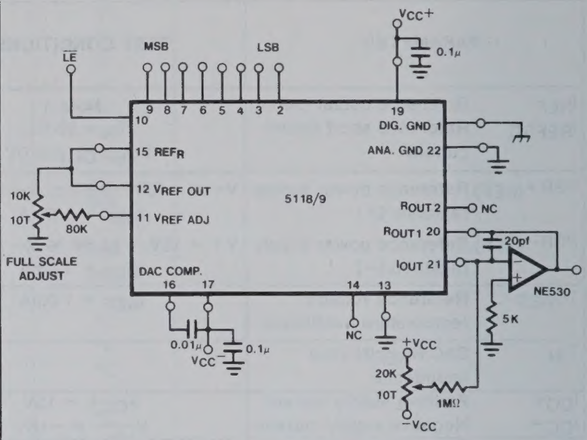
NOTES

1. For reference currents > 3mA, use of an external buffer is required.

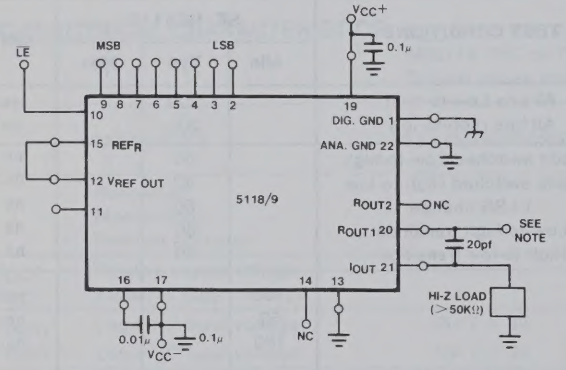
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)


MSB
LSB
LE
VCC+
0.1μ
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
20 ROUT1
11 VREF ADJ
5118/9
10K
10T
FULL SCALE ADJUST
80K
DAC COMP.
16 17
14 13
IOUT 21
LOAD
0.01μ
0.01μ
VCC−
NC

UNIPOLAR VOLTAGE OUTPUT (0 → +10V)


VCC+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118/9
ROUT2
NC
ROUT1 20
20pf
IOUT 21
NE530
5K
10K
10T
80K
FULL SCALE ADJUST
DAC COMP.
16 17
14 13
NC
0.01μ
VCC−
0.1μ
+VCC
20K
10T
1MΩ
VCC

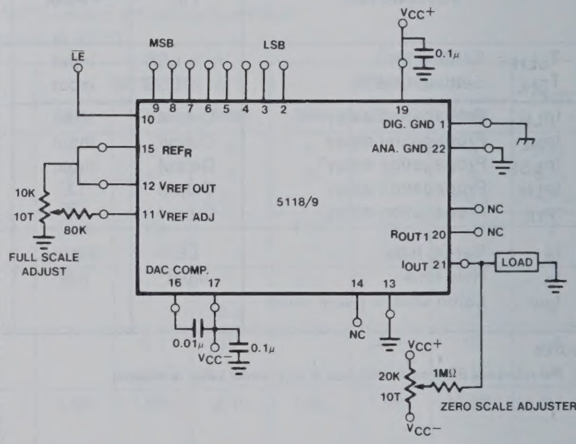
FAST VOLTAGE OUTPUT


VCC+
0.1μ
LE
MSB
LSB
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11
5118/9
ROUT2
NC
ROUT1 20
SEE NOTE
20pf
IOUT 21
HI-Z LOAD (>50KΩ)
16 17
14 13
NC
0.01μ
0.1μ
VCC−

NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 → −2mA)


VCC+
0.1μ
MSB
LSB
LE
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118/9
NC
ROUT1 20
NC
IOUT 21
LOAD
10K
10T
80K
FULL SCALE ADJUST
DAC COMP.
16 17
14 13
NC
0.01μ
VCC−
0.1μ
VCC+
20K
10T
1MΩ
ZERO SCALE ADJUSTER
VCC−

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

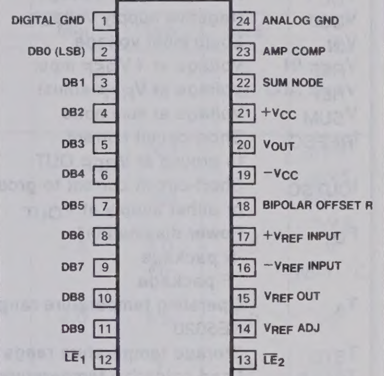
- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and Bipolar (±5V) output range**
- **Logic bus compatible**
- **5μsec settling time**

APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit Analog to Digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

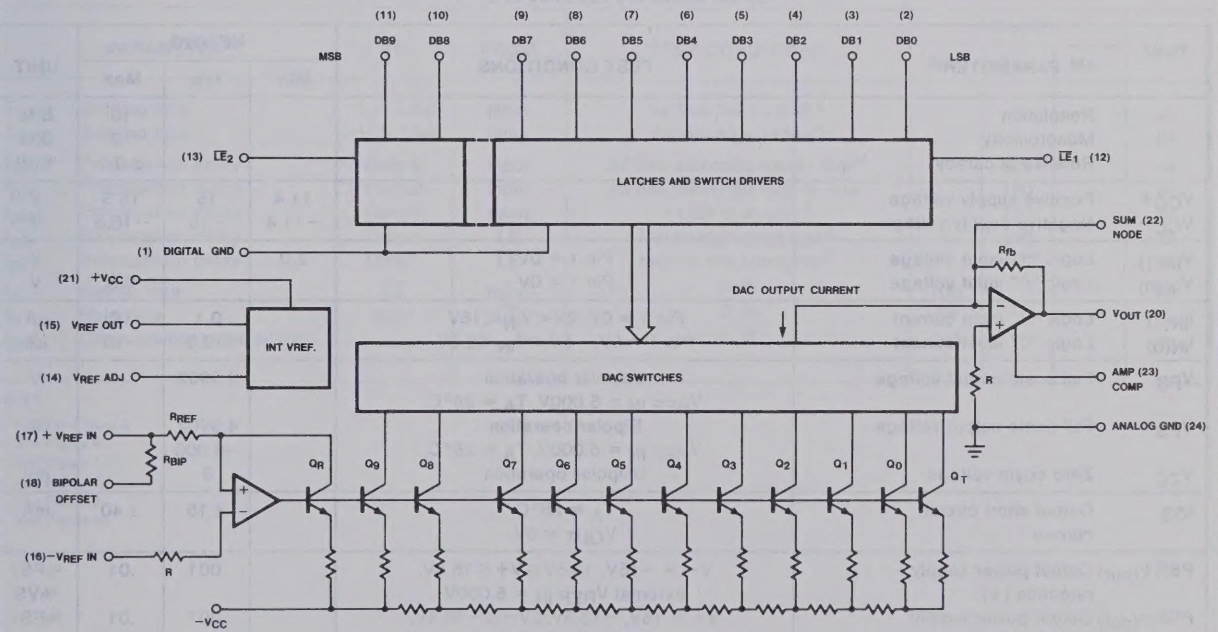
PIN CONFIGURATION

F, N PACKAGE


DIGITAL GND 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 9
DB8 10
DB9 11
$\overline{LE}_1$ 12
24 ANALOG GND
23 AMP COMP
22 SUM NODE
21 $+V_{CC}$
20 V_{OUT}
19 $-V_{CC}$
18 BIPOLAR OFFSET R
17 $+V_{REF}$ INPUT
16 $-V_{REF}$ INPUT
15 V_{REF} OUT
14 V_{REF} ADJ
13 $\overline{LE}_2$

ORDER PART NO.
NE5020F
NE5020N

BLOCK DIAGRAM


(11) DB9
(10) DB8
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(13) $\overline{LE}_2$
$\overline{LE}_1$ (12)
LATCHES AND SWITCH DRIVERS
(1) DIGITAL GND
(21) $+V_{CC}$
(15) V_{REF} OUT
(14) V_{REF} ADJ
INT VREF.
DAC OUTPUT CURRENT
DAC SWITCHES
SUM (22) NODE
R_{fb}
V_{OUT} (20)
AMP (23) COMP
R
ANALOG GND (24)
(17) $+V_{REF}$ IN
R_{REF}
R_{BIP}
(18) BIPOLAR OFFSET
(16) $-V_{REF}$ IN
R
Q_R
Q_9
Q_8
Q_7
Q_6
Q_5
Q_4
Q_3
Q_2
Q_1
Q_0
Q_T
$-V_{CC}$ (19)

ALL R VALUES EQUAL 5kΩ AND ARE THERMALLY MATCHED

Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
V_{REF} IN	Voltage at $+V_{REF}$ input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	F package	1000	mW
T_A	Operating temperature range		
	NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
	Resolution				10	Bits
	Monotonicity				10	Bits
	Relative accuracy				±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$		9.9902		V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$		4.9902 −5.000		V
V_{ZS}	Zero scale voltage	Unipolar operation		5		mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		±15	±40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20		ppmFS/°C
TC_{ZS}	Zero scale temperature coefficient			5		ppmFS/°C

NOTE
1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.5	5.0	5.5	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60		ppm/°C
Z_{IN}	DAC V_{REF}IN input impedance	$I_{REF} = 1.0mA$	4.0	5.0	6.0	kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435	mW

NOTE

1. Refer to Figure 2.
2. For I_{REF} OUT greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[3] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	NE5020			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[4]		5		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[5]		5		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[4]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[5]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[4,5]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[6]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[7]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	3, 8	100			ns
t_h	Hold time	Input	$\overline{LE}$	3, 8	50			ns
t_{pw}	Latch enable pulse width			3, 8	150			ns

NOTES

3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.

DC PARAMETRIC TEST CONFIGURATION

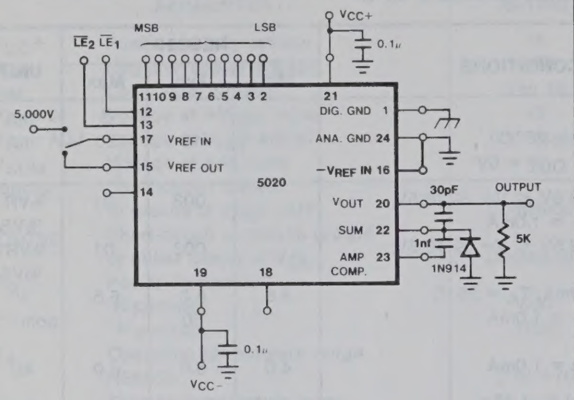

MSB
LSB
VCC+
0.1μ
LE2 LE1
11 10 9 8 7 6 5 4 3 2
21
DIG. GND 1
12
13
5,000V
17 VREF IN
ANA. GND 24
15 VREF OUT
−VREF IN 16
14
5020
30pF
OUTPUT
VOUT 20
SUM 22
1nf
5K
AMP COMP. 23
1N914
19
18
0.1μ
VCC−

Figure 2

AC PARAMETRIC TEST CONFIGURATION

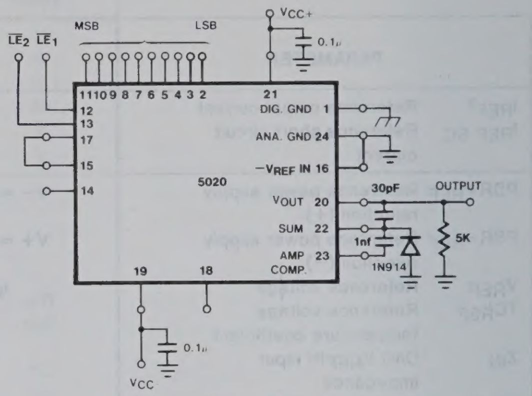

MSB
LSB
VCC+
0.1μ
LE2 LE1
11 10 9 8 7 6 5 4 3 2
21
DIG. GND 1
12
13
17
ANA. GND 24
15
−VREF IN 16
14
5020
30pF
OUTPUT
VOUT 20
SUM 22
1nf
5K
AMP COMP. 23
1N914
19
18
0.1μ
VCC

Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0–10V)

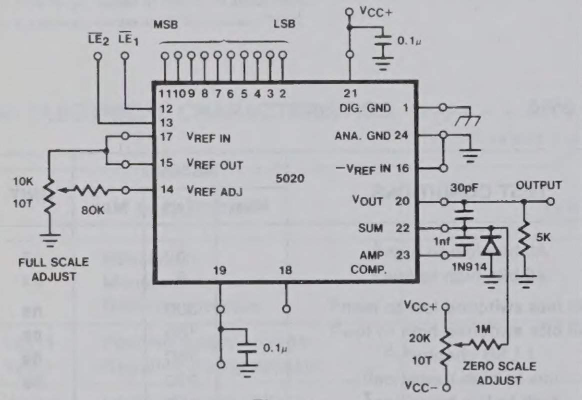

MSB
LSB
VCC+
0.1μ
LE2 LE1
11 10 9 8 7 6 5 4 3 2
21
DIG. GND 1
12
13
17 VREF IN
ANA. GND 24
15 VREF OUT
−VREF IN 16
10K
10T
14 VREF ADJ
80K
5020
30pF
OUTPUT
VOUT 20
SUM 22
1nf
5K
AMP COMP. 23
1N914
FULL SCALE ADJUST
19
18
0.1μ
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−

Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

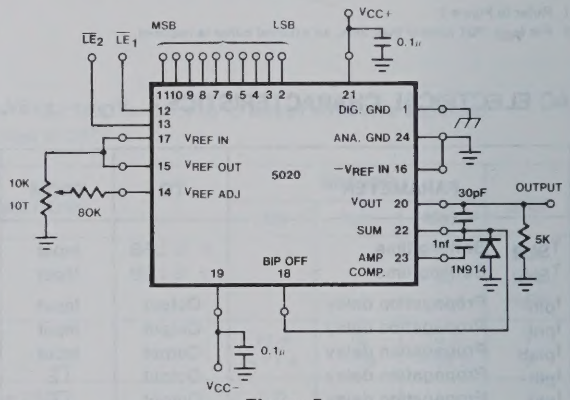

MSB
LSB
VCC+
0.1μ
LE2 LE1
11 10 9 8 7 6 5 4 3 2
21
DIG. GND 1
12
13
17 VREF IN
ANA. GND 24
15 VREF OUT
−VREF IN 16
10K
10T
14 VREF ADJ
80K
5020
30pF
OUTPUT
VOUT 20
SUM 22
1nf
5K
BIP OFF 18
AMP COMP. 23
1N914
19
0.1μ
VCC−

Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

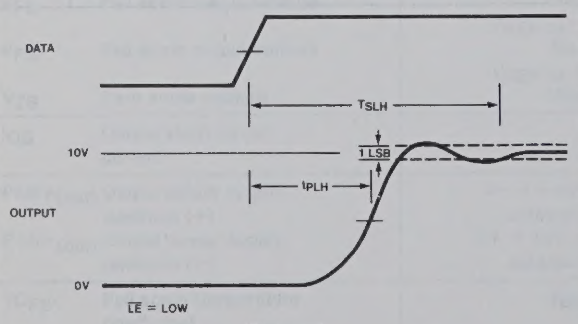

DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
LE = LOW

Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

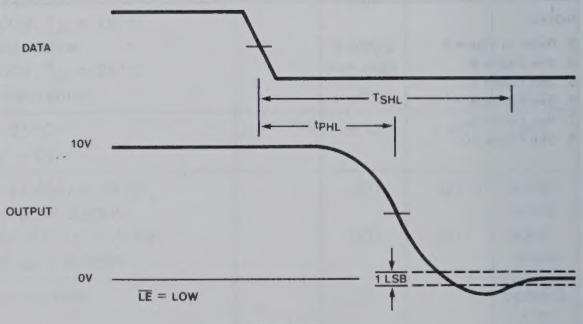

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
LE = LOW

Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

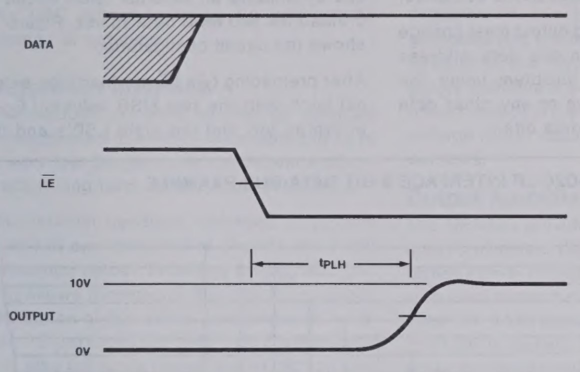

DATA
LE
t_{PLH}
10V
OUTPUT
0V

Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

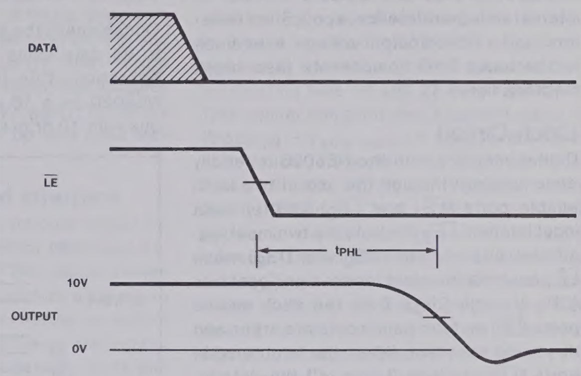

DATA
LE
t_{PHL}
10V
OUTPUT
0V

Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

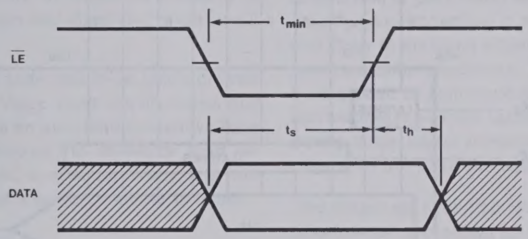

t_{min}
LE
t_s
t_h
DATA

Figure 10

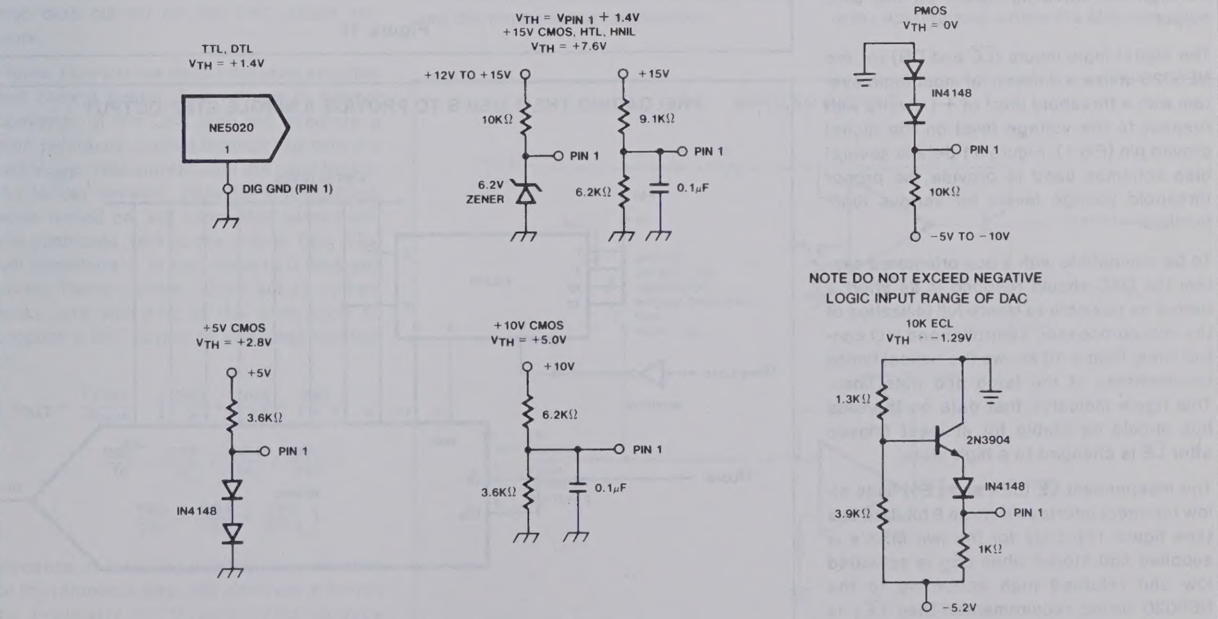

TTL, DTL
VTH = +1.4V
NE5020
1
DIG GND (PIN 1)
VTH = VPIN 1 + 1.4V
+15V CMOS, HTL, HNIL
VTH = +7.6V
+12V TO +15V
10KΩ
PIN 1
6.2V ZENER
+15V
9.1KΩ
PIN 1
6.2KΩ
0.1μF
PMOS
VTH = 0V
IN4148
PIN 1
10KΩ
−5V TO −10V
NOTE DO NOT EXCEED NEGATIVE LOGIC INPUT RANGE OF DAC
+5V CMOS
VTH = +2.8V
+5V
3.6KΩ
PIN 1
IN4148
+10V CMOS
VTH = +5.0V
+10V
6.2KΩ
PIN 1
3.6KΩ
0.1μF
10K ECL
VTH −1.29V
1.3KΩ
2N3904
IN4148
PIN 1
3.9KΩ
1KΩ
−5.2V

Figure 11

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage, in addition to the basic DAC components (see block diagram, figure 1).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_ϕ). Both the latch enable ports ($\overline{LE}$) and the data inputs are static and threshold sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low (Logic '0') the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which $\overline{LE}$ goes high) 'memorize' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (.8V max) or $0.1\mu A$ for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 11 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus orientated system the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 10 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50nsec after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8 bit data bus (see figure 12). Data for the two MSB's is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSB's of data are transferred into the DAC. With $\overline{LE}_1$ returning high the loading of ten bit data word from an eight bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16 bit bus or any other data bus with 10 or greater data bits. This can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 13 shows the circuit configuration.

After preloading (via $\overline{LE}$ pre-load) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSB's and the

NE5020 μP INTERFACE 8-BIT DATA BUS EXAMPLE

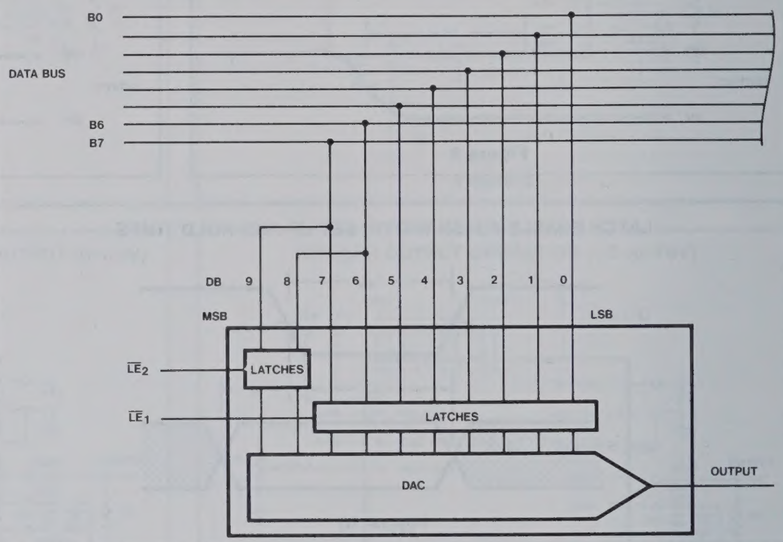


Figure 12

PRELOADING THE 2 MSB'S TO PROVIDE A SINGLE STEP OUTPUT

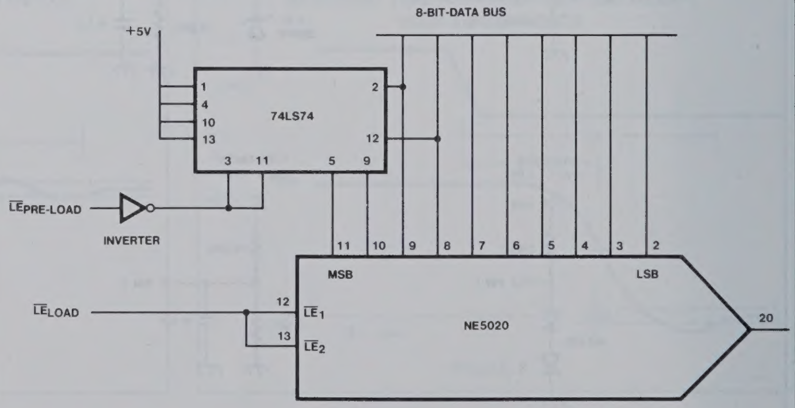


Figure 13

two MSB's are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a V_{REF}ADJ (pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in figure 16 performs not only V_{REF} adjustment but also full scale output adjust. Notice that the V_{REF}ADJ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the V_{REF}ADJ pin and observing good layout practices.

The V_{REF} out node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier is used.

Input Amplifier

The DAC reference amplifier is a high gain internally compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

Figure 1 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}}\left(\frac{DB9}{2}+\frac{DB8}{4}+\frac{DB7}{8}+\frac{DB6}{16}+\frac{DB5}{32}+\frac{DB4}{64}+\frac{DB3}{128}+\frac{DB2}{256}+\frac{DB1}{512}+\frac{DB0}{1024}\right)$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μsec and source impedances at the V_{REF} INPUT greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF}$ INPUT pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF}$ INPUT is grounded and the negative reference is tied directly to the $-V_{REF}$ INPUT. The $-V_{REF}$ INPUT contains a 5kΩ resistor that matches a like resistor in the $+V_{REF}$ INPUT to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on chip output op amp to eliminate the need for additional external active circuits. Its two stage design with feed forward compensation allows it to slew at 15V/μsec and settle to within ±½LSB in 5μsec. These times are typical when driving the rated loads of $R_L \geq 5k$ and $C_L \leq 50pF$ with recommended values of $C_{FF} = 1nF$ and $C_{FB} = 30pF$. Typical input offset voltages of 5mV and 50k open loop gain insure an accurate current to voltage conversion is performed when using the on chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ±15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5 volts to obtain −5V to +5V output voltage range operation. This is accomplished by shorting pins 18 and 22 (see figure 14). This connection produces a current equal to $(V_{REF\,IN} - V_{sum\,node}) \div R_{BIP}$, (1mA nominal), which is injected into the sum node. Since full scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5k = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum mode and $V_{OUT} = -(5k)(1mA) = -5V$. Zero scale adjust and full scale adjust are performed as described below, noting that full scale voltage is now approximately +5 volts, zero scale adjust may be used to trim $V_{OUT} = 0.00$ with the MSB high or $V_{OUT} = -5.0V$ with all bits off.

Zero Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in figure 15. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000 volts in the unipolar mode or −5.000 volts in the bipolar mode (see bipolar section) accomplishes this trim.

Full Scale Adjustment

A recommended full scale adjustment circuit when using the internal voltage reference is shown in figure 16. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accu-

BIPOLAR OUTPUT

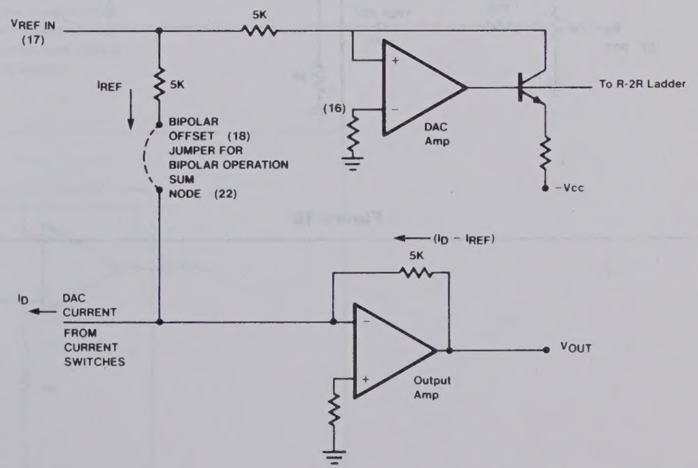


Figure 14

racy of full scale is of low importance when compared to the other system accuracy factors, then this adjustment circuit is optional.

As resistors R_{REF}, R_{fb} and R_{BIP} shown in figure 1 are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full scale (or gain) error is less than ±0.3% of ideal full scale value.

ZERO SCALE ADJUSTMENT

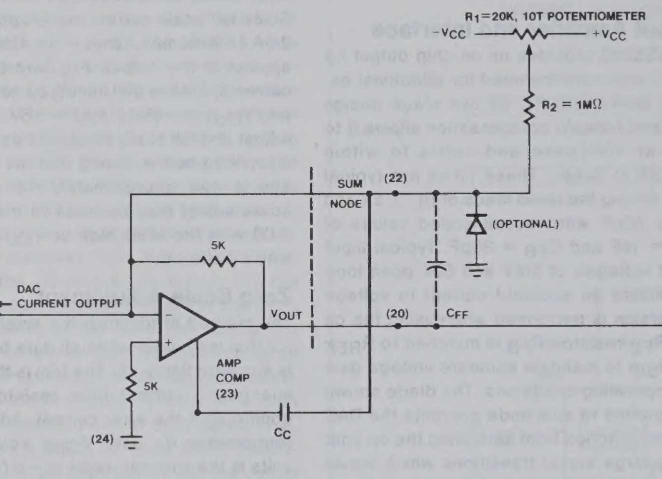

R1=20K, 10T POTENTIOMETER
−VCC
+VCC
R2 = 1MΩ
SUM NODE
(22)
(OPTIONAL)
5K
DAC CURRENT OUTPUT
VOUT
(20)
CFF
AMP COMP (23)
5K
(24)
CC

Figure 15

REFERENCE ADJUST CIRCUIT

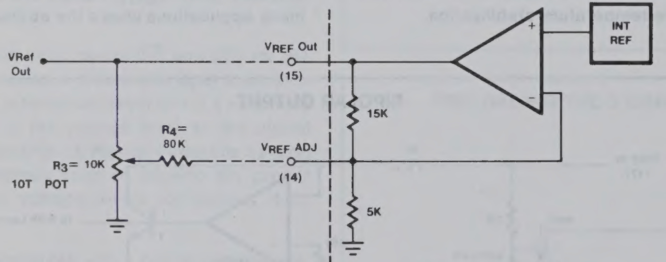

VRef Out
VREF Out
(15)
INT REF
+
−
15K
R4= 80K
VREF ADJ
(14)
R3= 10K
10T POT
5K

Figure 16

SAMPLE AND HOLD AMPLIFIER NE/SE5537

NE/SE5537-H,N • NE5537-H,N

DESCRIPTION

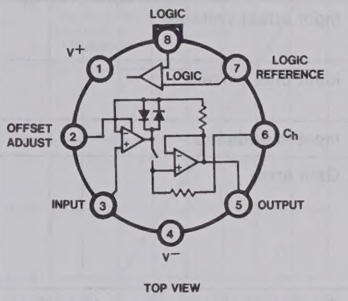
The NE5537 monolithic Sample and Hold amplifier combines the best features of ion implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the Sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2KΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the Sample mode occurring when the logic input is high. It is available in 8-lead TO-5 and 8-pin plastic DIP packages.

FEATURES

- Operates from ±5V to ±18V supplies
- Hold leakage current 6pA @ T_j25°C
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at $C_h = 0.01\mu F$
- Low input offset: 1MV (typical)
- 0.002% gain accuracy with $R_L = 2k\Omega$
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

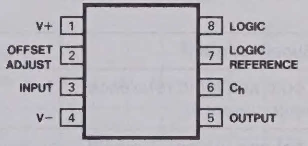
PIN CONFIGURATION

H PACKAGE
Metal Can Package



ORDER PART NO.
NE/SE5537-H

N PACKAGE



ORDER PART NO.
NE/SE5537N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
SE5537	−55 to +125	°C
NE5537	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. The maximum junction temperature of the SE5537 is 150°C and for the NE5537 is100°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θja) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BLOCK DIAGRAM

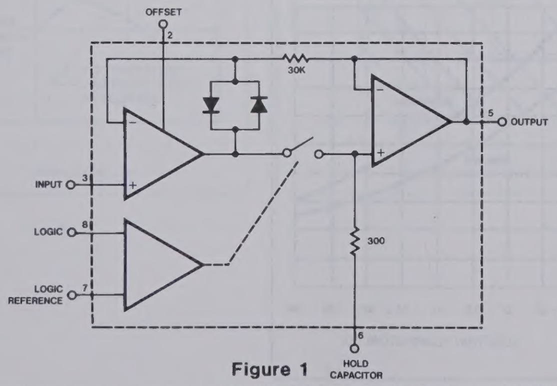


Figure 1

ELECTRICAL CHARACTERISTICS[3]

PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[6]	$T_j = 25°C$ Full temperature range		1	3 5		2	7 10	mV mV
Input bias current[6]	$T_j = 25°C$ Full temperature range		5	25 75		10	50 100	nA nA
Input impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain error	$T_j = 25°C$, $-10V \leq V_{IN} \leq 10V$, $R_L = 2K$ $-11.5V \leq V_{IN} \leq 11.5V$, $R_L = 10K$		0.002	0.007		0.004	0.01	%
	Full temperature range		0.02			0.02		%
Feedthrough attenuation ratio at 1kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output impedance	$T_j = 25°C$, "HOLD" mode full temperature range		0.5	2 4		0.5	4 6	Ω
"HOLD" Step[4]	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply current[6]	$T_j=25°C$		4.5	6.5		4.5	7.5	mA
Logic and logic reference input current	$T_j = 25°C$		2	10		2	10	μA
Leakage current into hold capacitor[6]	$T_j = 25°C$ hold mode[5]		6	50		6	100	pA
Acquisition time to 0.1%	$V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu f$		4 20			4 20		μs μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential logic threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES

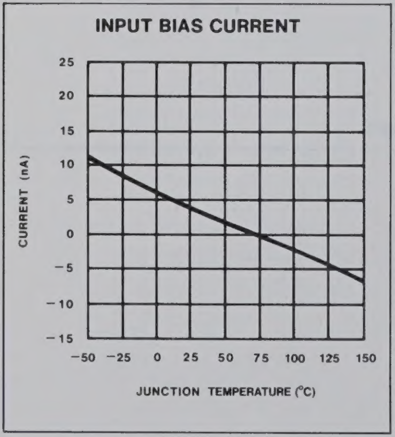
[3] Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq 11.5V$, $C_h = 0.01\mu F$, and $R_L = 2k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

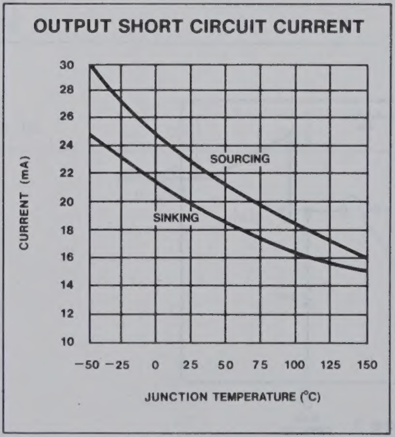
[4] Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

[5] Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

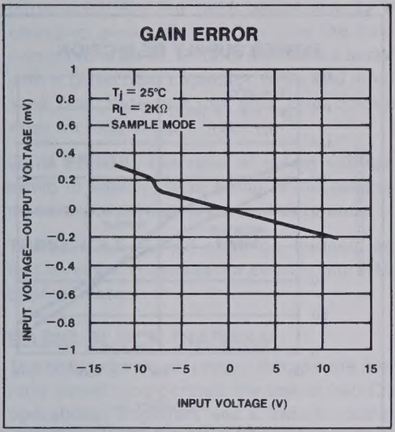
[6] These parameters guaranteed over a supply voltage range of ±5 to ±18V.

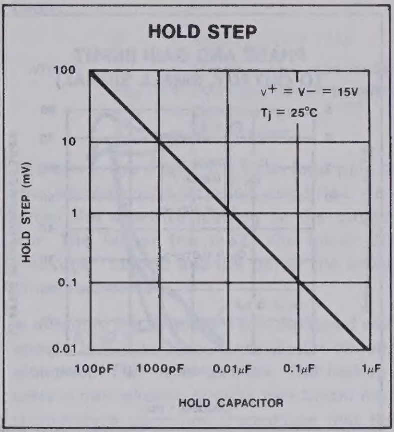
TYPICAL PERFORMANCE CHARACTERISTICS

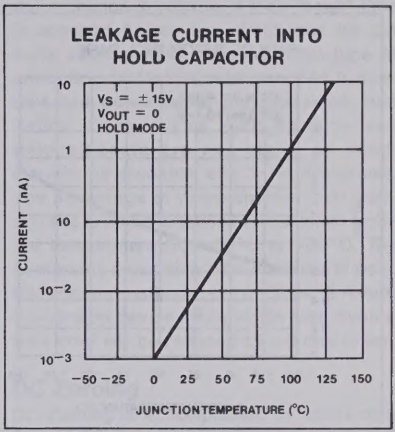

INPUT BIAS CURRENT

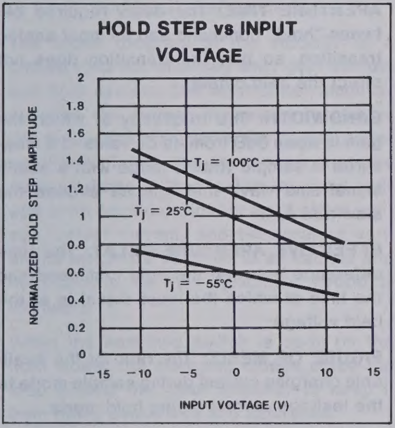

OUTPUT SHORT CIRCUIT CURRENT

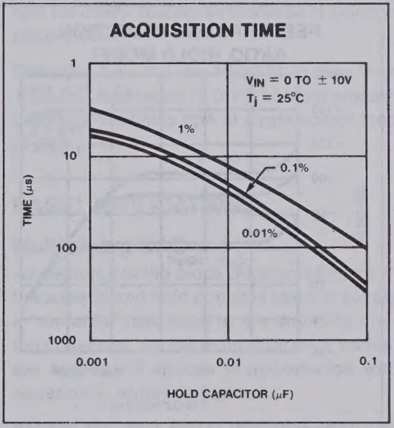
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

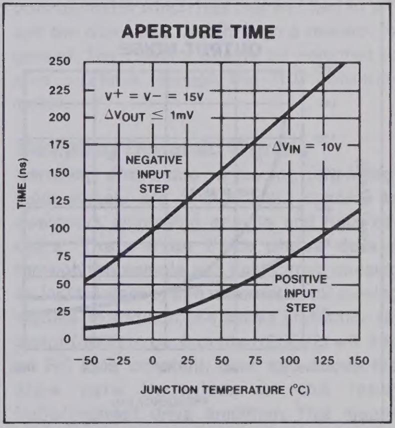

GAIN ERROR

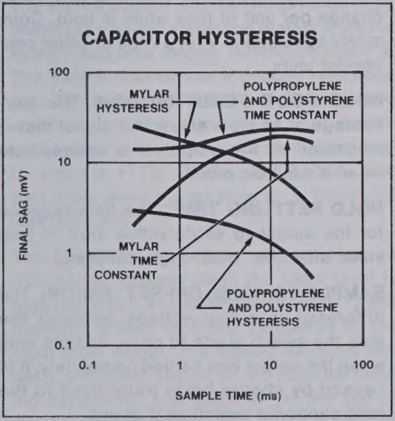

HOLD STEP

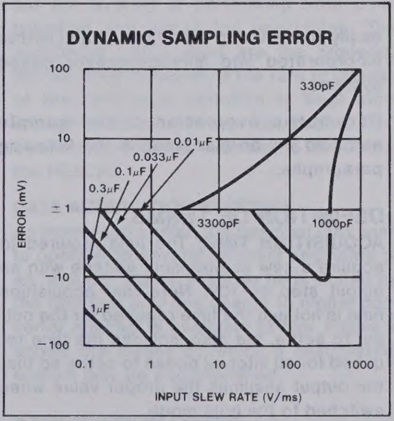

LEAKAGE CURRENT INTO HOLD CAPACITOR

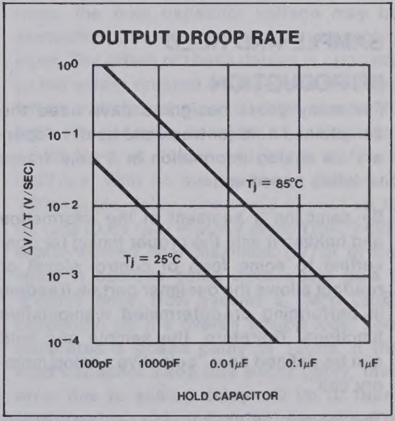

HOLD STEP vs INPUT VOLTAGE


ACQUISITION TIME

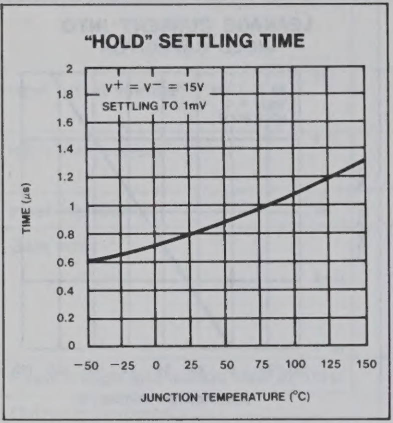

APERTURE TIME

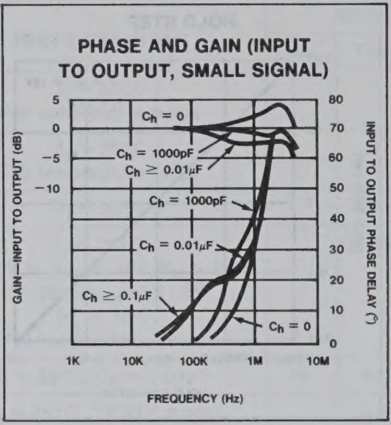

CAPACITOR HYSTERESIS

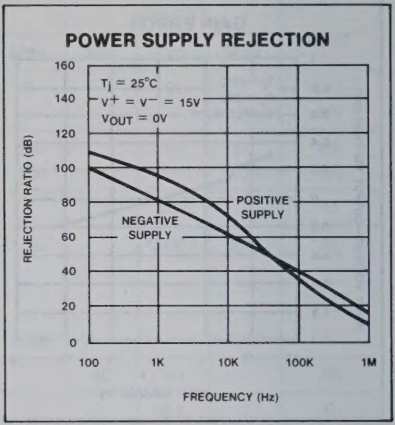

DYNAMIC SAMPLING ERROR

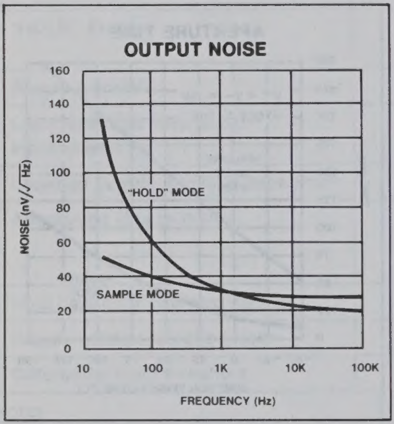

OUTPUT DROOP RATE

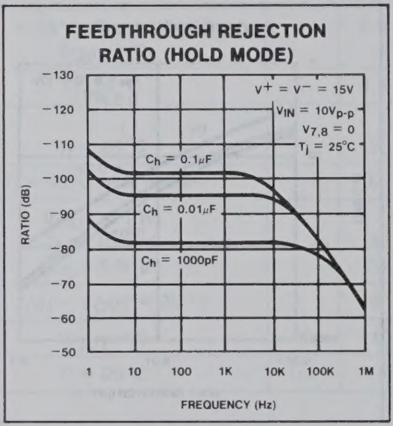
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


"HOLD" SETTLING TIME


PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)


POWER SUPPLY REJECTION


OUTPUT NOISE


FEEDTHROUGH REJECTION RATIO (HOLD MODE)

SAMPLE AND HOLD

INTRODUCTION

For many years designers have used the sample and hold (or track and hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout allows the designer certain freedom in performing predetermined manipulative functions. Therefore, the sample and hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample and hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog to digital converter products available today the "dc memory" of the sample and hold can be easily converted to digital format and further incorporated into microprocessor based systems.

Parametric evaluation of the sample and hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

ACQUISITION TIME: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

APERTURE DELAY TIME: The time elapsed from the hold command to the opening of the switch.

APERTURE JITTER: Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

APERTURE TIME: The delay required between "hold" command and an input analog transition, so that the transition does not affect the held output.

BANDWIDTH: The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

EFFECTIVE APERTURE DELAY: The time difference between the hold command and the time at which the input signal is at the held voltage.

FIGURE OF MERIT: The ratio of the available charging current during sample mode to the leakage current during hold mode.

HOLD-MODE DROOP: The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

HOLD-MODE FEEDTHROUGH: The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

HOLD SETTLING TIME: The time required for the output to settle within 1mV of final value after the "hold" logic command.

SAMPLE-TO-HOLD OFFSET ERROR: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

SLEW RATE: The fastest rate at which the sample & hold output can change (specified in V/μs).

HOLD STEP: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

DYNAMIC SAMPLING ERROR: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

GAIN ERROR: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

THRESHOLD: Level shall be defined as that level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample and hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions). Reference figure 1.

The block diagram of the NE5537 is a closed loop non-inverting unity gain sample and hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop such that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to *all* sample and hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample and hold device. Reference figure 2. The switch control has a floating reference (pin 7), referred to as the logic reference which makes the sample and hold device compatible to several types of external logic signals (TTL, PMOS, & CMOS). The switching device operates at a threshold level of 1.4V.

The switch mechanism is on (sampling an information stream) when the logic level is high (pin 8 is 1.4 volts higher than pin 7) and presents a load of 5 microamperes to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This amplifier, whose input impedance is effectively:

$$R = R_{IN}(A_{OL})/(1 + 1/A)$$

where R = Effective input impedance
R_{IN} = Open loop input impedance
A_{OL} = Open loop gain
A = AC loop gain

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation (remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature).

Sampling time for the NE5537 is less than 10μsec, (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of figure 3, the sample and hold circuit is used to supply a "variable" reference to the digital to analog converter. As the input reference varies, the output will change in accordance with equation 1, shown in figure 3.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DAC's used are the Signetics SE/NE 5008; however, if the rate of change of the reference variation is kept slow enough a microprocessor compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however he is limited by the fact that only one analog to digital converter channel is available to him. Figure 4 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with >1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC Zeroing

DC Zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≃0.6mA through the 1KΩ potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample and hold circuits. There exist finite phase delays through the sample and hold circuit causing an input-output phase differential for moving signals. In addition, the series protection resistor (300Ω to pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) = 60mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs) = −96mV (analog) for a total of −36mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a P.C. card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample and hold systems.
2. Reference should be made to Design Engineering, volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc. for a further discussion of sample and hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

TYPICAL APPLICATIONS

TYPICAL CONNECTION

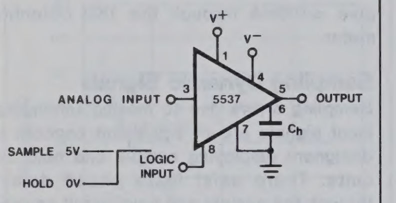
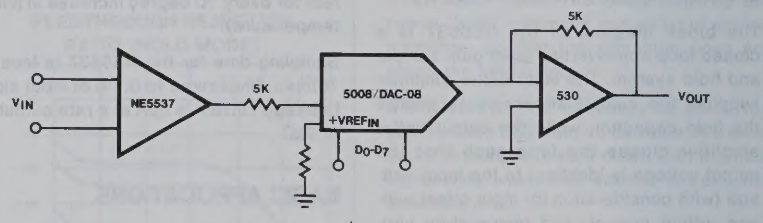

V+
V−
1
4
ANALOG INPUT
3
5537
5
OUTPUT
6
7
Ch
8
SAMPLE 5V
LOGIC INPUT
HOLD 0V

Figure 2

MULTIPLYING DAC APPLICATION


5K
VIN
NE5537
5K
5008/DAC-08
+VREFIN
D0-D7
530
VOUT

$$V_{OUT} = V_{IN} \times \frac{1}{256} \left\{ 2^0 D_0 + 2^1 D_1 + \ldots 2^7 D_7 \right\} \quad \text{EQUATION 1}$$

Figure 3

ANALOG DATA MULTIPLEXING

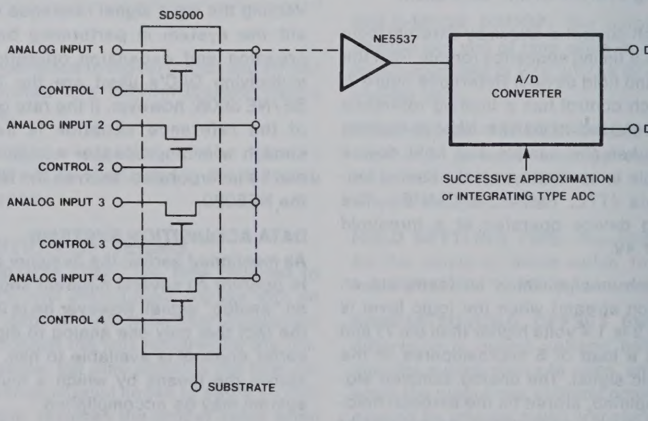

SD5000
ANALOG INPUT 1
CONTROL 1
ANALOG INPUT 2
CONTROL 2
ANALOG INPUT 3
CONTROL 3
ANALOG INPUT 4
CONTROL 4
SUBSTRATE
NE5537
A/D CONVERTER
D0
D7
SUCCESSIVE APPROXIMATION or INTEGRATING TYPE ADC

Figure 4

SECTION II
RADIO CIRCUITS

Section 11—RADIO CIRCUITS

CA3089 FM-IF System 359
MC1496/1596 Balanced Modulator-Demodulator 364
NE544/644 Servo Amplifier 367
NE5044 Programmable Seven Channel RC Encoder 373
NE5045 Seven Channel RC Decoder 376
NE5046 2-Channel RC Decoder 379
TCA440 AM Receiver Circuit 381
μA758 FM Stereo Multiplex Decoder, Phase Locked Loop 388

NEW PRODUCTS

CA3189	FM-IF System—Available 1st Quarter 1981
LM1870	FM Decoder with Stereo/Mono Switching—Available 3rd Quarter 1981

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8 to +18 volts.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40°C to +85°C.

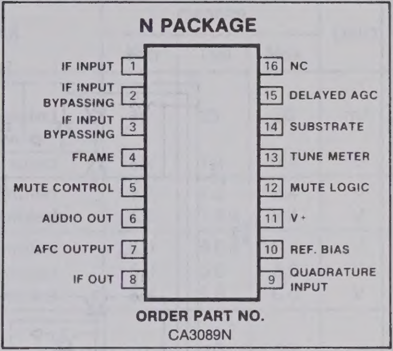
FEATURES

- **Exceptional limiting sensitivity: 10μV typ. at -3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

APPLICATIONS

- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

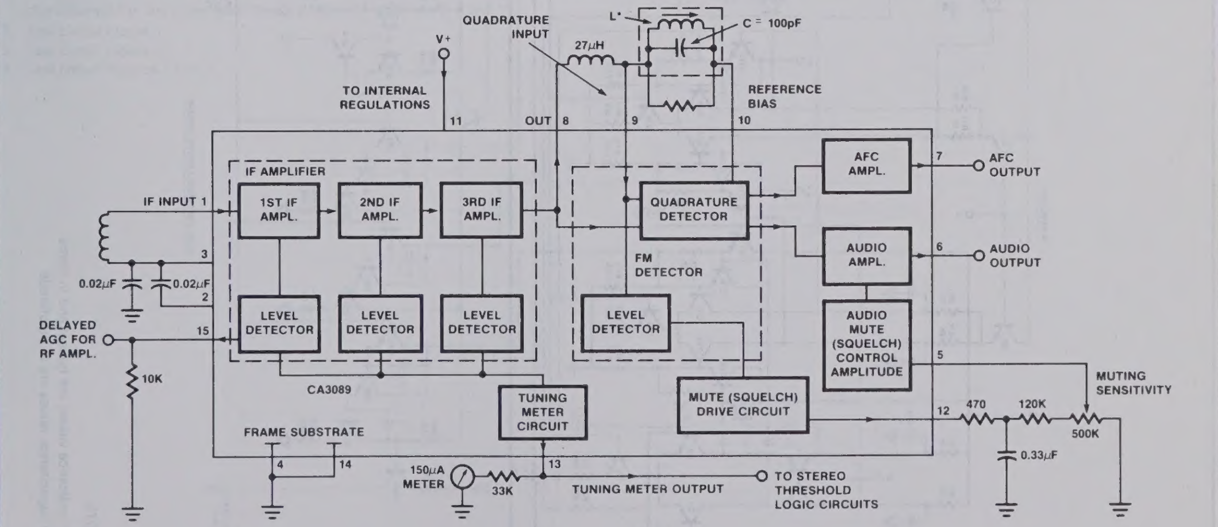
PIN CONFIGURATION


N PACKAGE
IF INPUT 1
IF INPUT BYPASSING 2
IF INPUT BYPASSING 3
FRAME 4
MUTE CONTROL 5
AUDIO OUT 6
AFC OUTPUT 7
IF OUT 8
16 NC
15 DELAYED AGC
14 SUBSTRATE
13 TUNE METER
12 MUTE LOGIC
11 V+
10 REF. BIAS
9 QUADRATURE INPUT
ORDER PART NO.
CA3089N

ABSOLUTE MAXIMUM RATINGS

	RATING	UNIT
DC supply voltage:		
Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC Current (out of terminal 15)	2	mA
Device dissipation:		
Up to $T_A = 60°C$	600	mW
Above $T_A = 60°C$	derate linearly 6.7	mW/°C
Ambient temperature range:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C
Lead temperature (during soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.	+265	°C

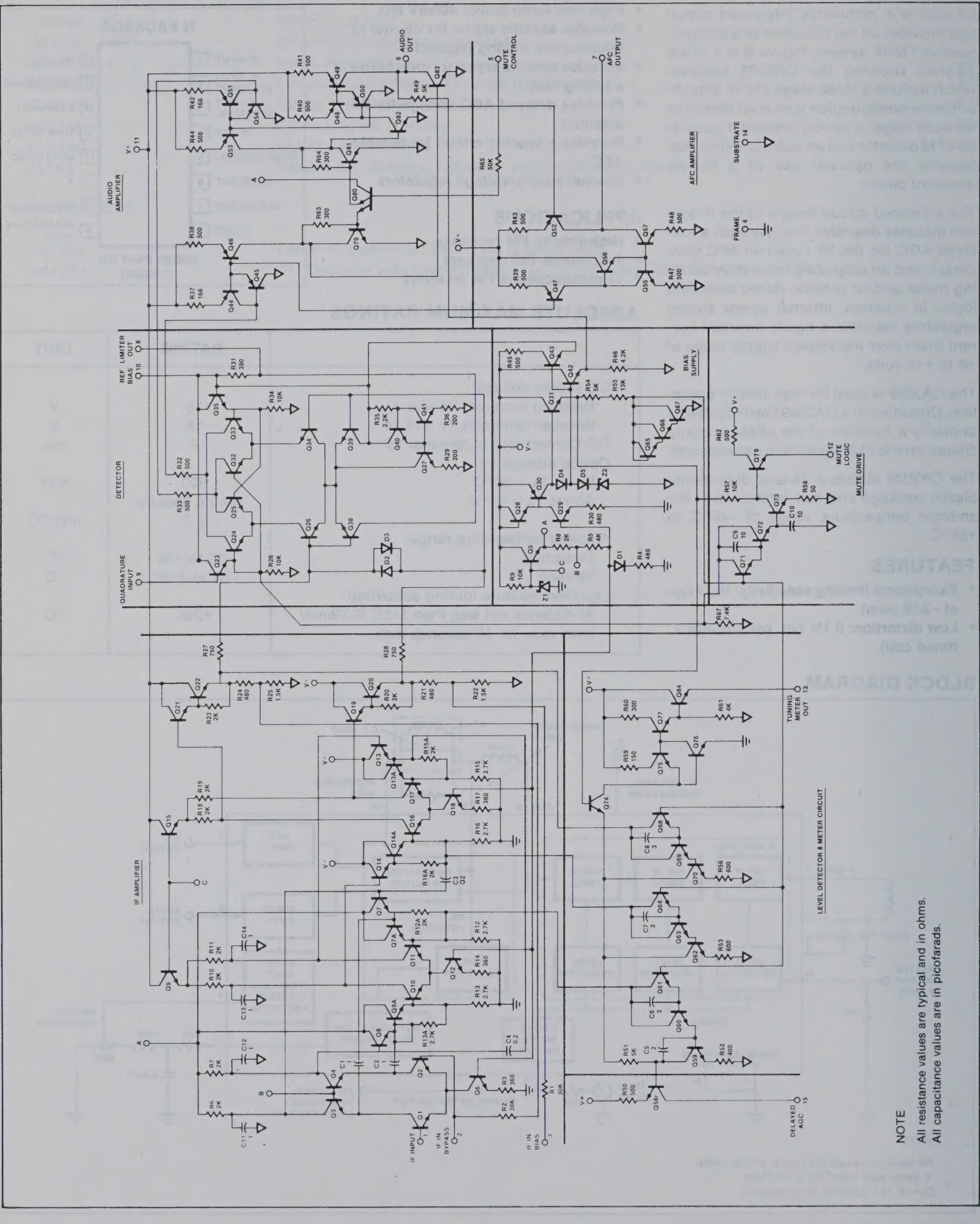
BLOCK DIAGRAM


QUADRATURE INPUT
L*
C = 100pF
V+
27μH
TO INTERNAL REGULATIONS
REFERENCE BIAS
11
OUT 8
9
10
IF AMPLIFIER
IF INPUT 1
1ST IF AMPL.
2ND IF AMPL.
3RD IF AMPL.
QUADRATURE DETECTOR
FM DETECTOR
AFC AMPL.
7
AFC OUTPUT
AUDIO AMPL.
6
AUDIO OUTPUT
3
0.02μF
0.02μF
2
DELAYED AGC FOR RF AMPL.
15
LEVEL DETECTOR
LEVEL DETECTOR
LEVEL DETECTOR
LEVEL DETECTOR
AUDIO MUTE (SQUELCH) CONTROL AMPLITUDE
5
MUTING SENSITIVITY
10K
CA3089
TUNING METER CIRCUIT
MUTE (SQUELCH) DRIVE CIRCUIT
12
470
120K
500K
0.33μF
FRAME SUBSTRATE
4
14
13
150μA METER
33K
TUNING METER OUTPUT
TO STEREO THRESHOLD LOGIC CIRCUITS

NOTE

All resistors values are typical and in ohms.
*L tunes with 100pF (C) at 10.7MHz
$Q_0 \cong 75$ (G.I. EX22741 or equivalent)

EQUIVALENT SCHEMATIC


AUDIO AMPLIFIER
DETECTOR
IF AMPLIFIER
AFC AMPLIFIER
BIAS SUPPLY
MUTE DRIVE
LEVEL DETECTOR & METER CIRCUIT
V+ 11
AUDIO OUT 6
MUTE CONTROL 5
AFC OUTPUT 7
SUBSTRATE 14
FRAME 4
REF BIAS 10
LIMITER OUT 8
QUADRATURE INPUT 9
MUTE LOGIC 12
TUNING METER OUT 13
DELAYED AGC 15
IF INPUT 1
IF IN BYPASS 2
IF IN BIAS 3
V+
A
B
C
R41 500
R42 166
R44 500
R40 500
R49 5K
R64 300
R65 50K
R63 300
R38 500
R37 166
R43 500
R39 500
R48 500
R47 500
R31 390
R34 10K
R35 2.2K
R36 200
R29 200
R32 500
R33 500
R26 10K
R45 500
R46 4.2K
R54 5K
R55 13K
R62 500
R57 10K
R58 50
R9 10K
R8 2K
R5 4K
R30 480
R4 480
R67 7.4K
R27 750
R28 750
R23 2K
R24 480
R25 1.5K
R20 2K
R21 480
R22 1.5K
R60 300
R61 4K
R59 150
R19 2K
R18 2K
R15A 2K
R15 2.7K
R17 360
R16 2.7K
R16A 2K
C3 0.2
R11 2K
R10 2K
R12A 2K
R12 2.7K
R14 360
R13 2.7K
R13A 2.7K
C4 0.2
R7 2K
R6 2K
R3 360
R2 30K
R1 30K
R50 500
R51 5K
R52 400
R56 600
R53 600
C1 1
C2 1
C5 2
C6 3
C7 3
C8 3
C9 10
C10 10
C11 1
C12 1
C13 1
C14 1
D1
D2
D3
D4
D5
Z1
Z2
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q7A Q8 Q8A Q9 Q10 Q11 Q12 Q13 Q13A Q14 Q14A Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31 Q32 Q33 Q34 Q35 Q38 Q39 Q40 Q41 Q42 Q43 Q44 Q45 Q46 Q47 Q48 Q49 Q50 Q51 Q52 Q53 Q54 Q55 Q56 Q57 Q58 Q59 Q60 Q61 Q62 Q63 Q64 Q65 Q66 Q67 Q68 Q69 Q70 Q71 Q72 Q73 Q74 Q75 Q76 Q77 Q78 Q79 Q80 Q81 Q82 Q83 Q84

NOTE
All resistance values are typical and in ohms.
All capacitance values are in picofarads.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$ unless otherwise specified.

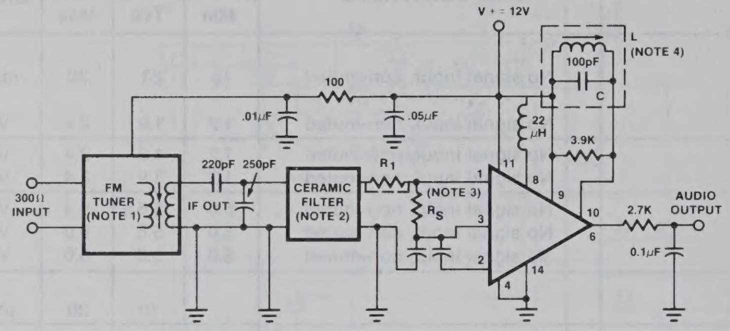
PARAMETER		TEST CONDITIONS	CA3089			UNIT
			Min	Typ	Max	
STATIC (DC) CHARACTERISTICS						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages:[4]						
V_1	Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2	Terminal 2 (ac return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3	Terminal 3 (dc bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6	Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.4	V
V_7	Terminal 7 (A.F.C.)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10}	Terminal 10 (dc reference)	No signal input, non-muted	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS						
$V_{I(lim)}$	Input limiting voltage (-3dB point)[3]			10	30	µV
	AMR AM Rejection (terminal 6)[4]	$V_{IN} = 0.1V$, $F_o = 10.7MHz$, $f_{mod} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (terminal 6)[3]		300	400	500	mV
Total harmonic distortion:[1]						
THD	Single tuned (terminal 6)[3]			0.5	1.0	%
THD	Double tuned (terminal 6)[4]	$f_{mod} = 400Hz$, $V_{IN} = 0.1$		0.1		%
S+N/N	Signal plus noise to noise ratio (terminal 6)[3]	Deviation = ±75kHz	60	67		dB
MU_{IN}	Mute input (terminal 5)	$V_5 = 2.5V$		70		dB
MU_{OUT}	Mute output (terminal 12)	$V_{IN} = 50\mu V$			.5	V
		$V_{IN} = 0V$	4.0			V
MTR	Meteroutput (terminal 13)	$V_{IN} = 0.1V$	3.5	4.5		V
		$V_{IN} = 500\mu V$	1.0	1.5		V
		$V_{IN} = 0V$			.7	V
AGC	Delayed AGC (terminal 15)	$V_{IN} = 0.1V$			.5	V
		$V_{IN} = 10\mu V$	4.0	5.0		V
THD	Double tuned (terminal 6)[4]	$f_{mod} = 400Hz$ $V_{IN} = 0.1$		0.1		%

NOTES

1. THD characteristics and Audio Level are essentiallly a function of the phase and Q characteristics of the network connected between terminals 8, 9 and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

TEST CIRCUITS

TYPICAL FM TUNER (With a single-tuned detector coil.)



NOTES: All resistors values are typical and in ohms.

1. Waller 4SN3FIC or equivalent
2. Murate SFG 10.7mA or equivalent
3. R_S will affect stability depending on circuit layout. To increase stability R_S is decreased. Range of R_S is 330 to 50Ω, $R_1 + R_S \leq 330\Omega$
4. L tunes with 100pF (C) at 10.7MHz
   Q_o unloaded ≅ 75 (G.I. EX2274I or equivalent)

Performance data at f_o = 98MHz, f_{MOD} = 400Hz, deviation = ±74kHz:

-3dB limiting sensitivity	2μV (antenna level)
20dB quieting sensitivity	1μV (antenna level)
30dB quieting sensitivity	1.5μV (antenna level)

SYSTEM DESIGN CONSIDERATIONS

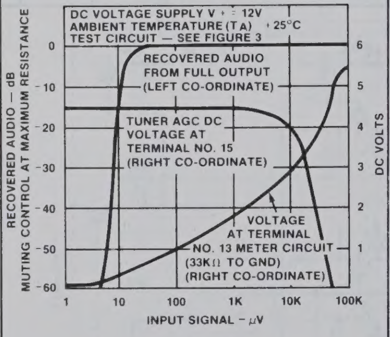
The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input by-pass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good by-pass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.

The input impedance of the CA3089 is approximately 10,000 ohms. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

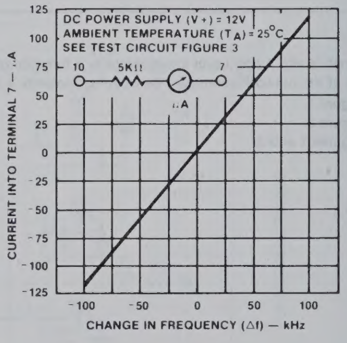
MUTING ACTION, TUNER AGC

(Tuning meter output as a function of input signal voltage.)



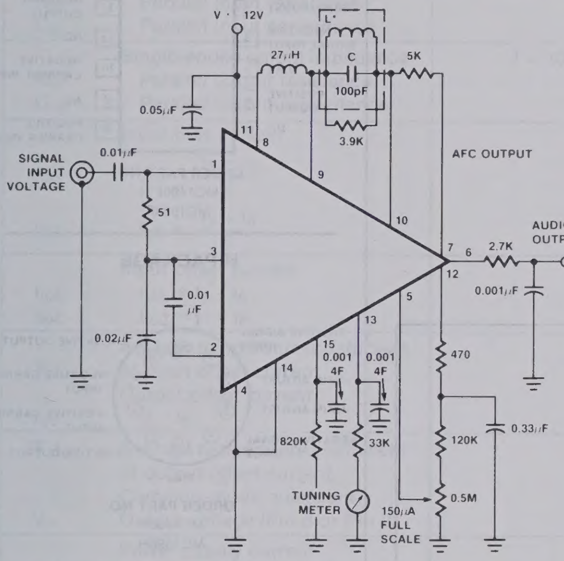
AFC CHARACTERISTICS

(Current at Term. 7 as a function of change in frequency.)



TEST CIRCUITS

TEST CIRCUIT
(Using a single-tuned detector coil.)

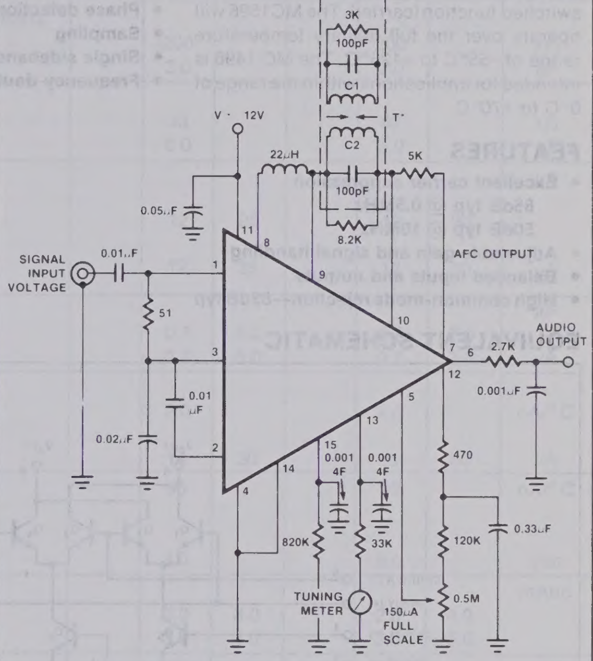

V+ 12V
27μH
L*
C
100pF
3.9K
5K
0.05μF
SIGNAL INPUT VOLTAGE
0.01μF
51
0.01 μF
0.02μF
1
2
3
4
8
9
10
11
12
13
14
15
5
6
7
AFC OUTPUT
AUDIO OUTPUT
2.7K
0.001μF
0.001 4F
0.001 4F
820K
33K
470
120K
0.33μF
0.5M
TUNING METER
150μA FULL SCALE

*NOTE

L tunes with 100pF (C) at 10.7MHz.
All resistors values are typical and in ohms.
Q_0 (unloaded) ≅ 75 (G.I. automatic mfg. div. EX22741 or equivalent).

Figure 1

TEST CIRCUIT
(Using a double-tuned detector coil.)


3K
100pF
C1
T*
C2
100pF
8.2K
V+ 12V
22μH
5K
0.05μF
SIGNAL INPUT VOLTAGE
0.01μF
51
0.01 μF
0.02μF
1
2
3
4
8
9
10
11
12
13
14
15
5
6
7
AFC OUTPUT
AUDIO OUTPUT
2.7K
0.001μF
0.001 4F
0.001 4F
820K
33K
470
120K
0.33μF
0.5M
TUNING METER
150μA FULL SCALE

*NOTE: All resistors values are typical and in ohms.

T: Pri. – Q_0 (unloaded) ≅ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32" dia. form)
Sec. – Q_0 (unloaded) ≅ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32" dia. form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C) = 150mV

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm

Figure 2

MC1496-F,N,H
MC1596-F,H

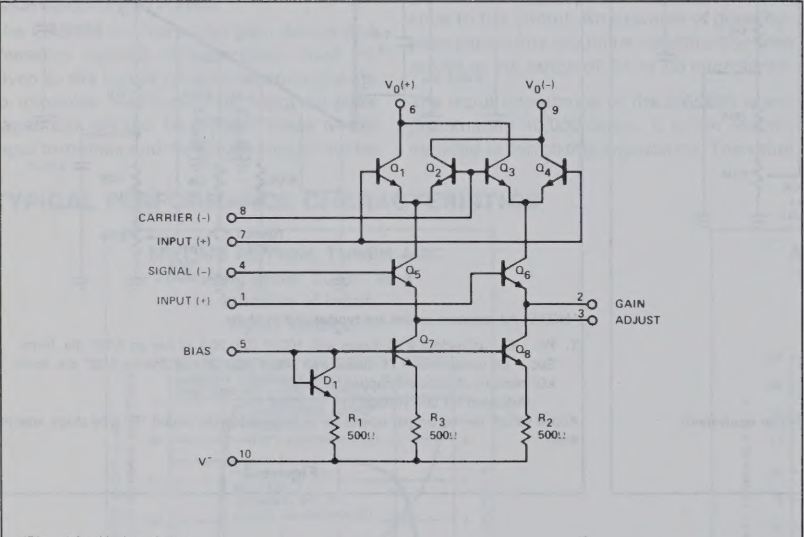
DESCRIPTION

The MC1496 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of –55°C to +125°C. The MC 1496 is intended for applications within the range of 0°C to +70°C.

FEATURES

- **Excellent carrier suppression**
  65dB typ @ 0.5MHz
  50dB typ @ 10MHz
- **Adjustable gain and signal handling**
- **Balanced inputs and outputs**
- **High common-mode rejection—85dB typ**

EQUIVALENT SCHEMATIC


$V_0(+)$
6
$V_0(-)$
9
Q_1
Q_2
Q_3
Q_4
CARRIER (-)
8
INPUT (+)
7
SIGNAL (-)
4
Q_5
Q_6
INPUT (+)
1
2
3
GAIN
ADJUST
BIAS
5
Q_7
Q_8
D_1
R_1
500Ω
R_3
500Ω
R_2
500Ω
V^-
10

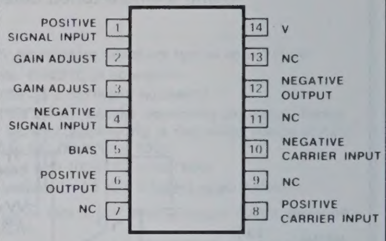
(Pinout for H pkg. shown)

APPLICATIONS

- **Suppressed carrier and amplitude modulation**
- **Synchronous detection**
- **FM detection**
- **Phase detection**
- **Sampling**
- **Single sideband**
- **Frequency doubling**

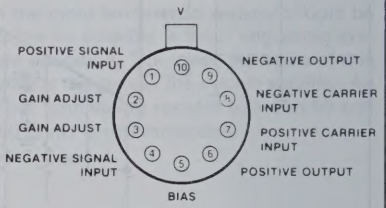
PIN CONFIGURATIONS

F, N PACKAGE


POSITIVE SIGNAL INPUT
1
GAIN ADJUST
2
GAIN ADJUST
3
NEGATIVE SIGNAL INPUT
4
BIAS
5
POSITIVE OUTPUT
6
NC
7
14
V
13
NC
12
NEGATIVE OUTPUT
11
NC
10
NEGATIVE CARRIER INPUT
9
NC
8
POSITIVE CARRIER INPUT

ORDER PART NO.
MC1496F,N
MC1596F

H PACKAGE


V
POSITIVE SIGNAL INPUT
GAIN ADJUST
GAIN ADJUST
NEGATIVE SIGNAL INPUT
1
2
3
4
5
6
7
8
9
10
NEGATIVE OUTPUT
NEGATIVE CARRIER INPUT
POSITIVE CARRIER INPUT
POSITIVE OUTPUT
BIAS

ORDER PART NO.
MC1496H
MC1596H

*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Applied voltage[1,2]	30	V
Differential input signal (V_7-V_8)	±5.0	V
Differential input signal (V_4-V_1)	($5 \pm I_5 R_e$)	V
Input signal (V_2-V_1, V_3-V_4)	5.0	V
Bias current (I_5)	10	mA
Power dissipation (pkg. limitation)		
N package	900	mW
Operating temperature range		
MC1496	0 to +70	°C
MC1596	-55 to +125	°C
Storage temperature range	-65 to +150	°C

NOTES

1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to H package pinout only.

MC1496-F,N,H
MC1596-F,H

DC ELECTRICAL CHARACTERISTICS

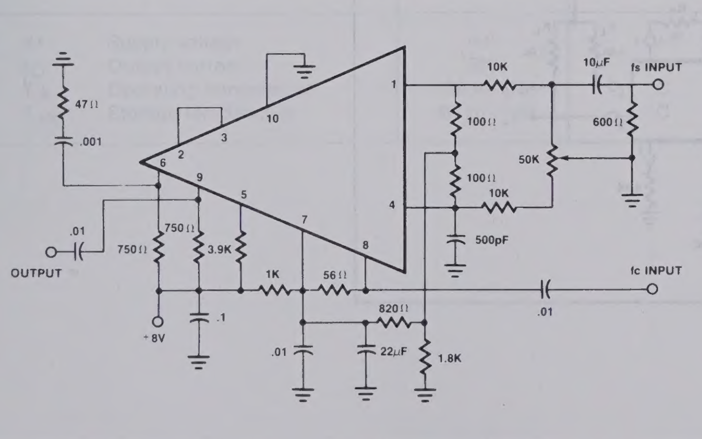
$V^+ = +12Vdc$, $V^- = -8.0Vdc$, $I_5 = 1.0mAdc$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = 25°C$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Single-ended input impedance	Signal port, f = 5.0MHz							
R_{ip}	Parallel input resistance			200			200		kΩ
C_{ip}	Parallel input capacitance			2.0			2.0		pF
	Single-ended output impedance	f = 10MHz							
R_{op}	Parallel output resistance			40			40		kΩ
C_{op}	Parallel output capacitance			5.0			5.0		pF
	Input bias current								μA
I_{bS}	$I_{bS} = \frac{I_1 + I_4}{2}$			12	25		12	30	
I_{bC}	$I_{bS} = \frac{I_7 + I_8}{2}$			12	25		12	30	μA
	Input offset current								μA
I_{ioS}	$I_{ioS} = I_1 - I_4$			0.7	5.0		0.7	7.0	
I_{ioC}	$I_{ioC} = I_7 - I_8$			0.7	5.0		0.7	7.0	μA
TcI_{io}	Average temperature coefficient of input offset current			2.0			2.0		nA/°C
I_{oo}	Output offset current $I_6 - I_9$			14	50		15	80	μA
TcI_{oo}	Average temperature coefficient of output offset current			90			90		nA/°C
V_o	Common-mode quiescent Output voltage (Pin 6 or Pin 9)			8.0			8.0		Vdc
	Power supply current								mAdc
I_{D+}	$I_6 + I_9$			2.0	3.0		2.0	4.0	
I_{D-}	I_{10}			3.0	4.0		3.0	5.0	
P_D	DC power dissipation			33			33		mW

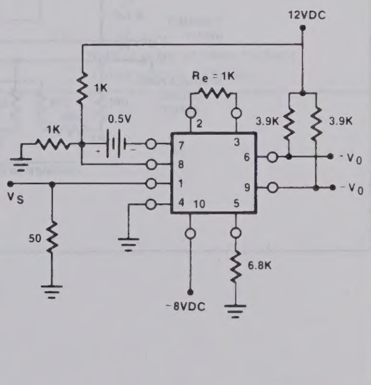
NOTE

Pin number references pertain to H package pinout only.

CARRIER REJECTION AND SUPPRESSION


47Ω
.001
3
2
6
10
9
5
7
8
1
4
10K
10μF
fs INPUT
100Ω
600Ω
50K
100Ω
10K
500pF
.01
OUTPUT
750Ω
750Ω
3.9K
1K
56Ω
fc INPUT
.01
+8V
.1
820Ω
.01
22μF
1.8K

SIGNAL GAIN AND OUTPUT SWING


12VDC
1K
Re = 1K
0.5V
1K
2
3
3.9K
3.9K
7
8
6
-Vo
1
9
-Vo
VS
4
10
5
50
6.8K
-8VDC

MC1496-F,N,H
MC1596-F,H

AC ELECTRICAL CHARACTERISTICS

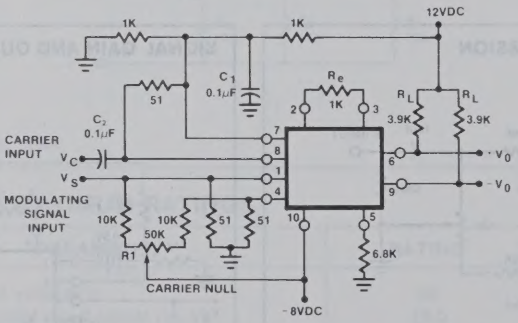
$V^+ = +12$Vdc, $V^- = -9.0$Vdc, $I_5 = 1.0$mAdc, $R_L = 3.9$kΩ, $R_e = 1.0$kΩ, $T_A = +25°C$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	$V_c = 60$mVrms sinewave and offset adjusted to zero							
		$f_C = 1.0$kHz		40			40		µVrms
		$f_C = 10$MHz		140			140		
		$V_c = 300$mVp-p squarewave:							
		Offset adjusted to zero $f_C = 1.0$kHz		0.04	0.2		0.04	0.4	mVrms
		Offset not adjusted $f_C = 1.0$kHz		20	100		20	200	
V_{CS}	Carrier suppressions	$f_S = 10$kHz, 300mVrms sinewave							
		$f_C = 500$kHz, 60mVrms sinewave	50	65		40	65		dB
		$f_C = 10$MHz, 60mVrms sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth (Magnitude) ($R_L = 50Ω$)	Carrier input port, $V_C = 60$mVrms sinewave $f_S = 1.0$kHz, 300mVrms sinewave		300			300		MHz
		Signal input port, $V_S = 300$mVrms sinewave $\|V_C\| = 0.5$Vdc		80			80		MHz
AV_S	Signal gain	$V_S = 100$mVrms; f = 1.0kHz $\|V_C\| = 0.5$Vdc	2.5	3.5		2.5	3.5		V/V
CMV	Common-mode input swing	Signal port, $f_s = 1.0$kHz		5.0			5.0		Vp-p
ACM	Common-mode gain	Signal port, $f_S = 1.0$kHz $\|V_C\| = 0.5$Vdc		-85			-85		dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		Vp-p

NOTE

Pin number references pertain to H package pinout only.

CARRIER REJECTION AND SUPPRESSION


1K
1K
12VDC
C1 0.1µF
51
Re 1K
2
3
RL 3.9K
RL 3.9K
C2 0.1µF
CARRIER INPUT
VC
VS
MODULATING SIGNAL INPUT
7
8
1
4
6
9
+V0
-V0
10K
10K
50K
R1
51
51
10
5
6.8K
CARRIER NULL
-8VDC

NE544/644-N,W
NE544-D

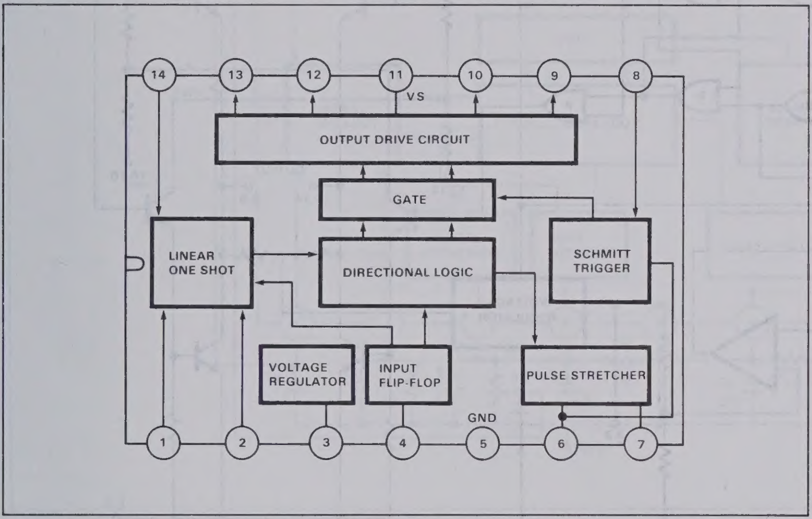
DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

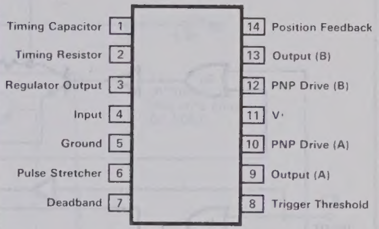
- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

BLOCK DIAGRAM


14
13
12
11
10
9
8
VS
OUTPUT DRIVE CIRCUIT
GATE
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
GND
1
2
3
4
5
6
7

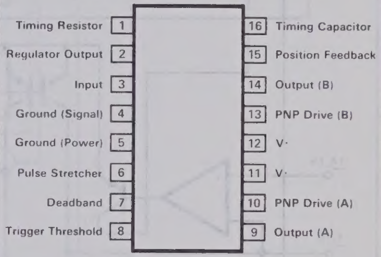
PIN CONFIGURATIONS

D,N PACKAGE


Timing Capacitor 1
Timing Resistor 2
Regulator Output 3
Input 4
Ground 5
Pulse Stretcher 6
Deadband 7
8 Trigger Threshold
9 Output (A)
10 PNP Drive (A)
11 V+
12 PNP Drive (B)
13 Output (B)
14 Position Feedback

ORDER PART NO.
NE544N
NE544D

N PACKAGE


Timing Resistor 1
Regulator Output 2
Input 3
Ground (Signal) 4
Ground (Power) 5
Pulse Stretcher 6
Deadband 7
Trigger Threshold 8
9 Output (A)
10 PNP Drive (A)
11 V+
12 V+
13 PNP Drive (B)
14 Output (B)
15 Position Feedback
16 Timing Capacitor

Order part no. NE644N

W PACKAGE*

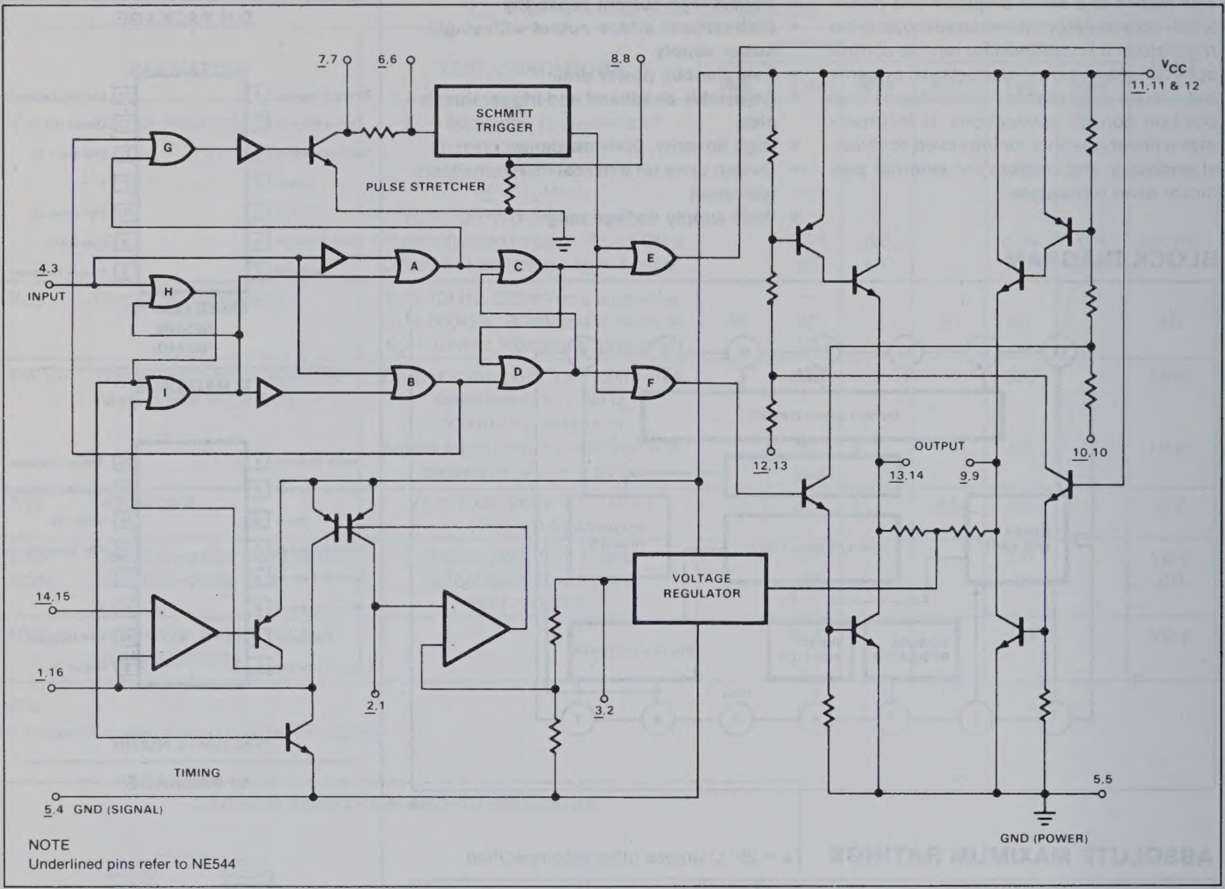
*Pinout same as 644N package
Order part no. NE644W

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

PARAMETER		RATING	UNIT
V+	Supply voltage	6.0	V
I_O	Output current	500	mA
T_A	Operating temperature	-20 to +75	°C
T_{stg}	Storage temperature	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC

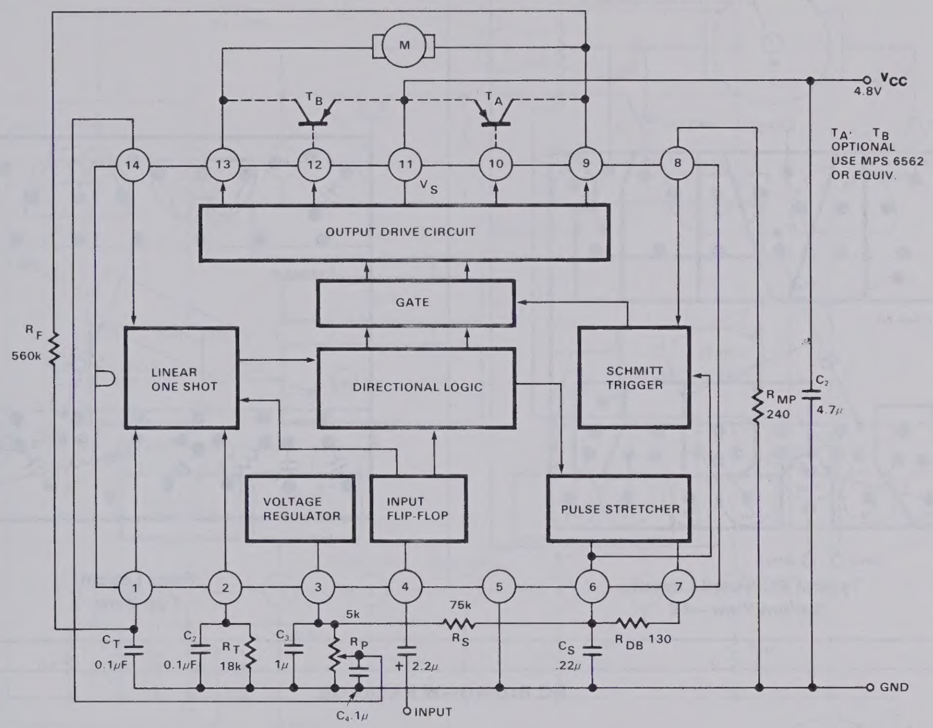

7,7
6,6
8,8
V_CC
11,11 & 12
SCHMITT TRIGGER
PULSE STRETCHER
G
H
I
A
B
C
D
E
F
4,3
INPUT
12,13
OUTPUT
13,14
9,9
10,10
14,15
1,16
2,1
3,2
VOLTAGE REGULATOR
TIMING
5,4 GND (SIGNAL)
5,5
GND (POWER)

NOTE
Underlined pins refer to NE544

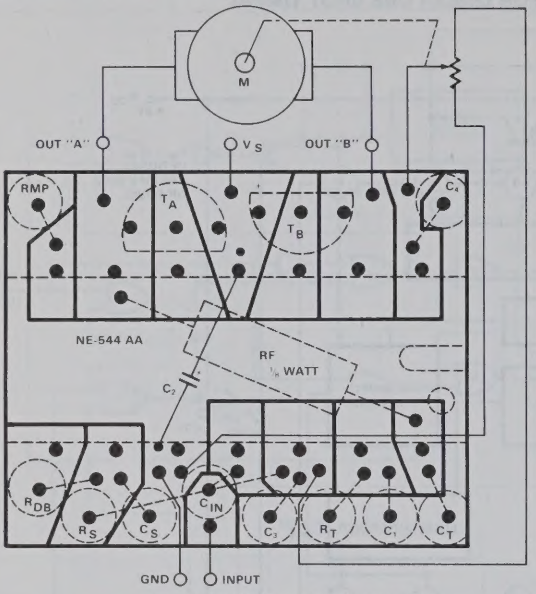
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 4.8V$ unless otherwise specified.

PARAMETER			TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage			3.2	4.8	6	V
I_{CC}	Supply current	Pin 11	Quiescent	4.2	5.5	10	mA
V_{TH}	Input threshold	Pin 4					V
	On				1.5		
	Off				1.4		
Z_{IN}	Input resistance	Pin 4			18		kΩ
	Output voltage						V
V_{OL}	Low		Pin 9 or 13, $I_L = 400mA$		0.3		
V_{OH}	High				3.9		
V_{REG}	Regulated voltage	Pin 3		2.1	2.5	2.9	V
ΔV_{REG}	Regulation	Pin 3	$3.5V \leq V_{CC} \leq 6V$		10		mV/V
	Minimum dead band	Pin 7	$R_{DB} = 0$		1		μs
	One shot temperature coefficient				.01		%/°C
	Standby output voltage		Pin 9 and 13		2.5		V
	PNP drive current		Pin 10 and 12		20		mA

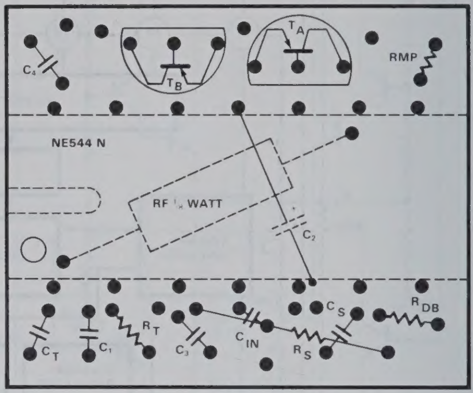
TYPICAL CONNECTION OF NE544N FOR LINEAR ONE SHOT TIMING


M
T_B
T_A
VCC
4.8V
T_A, T_B
OPTIONAL
USE MPS 6562
OR EQUIV.
14
13
12
11
10
9
8
V_S
OUTPUT DRIVE CIRCUIT
GATE
R_F
560k
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
R_MP
240
C_2
4.7μ
VOLTAGE REGULATOR
INPUT FLIP-FLOP
PULSE STRETCHER
1
2
3
4
5
6
7
5k
75k
R_S
R_DB 130
C_T
0.1μF
C_2
0.1μF
R_T
18k
C_3
1μ
R_P
+ 2.2μ
C_S
.22μ
C_4 .1μ
INPUT
GND

PC BOARD—N PACKAGE

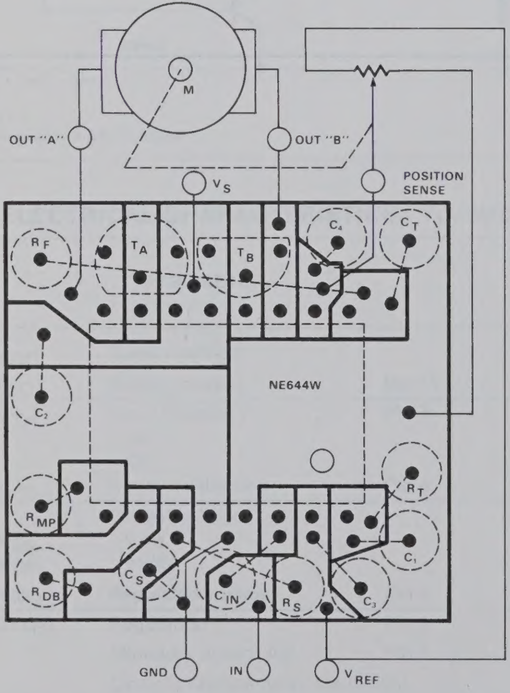

M
OUT "A"
V S
OUT "B"
RMP
T A
T B
C4
NE-544 AA
RF
1/8 WATT
C2
R DB
R S
C S
C IN
C3
R T
C1
C T
GND
INPUT

Typical PC Board Layout
Bottom View—4X

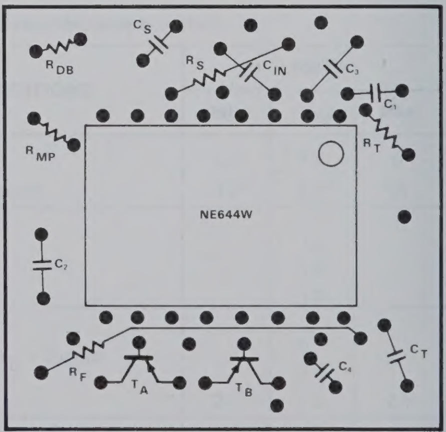

C4
T B
T A
RMP
NE544 N
RF 1/4 WATT
C2
C T
C1
R T
C3
C IN
R S
C S
R DB

Parts Layout
Top View

PC BOARD—W PACKAGE

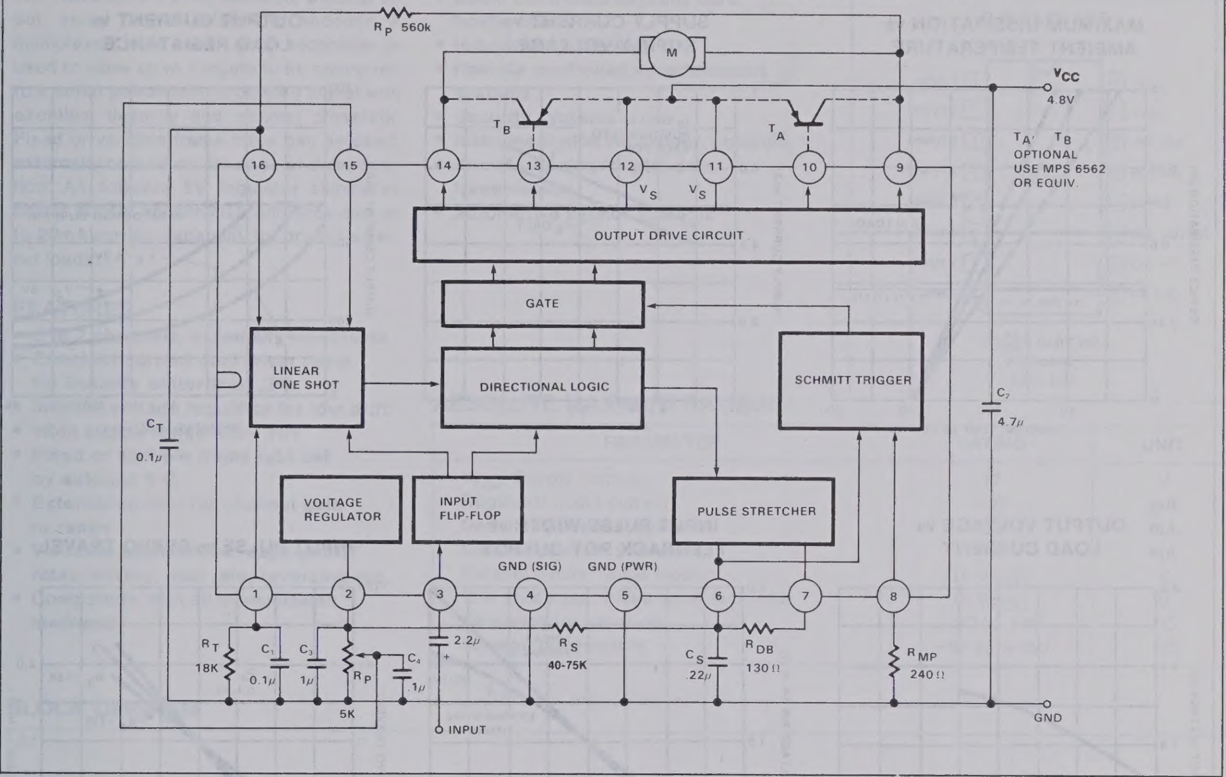

M
OUT "A"
OUT "B"
V S
POSITION SENSE
R F
T A
T B
C4
C T
NE644W
C2
R MP
R T
C1
R DB
C S
C IN
R S
C3
GND
IN
V REF

PC Board Layout
Bottom View—4X


C S
R DB
R S
C IN
C3
C1
R MP
R T
NE644W
C2
R F
T A
T B
C4
C T

Parts Layout
Top View

TYPICAL CONNECTION OF NE644W AND NE644N FOR LINEAR ONE SHOT TIMING

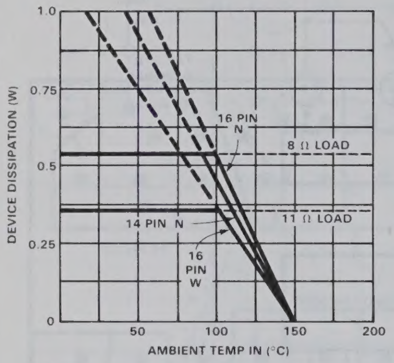


R_P 560k
M
T_B
T_A
V_CC
4.8V
T_A, T_B
OPTIONAL
USE MPS 6562
OR EQUIV.
16
15
14
13
12
11
10
9
V_S
V_S
OUTPUT DRIVE CIRCUIT
GATE
LINEAR
ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
C_T
0.1μ
C_2
4.7μ
VOLTAGE
REGULATOR
INPUT
FLIP-FLOP
PULSE STRETCHER
GND (SIG)
GND (PWR)
1
2
3
4
5
6
7
8
2.2μ
R_T
18K
C_1
0.1μ
C_3
1μ
R_P
5K
C_4
.1μ
R_S
40-75K
C_S
.22μ
R_DB
130Ω
R_MP
240Ω
INPUT
GND

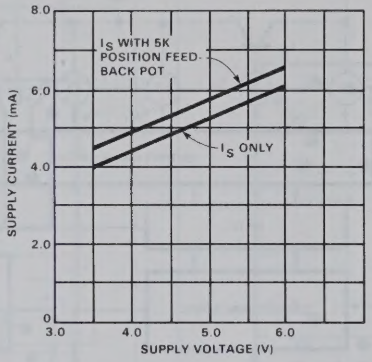
NE544/644-N,W
NE544-D

TYPICAL PERFORMANCE CHARACTERISTICS

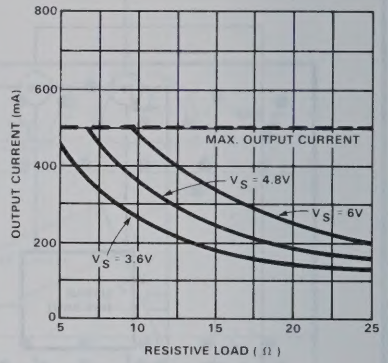
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



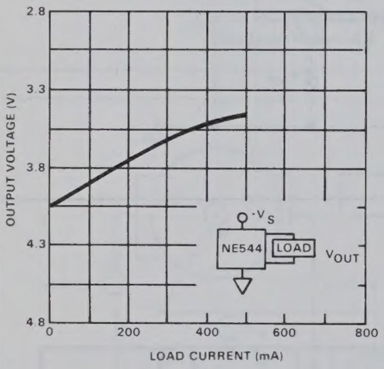
SUPPLY CURRENT vs SUPPLY VOLTAGE



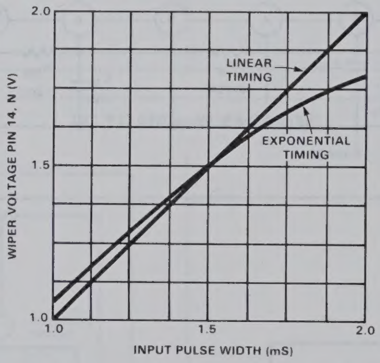
OUTPUT CURRENT vs LOAD RESISTANCE



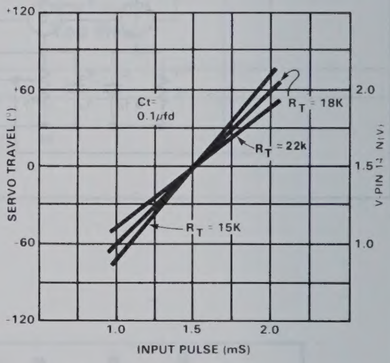
OUTPUT VOLTAGE vs LOAD CURRENT



INPUT PULSE WIDTH vs FEEDBACK POT OUTPUT



INPUT PULSE vs SERVO TRAVEL



PROGRAMMABLE SEVEN CHANNEL RC ENCODER NE5044

NE5044-D,N

DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulsewidth encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulsewidth modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An onboard 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

FEATURES

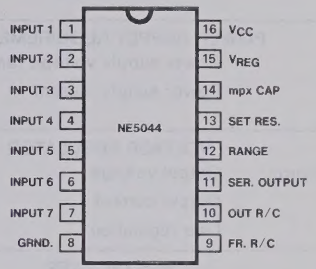
- **3 to 7 channels, externally selectable**
- **Constant current dual linear ramp for linearity better than .3%**
- **Internal voltage regulator for low drift**
- **Wide supply range 4.5 – 16V**
- **Fixed or variable frame rate set by external R-C**
- **External control for channel gain or range**
- **Versatile applications; exponential rates, mixing, dual rate, reversing etc.**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**

PIN CONFIGURATION

D,N PACKAGE


INPUT 1 1
INPUT 2 2
INPUT 3 3
INPUT 4 4
INPUT 5 5
INPUT 6 6
INPUT 7 7
GRND. 8
NE5044
16 VCC
15 VREG
14 mpx CAP
13 SET RES.
12 RANGE
11 SER. OUTPUT
10 OUT R/C
9 FR. R/C

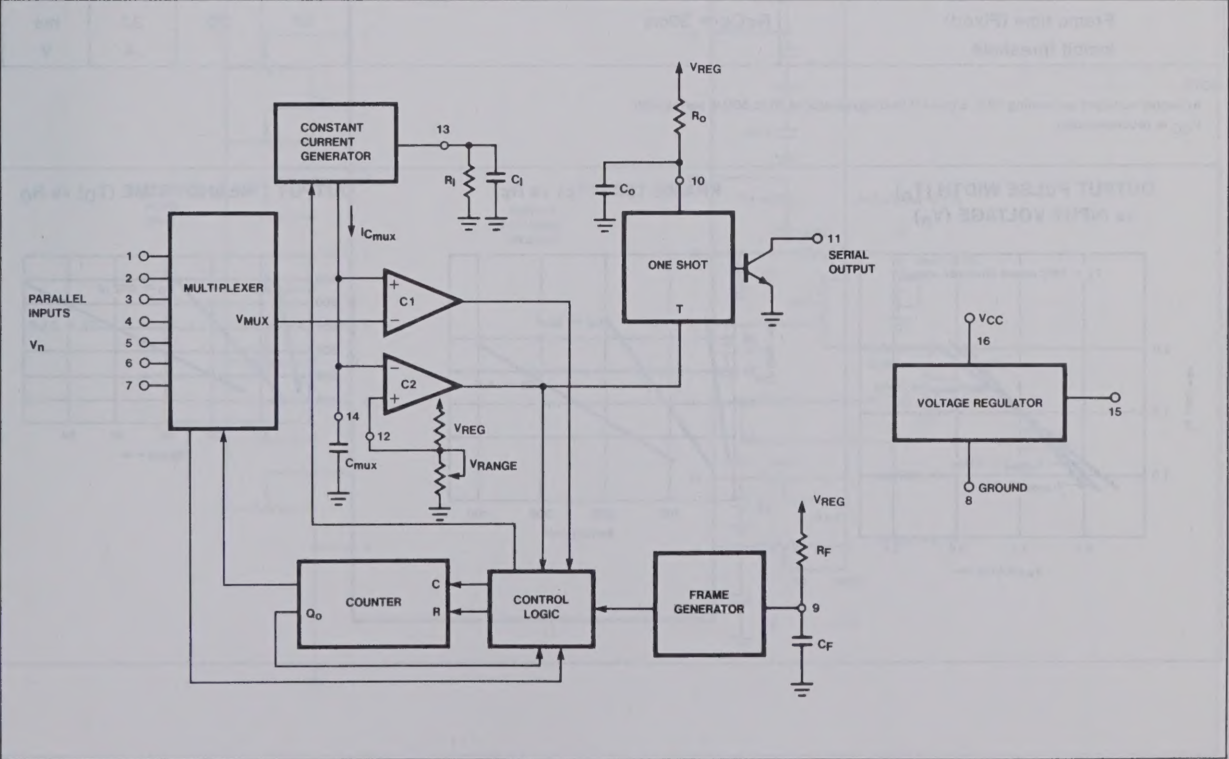
ORDER PART NO.
NE5044D
NE5044N

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	17	V
Regulator ouput current	−25	mA
Serial output peak current	30	mA
Constant current generator	−1	mA
Parallel inputs, range input	0-V_{REG}	V
One shot input, frame generator input	0-V_{REG}	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE
1. T_A = 25° unless otherwise stated.

BLOCK DIAGRAM


VREG
RO
CONSTANT CURRENT GENERATOR
13
RI
CI
CO
10
ICmux
ONE SHOT
T
11
SERIAL OUTPUT
1
2
3
4
5
6
7
PARALLEL INPUTS
Vn
MULTIPLEXER
VMUX
C1
C2
14
12
Cmux
VREG
VRANGE
VCC
16
VOLTAGE REGULATOR
15
GROUND
8
VREG
RF
COUNTER
QO
C
R
CONTROL LOGIC
FRAME GENERATOR
9
CF

NE5044-D,N

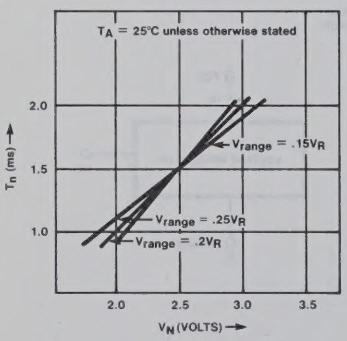
DC ELECTRICAL CHARACTERISTICS

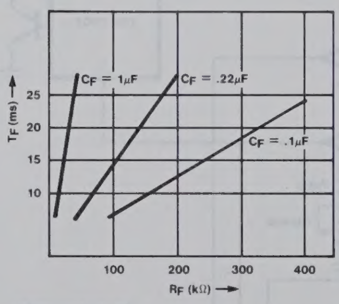
Test conditions T_A = 25°C, V_{CC} = 10V using Test Circuit A unless otherwise stated.

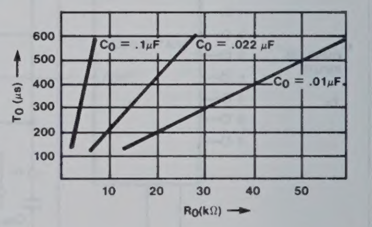
	PARAMETER	TEST CONDITIONS	NE 5044 Min	Typ	Max	UNIT
	POWER SUPPLY REQUIREMENTS[1]					
	Power supply voltage range		4.5		16	V
	Power supply current	Excluding control pots and • serial output currents		11	15	mA
	VOLTAGE REGULATOR					
V_{REG}	Output voltage		4.5	5.0	5.5	V
	Output current	$V_R \geq 4.5V$			−20	mA
	Line regulation	$7 \leq V_{CC} \leq 16$		.005	0.2	V/V
	MULTIPLEXER					
	Input current	$V_n = 2.5v$		±30	±200	nA
	Input voltage range	$V_n - V_{Range} \geq .75V$	1.5		5	V
	Crosstalk			±1	±5	μs
	OUTPUT PULSE					
T_n	Position	$R_I \bullet C_{mux} = 1.25ms$ $V_n = .5V_{REG}$; $V_{RANGE} = .2V_{REG}$	1350	1500	1650	μs
	Position linearity error			5		μs
	Position tempco	$0°C \leq T_A \leq 70°C$.		.15		μs/°C
	Position PSR	$6V \leq V_{CC} \leq 16V$		.5	1	μs/V
T_O	Width	$R_OC_O = 300\mu s$	240	285	330	μs
	Saturation voltage	$I_O = 25mA$		.6	1	V
I_{11}	Leakage current			.05	50	μA
	Range input voltage	$R_I = 50k\Omega$	.75			V
		$R_I = 25k\Omega$	1.00			V
	Frame time (Fixed)	$R_FC_F = 30ms$	17	20	23	ms
	Inhibit threshold				.4	V

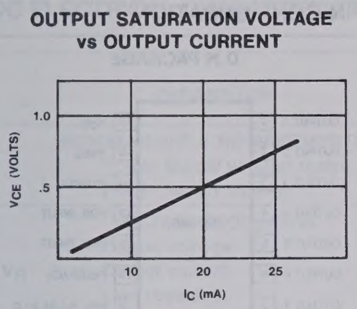
NOTE

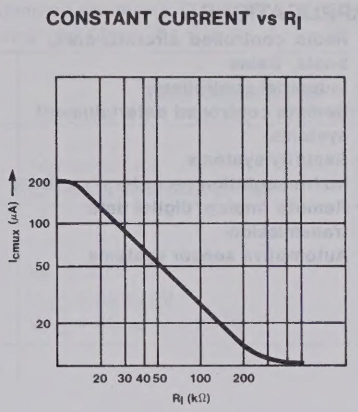
1. At supply voltages exceeding 12 V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended.


OUTPUT PULSE WIDTH (T_n) vs INPUT VOLTAGE (V_n)

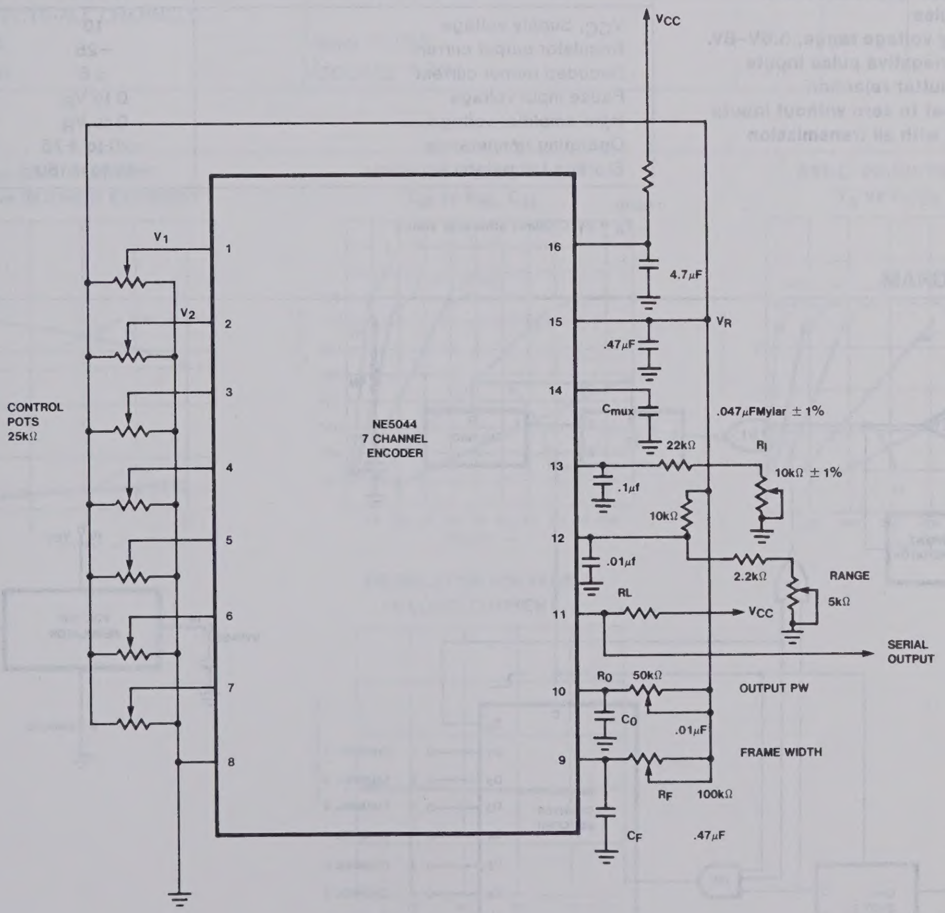

FRAME TIME (T_F) vs R_F


OUTPUT ONESHOT TIME (T_O) vs R_O





TEST CIRCUIT A


VCC
V1
V2
1
2
3
4
5
6
7
8
CONTROL
POTS
25kΩ
NE5044
7 CHANNEL
ENCODER
16
15
14
13
12
11
10
9
4.7μF
VR
.47μF
Cmux
.047μFMylar ± 1%
22kΩ
RI
.1μf
10kΩ ± 1%
10kΩ
.01μf
2.2kΩ
RANGE
5kΩ
RL
VCC
SERIAL
OUTPUT
RO
50kΩ
OUTPUT PW
CO
.01μF
FRAME WIDTH
RF
100kΩ
CF
.47μF

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_W = R_SC_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

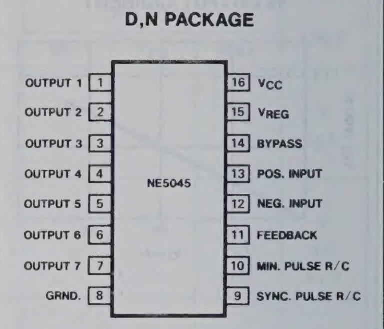
FEATURES

- **Decodes up to 7 channels**
- **High gain input amplifier**
- **Externally set sync. pause and minimum pulse**
- **Wide supply voltage range, 3.6V–8V.**
- **Positive or negative pulse inputs**
- **Noise and flutter rejection**
- **Outputs reset to zero without inputs**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**

PIN CONFIGURATION


D,N PACKAGE
OUTPUT 1 1
OUTPUT 2 2
OUTPUT 3 3
OUTPUT 4 4
OUTPUT 5 5
OUTPUT 6 6
OUTPUT 7 7
GRND. 8
NE5045
16 V_{CC}
15 V_{REG}
14 BYPASS
13 POS. INPUT
12 NEG. INPUT
11 FEEDBACK
10 MIN. PULSE R/C
9 SYNC. PULSE R/C

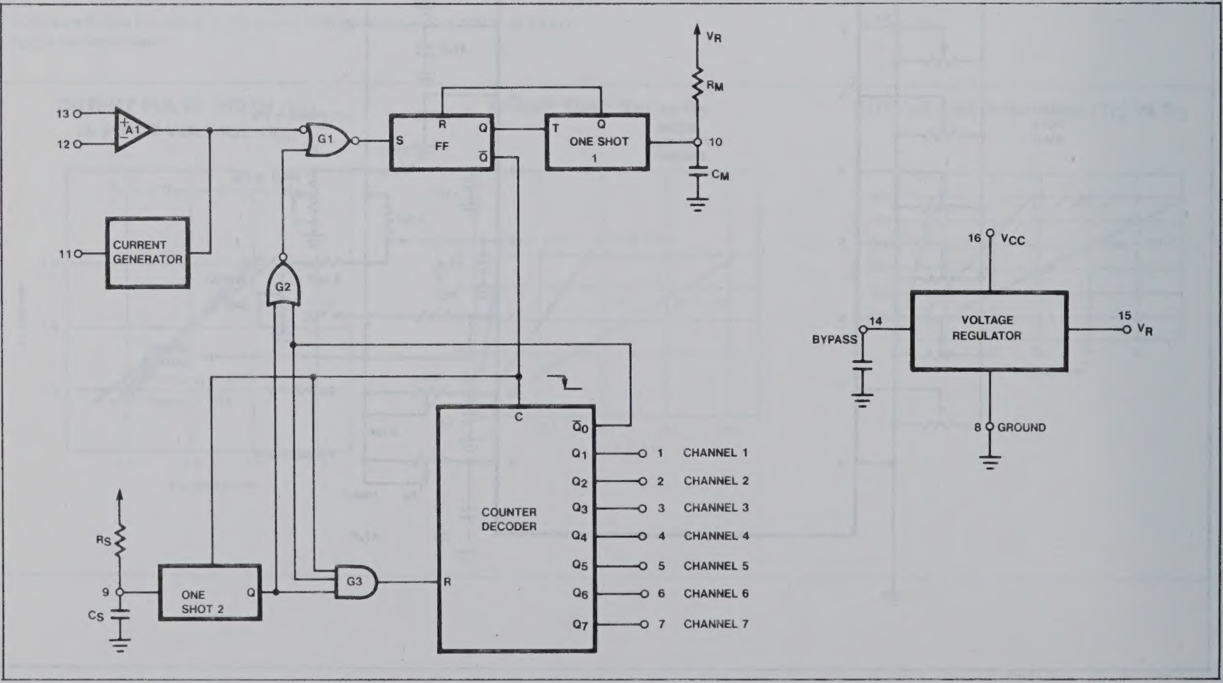
ORDER PART NO.
NE5045N
NE5045D

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	10	V
Regulator output current	−25	mA
Decoded output current	±5	mA
Pause input voltage	0 to V_R	V
Input amplifier voltage	0 to V_R	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE
1. T_A = 25°C unless otherwise stated

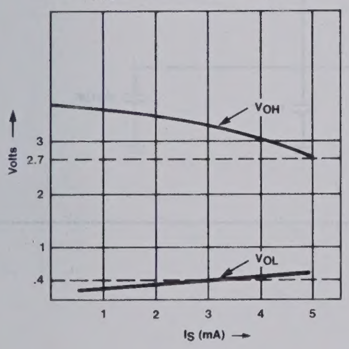
BLOCK DIAGRAM


13
12
A1
11
CURRENT GENERATOR
G1
S
R
FF
Q
$\bar{Q}$
T
Q
ONE SHOT 1
V_R
R_M
10
C_M
G2
C
COUNTER DECODER
$\bar{Q}_0$
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
R
1 CHANNEL 1
2 CHANNEL 2
3 CHANNEL 3
4 CHANNEL 4
5 CHANNEL 5
6 CHANNEL 6
7 CHANNEL 7
R_S
9
C_S
ONE SHOT 2
Q
G3
16 V_{CC}
BYPASS
14
VOLTAGE REGULATOR
15
V_R
8 GROUND

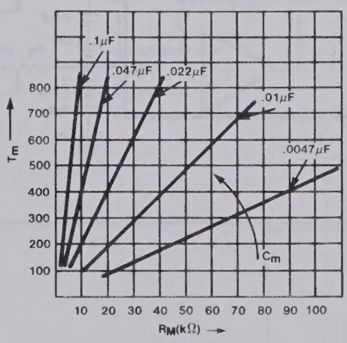
DC ELECTRICAL CHARACTERISTICS

Standard conditions: ($T_A = 25°C$, $V_{CC} = 5.0V$ unless otherwise stated), using Test Circuit #1

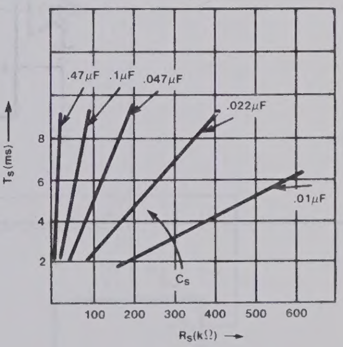
PARAMETER	TEST CONDITIONS	NE5045			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS					
Power supply voltage range	Test circuit #1	3.6		8.0	V
Power supply current	Excluding input bias current		9.0	14.0	mA
VOLTAGE REGULATOR					
Output voltage		3.7	4.1	4.5	V
V_R Output current	$V_R \geq 3.7V$			−15	mA
Line regulation	V_{CC} = 6V to 8V		.01	.05	V/V
Voltage drop	V_{CC} = 4V, I_R = −10mA			1.3	V
INPUT AMPLIFIER					
Input bias current			10	100	nA
Input voltage range		2.0		4.0	V
Open loop gain			60		dB
Feedback current		100	200	400	µA
Detection threshold	Test circuit #1, ΔV12 & 13		8	20	mV
T_S Sync. pause time	$R_s C_s$ = 6.0ms	5.1	6.0	6.9	ms
T_M Minimum pulse time	$R_m C_m$ = 500µs	405	475	545	µs
OUTPUTS-ALL CHANNELS					
V_{OL}	I_{SINK} = 1mA		.25	.5	V
V_{OH}	I_{SOURCE} = 2mA	2.7			V



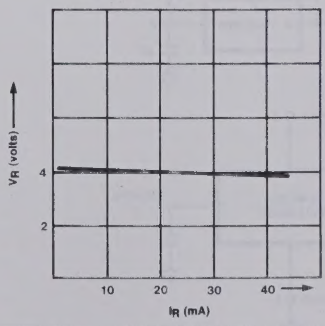
V_{OL} vs SINK CURRENT AND V_{OH} vs SOURCE CURRENT



MINIMUM PULSE TIME, T_M vs R_M, C_M

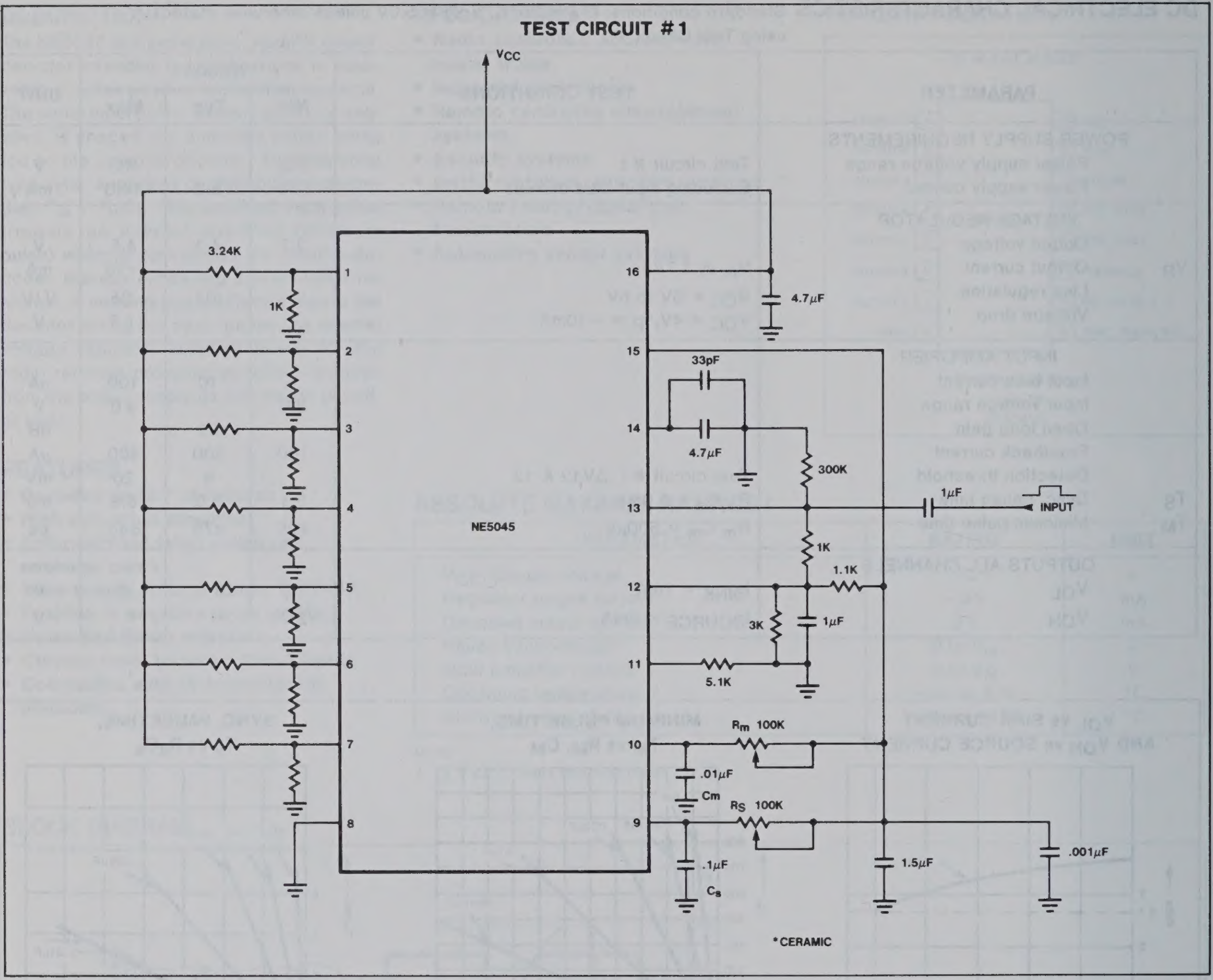


SYNC. PAUSETIME, T_s vs R_sC_s



REGULATOR VOLTAGE vs LOAD CURRENT

TEST CIRCUIT #1


V_CC
3.24K
1K
1
2
3
4
5
6
7
8
NE5045
16
15
14
13
12
11
10
9
4.7µF
33pF
4.7µF
300K
1µF
INPUT
1K
1.1K
3K
1µF
5.1K
R_m 100K
.01µF
C_m
R_S 100K
.1µF
C_s
1.5µF
.001µF
*CERAMIC

NE5046-N

DESCRIPTION

The NE5046 is a serial input parallel output decoder designed for 2 channel digital proportional pulse width or pulse position modulation systems. The detection threshold is internally set and has hysteresis to prevent false triggering on noise. In a typical application, the serial input from the receiver is processed through an amplifier and pulse shaper, then converted to parallel output with a shift register. An internal sync separator detects the sync pause and clears the shift register. An internal voltage regulator provides power for the decoder and can be used to supply power for a radio receiver.

FEATURES

- **High gain input amplifier with hysteresis**
- **Externally adjustable sync separator**
- **Wide supply voltage range 3.6V–8V**
- **Noise and flutter rejection**
- **Outputs reset to zero without input**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio-controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote-controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**

ABSOLUTE MAXIMUM RATINGS[1]

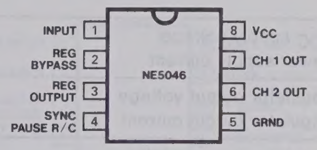
PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	10	V
Regulator output current	−25	mA
Decoded output current	±5	mA
Sync pause input	0 to V_R	V
Input amplifier voltage	0 to V_R	V
Input amplifier current	±1	mA
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE

1. T_A = 25°C unless otherwise stated.

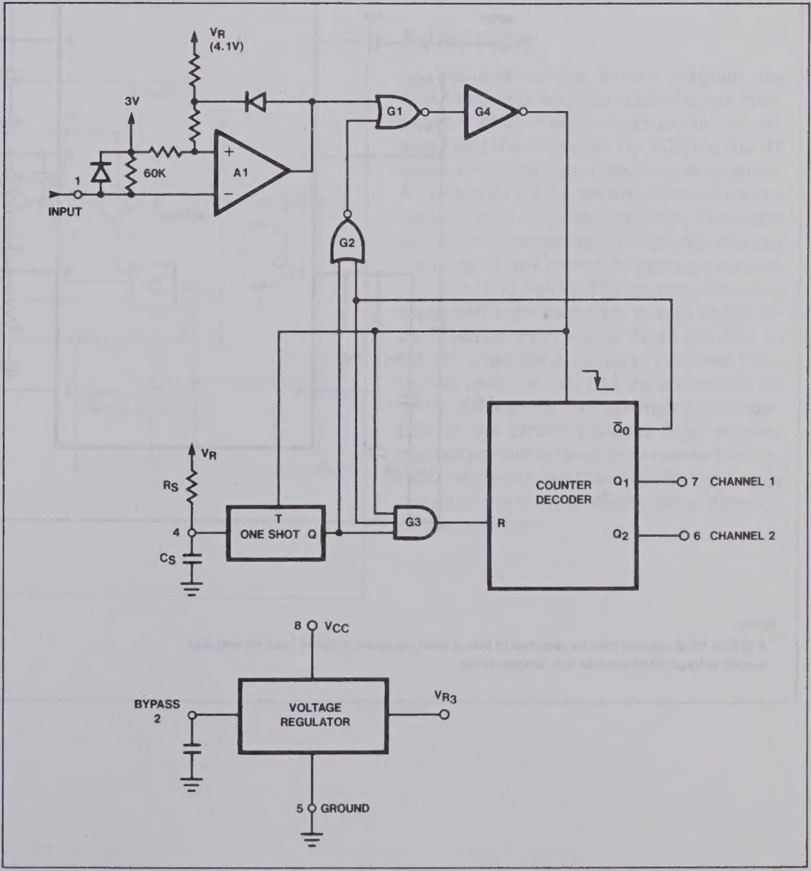
PIN CONFIGURATION

N PACKAGE


INPUT 1
REG BYPASS 2
REG OUTPUT 3
SYNC PAUSE R/C 4
NE5046
8 VCC
7 CH 1 OUT
6 CH 2 OUT
5 GRND

ORDER NE5046N
2 CHANNEL DECODER

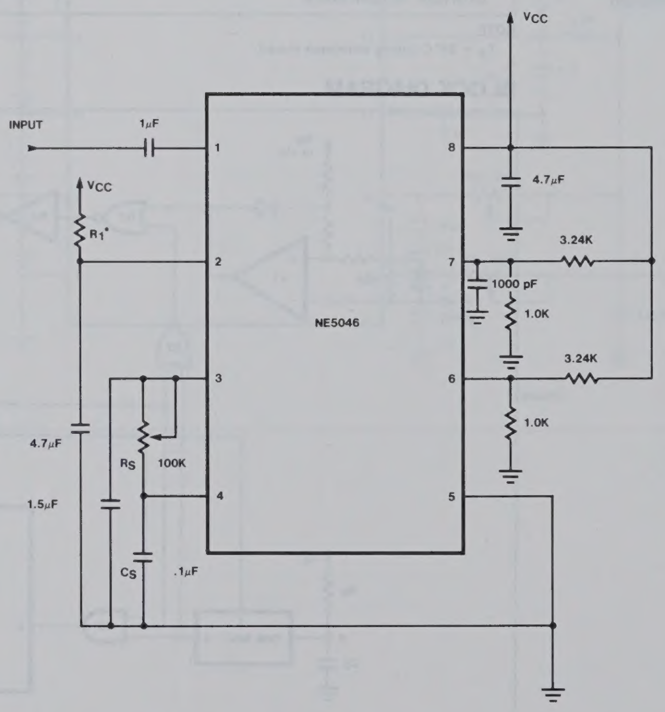
BLOCK DIAGRAM


VR (4.1V)
3V
60K
1
INPUT
A1
G1
G4
G2
VR
RS
4
CS
T
ONE SHOT Q
G3
COUNTER DECODER
R
Q̄0
Q1
Q2
7 CHANNEL 1
6 CHANNEL 2
8 VCC
BYPASS 2
VOLTAGE REGULATOR
VR3
5 GROUND

DC ELECTRICAL CHARACTERISTICS Test Conditions: $T_A = 25°C$, $V_{CC} = 5V$, Test Circuit 1, unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE5046			UNIT
		Min	Typ	Max	
V_{CC} supply voltage		3.6	5.0	8.0	V
Power supply current			6.0	9.0	mA
Regulator output voltage		3.0	4.1	4.5	V
Regulator output current	$V_R \geq 3.6V$			−15	mA
Regulator line regulation	$V_{CC} = 6V$ to $8V$		.01	.05	V/V
Regulator voltage drop	$V_{CC} = 4V$, $I_R = -10mA$			1.0	V
Input threshold voltage		.15			V
Sync. pause time	$R_S C_S = 6ms$	5.1	6.0	6.9	ms
Output voltage both channels			.25		
V_{OL}	$I_{SINK} = 1mA$			.5	V
V_{OH}	$I_{SOURCE} = 2mA$	2.7			V

TEST CIRCUITS


VCC
INPUT
1μF
1
8
4.7μF
VCC
R1*
2
7
3.24K
1000 pF
1.0K
NE5046
3
6
3.24K
1.0K
4.7μF
RS
100K
1.5μF
4
5
CS
.1μF

NOTE

*A 2kΩ to 10kΩ resistor may be required to insure start-up under extreme load current and supply voltage conditions at low temperatures.

AM RECEIVER CIRCUIT TCA440

TCA440-N

DESCRIPTION

TCA440 is a monolithic IC, especially developed for AM receivers up to 30MHz. It includes a RF stage with AGC, a balanced mixer, separate oscillator and an IF amplifier with AGC. Because of its low current consumption and of its internal stabilization the TCA440 is perfectly suited for battery operated portables, car and home radios.

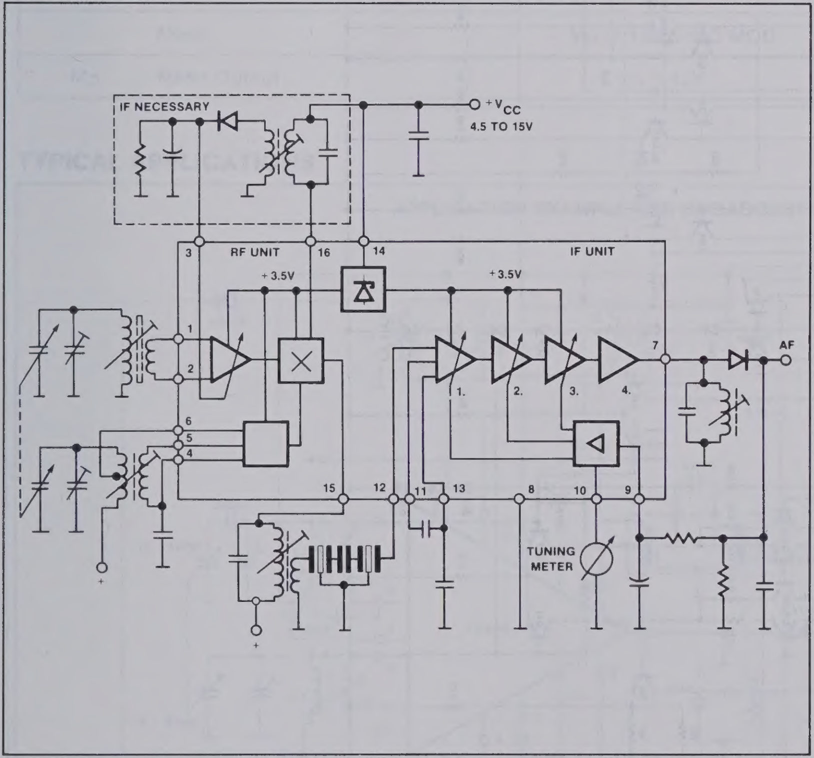
FEATURES

- **Balanced circuit**
- **Separately controllable prestage**
- **Multiplicative push-pull mixer with separate oscillator**
- **High signal handling capability even with 4.5V supply voltage**
- **100dB feedback control range in 5 stages**
- **Direct connection for tuning meter**
- **Minimum external components**

ABSOLUTE MAXIMUM RATINGS

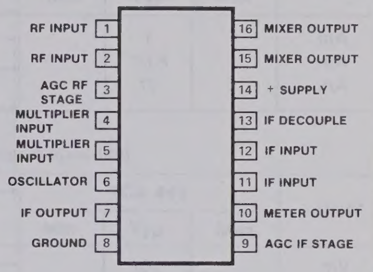
PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	15	V
T_{amb}	Ambient temperature in operation	-15 to +80	°C
T_s	Storage temperature	-30 to +125	°C
V_{CC}	Range of operation	4.5 to 15	V

BLOCK DIAGRAM


IF NECESSARY
+V_{CC}
4.5 TO 15V
3
RF UNIT
16
14
IF UNIT
+3.5V
+3.5V
1
2
6
5
4
1.
2.
3.
4.
7
AF
15
12
11
13
8
10
9
TUNING METER
+
+

PIN CONFIGURATION

N PACKAGE


RF INPUT 1
RF INPUT 2
AGC RF STAGE 3
MULTIPLIER INPUT 4
MULTIPLIER INPUT 5
OSCILLATOR 6
IF OUTPUT 7
GROUND 8
16 MIXER OUTPUT
15 MIXER OUTPUT
14 + SUPPLY
13 IF DECOUPLE
12 IF INPUT
11 IF INPUT
10 METER OUTPUT
9 AGC IF STAGE

ORDER PART NO.
TCA440N

TUNING METER

Recommended instruments:

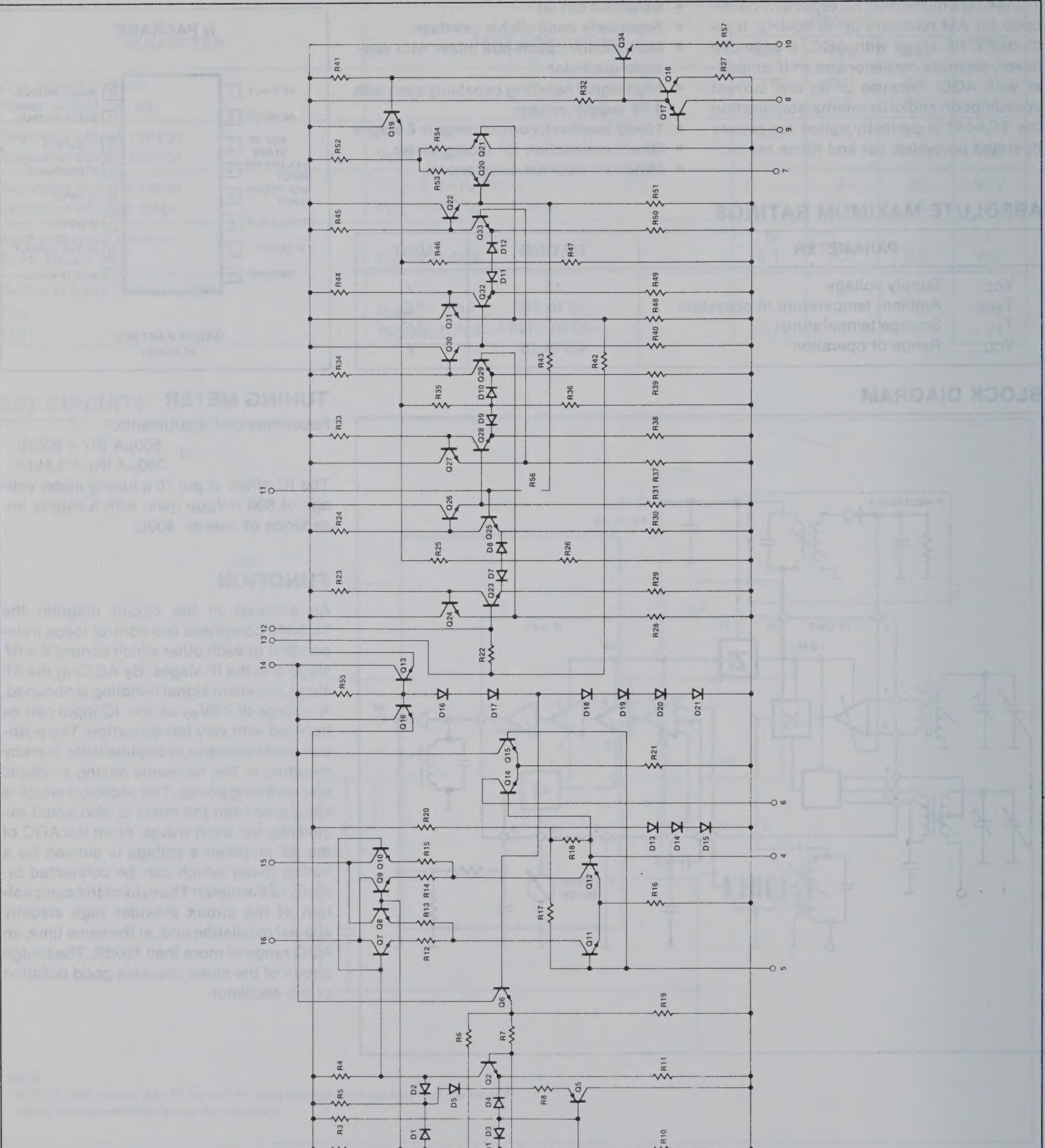
500μA ($R_1 = 800\Omega$)
or 300μA ($R_1 = 1.5k\Omega$)

The IC offers at pin 10 a tuning meter voltage of 600 mV_{EMP} max. with a source impedance of approx. 400Ω.

FUNCTION

As pictured in the circuit diagram the TCA440 comprises two control loops independent of each other which control the RF stage and the IF stages. By AGCing the RF stage, excellent signal handling is obtained. A voltage of 2.6V_{pp} on the IC input can be handled with very low distortion. The push-pull mixer operates multiplicatively, thereby resulting in few harmonic mixing products and whistling points. The oscillator which is separated from the mixer is also apted excellently for short waves. From the AGC of the RF amplifier a voltage is derived for a tuning meter which can be connected directly to the meter. The symmetric composition of the circuit provides high stability against oscillation and, at the same time, an AGC range of more than 100dB. The bridge circuit of the mixer provides good isolation of the oscillator.

EQUIVALENT SCHEMATIC


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
D1
D2
D3
D4
D5
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49
R50
R51
R52
R53
R54
R55
R56
R57

DC ELECTRICAL CHARACTERISTICS V_{CC} = 9V, T_A = 25°C unless otherwise specified.

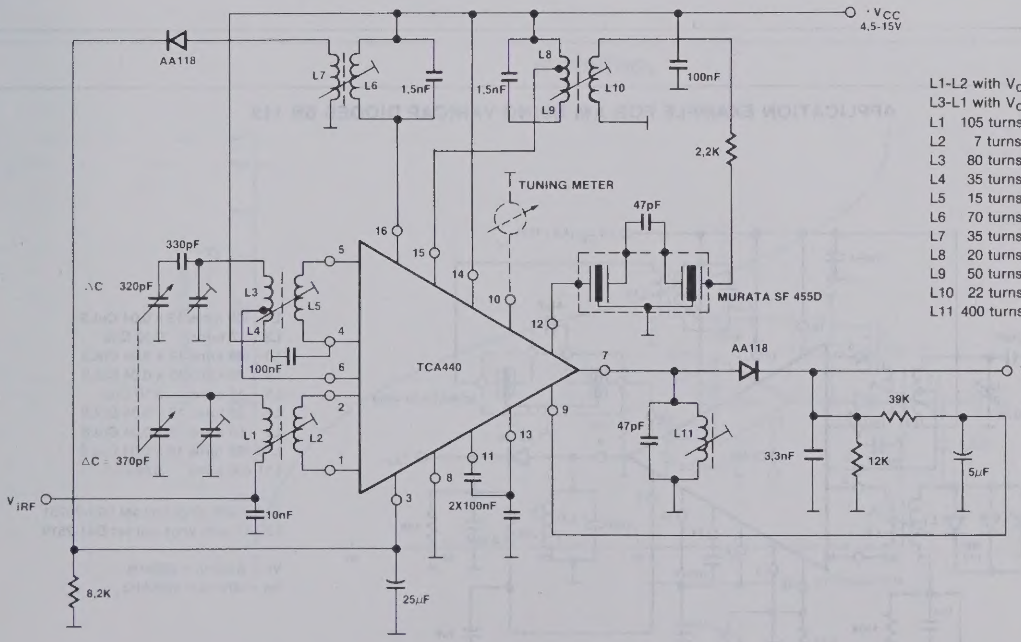
PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
I_{CC}	Total current consumption at:	V_{CC} = 4.5V V_{CC} = 9V V_{CC} = 15V		7 10.5 12		mA mA mA

AC ELECTRICAL TEST V_{CC} = 9V, T_A = 25°C, f_C = 1MHz, f_{MOD} = 1kHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
V_O	Audio output voltage	m = 30% V_{IN} = 1.0mV		100		mV
SEN	Input sensitivity (f_C = 1MHz, m = 30%/0%, R_G = 540Ω)	V_O = 30mV		10		μV
	Noise	V_{IN} = 1.0mV NO MOD.		1.5		mV
M_O	Meter Output	V_{IN} = 4μV		150		μV

TYPICAL APPLICATIONS

APPLICATION EXAMPLE FOR BROADCAST BAND

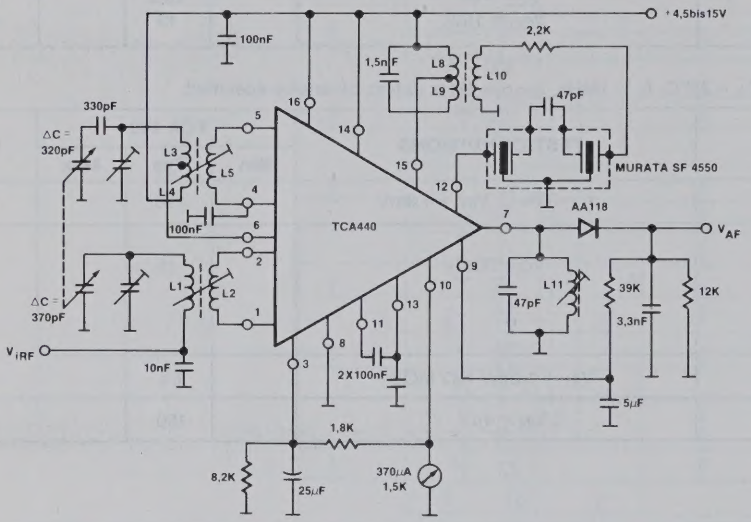

VCC 4.5-15V
AA118
L7
L6
1.5nF
1.5nF
L8
L9
L10
100nF
2,2K
TUNING METER
47pF
MURATA SF 455D
330pF
ΔC 320pF
L3
L4
L5
100nF
ΔC = 370pF
L1
L2
VIRF
10nF
8,2K
16
15
14
10
12
5
4
6
2
1
3
8
11
13
9
7
TCA440
2X100nF
25μF
AA118
VAF
47pF
L11
3,3nF
12K
39K
5μF

L1-L2 with V_{ogt} coil set D21-2375.1
L3-L1 with V_{ogt} coil set D41-2519

L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L6	70 turns	12 x 0.04 CuLS
L7	35 turns	12 x 0.04 CuLS
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.06 CuL

TYPICAL APPLICATIONS (Cont'd)

APPLICATION EXAMPLE FOR BROADCAST BAND

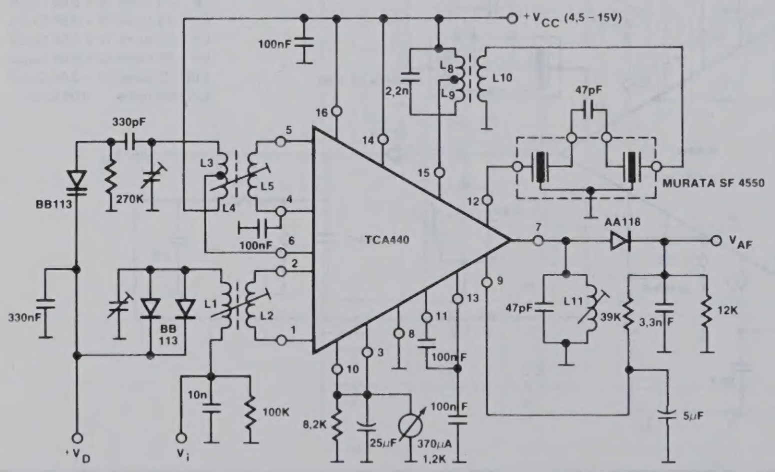

+4,5bis15V
100nF
2,2K
1,5nF
L8
L9
L10
47pF
330pF
ΔC = 320pF
L3
L4
L5
16
14
15
12
5
4
6
2
1
MURATA SF 4550
AA118
7
V_AF
TCA440
100nF
L1
L2
ΔC = 370pF
V_iRF
10nF
9
10
13
11
8
3
2 X 100nF
L11
47pF
39K
12K
3,3nF
5µF
1,8K
8,2K
25µF
370µA 1,5K

Prestage control is derived from IF control

L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.04 CuL

L1-L2 with V_{ogt} coil set D21-23751
L3-L11 with V_{ogt} coil set D41-2519

APPLICATION EXAMPLE FOR AM USING VARICAP DIODES BB 113


+V_CC (4,5 - 15V)
100nF
L8
L9
L10
2,2n
47pF
330pF
16
14
15
12
5
4
6
2
1
L3
L4
L5
BB113
270K
100nF
TCA440
MURATA SF 4550
AA118
7
V_AF
330nF
BB 113
L1
L2
9
13
11
8
3
10
47pF
L11
39K
3,3nF
12K
100nF
10n
100K
8,2K
25µF
370µA 1,2K
100nF
5µF
+V_D
V_i

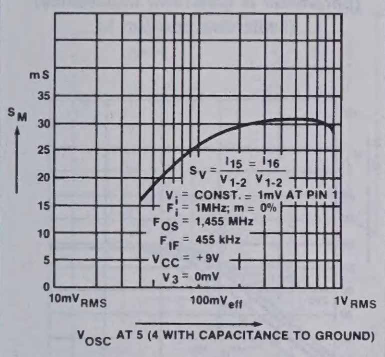
L1	105 turns	12 x 0.04 CuLS
L2	7 turns	0.10 CuL
L3	80 turns	12 x 0.04 CuLS
L4	35 turns	12 x 0.04 CuLS
L5	15 turns	0.10 CuL
L8	20 turns	12 x 0.04 CuLS
L9	50 turns	12 x 0.04 CuLS
L10	22 turns	12 x 0.04 CuLS
L11	400 turns	0.06 CuL

L1-L2 with Vogt coil set D21-23751
L3-L11 with Vogt coil set D41-2519

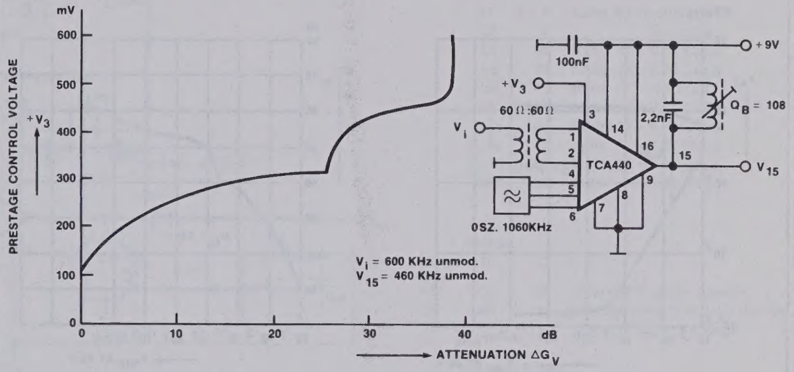
$V_D = 8.5V \rightarrow f_i = 800kHz$
$V_D = 30V \rightarrow f_i = 1620kHz$

TYPICAL APPLICATIONS (Cont'd)

CONVERSION CONDUCTANCE vs OSCILLATOR VOLTAGE

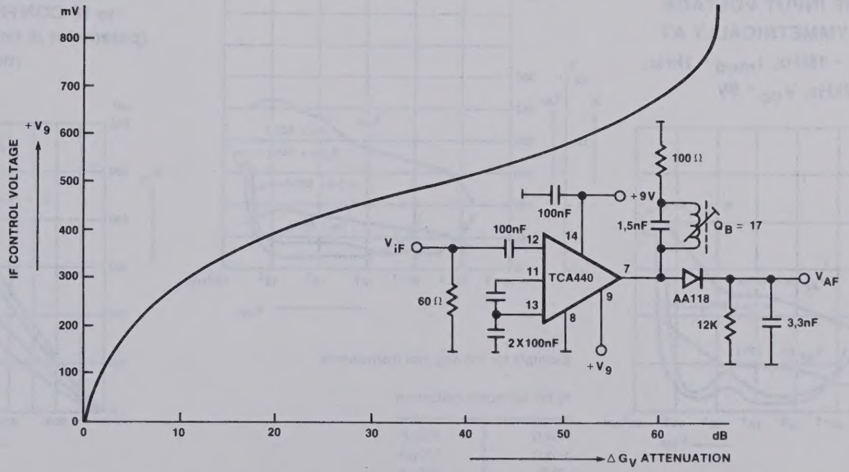


RF STAGE CONTROL



The input is not power matched and can be driven with a higher resistance, V_i is chosen so that a constant V_{15} is obtained (50mV$_{pp}$).

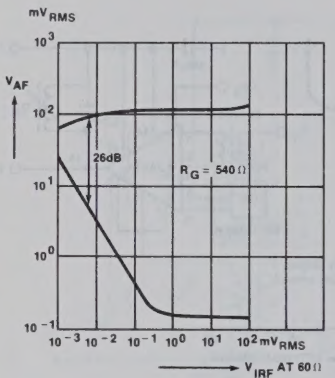
IF CONTROL



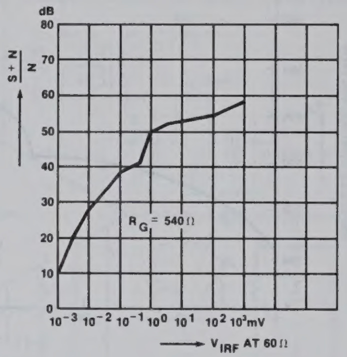
V_{IF} (469kHz; m = 80%; f_{mod} = 1kHz) is chosen so that always a constant V_{AF} is obtained (200mV$_{RMS}$)

TYPICAL PERFORMANCE CHARACTERISTICS

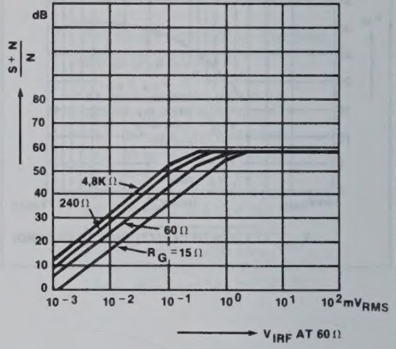
AF OUTPUT VOLTAGE AND NOISE FIGURE vs RF INPUT VOLTAGE
(switching position 1)



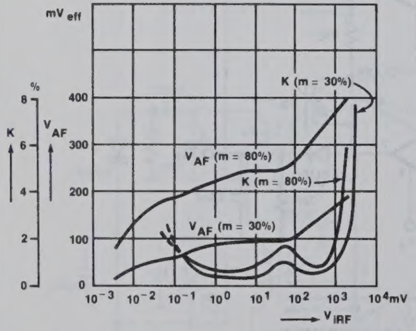
SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE
(switching position 2)



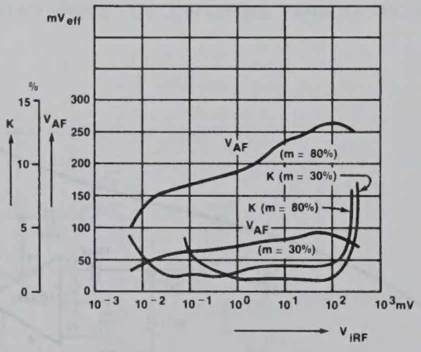
SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE
(parameter is generator impedance)
(switching position 1)



TEST FIGURES FOR APPLICATION EXAMPLE FOR MW HARMONIC DISTORTION AND AF OUTPUT VOLTAGE vs RF INPUT VOLTAGE MEASURED SYMMETRICALLY AT PINS 1 AND 2 f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455kHz, V_{CC} = 9V



TEST FIGURES FOR APPLICATION EXAMPLE FOR AM USING BB 113
f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455 kHz,
V_{CC} = 9V, V_{IRF} measured symmetrically at pins 1 and 2

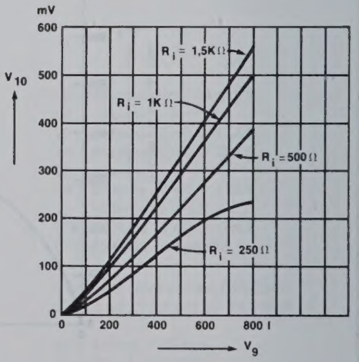


Example for moving coil instruments

R_i for full-scale deflection

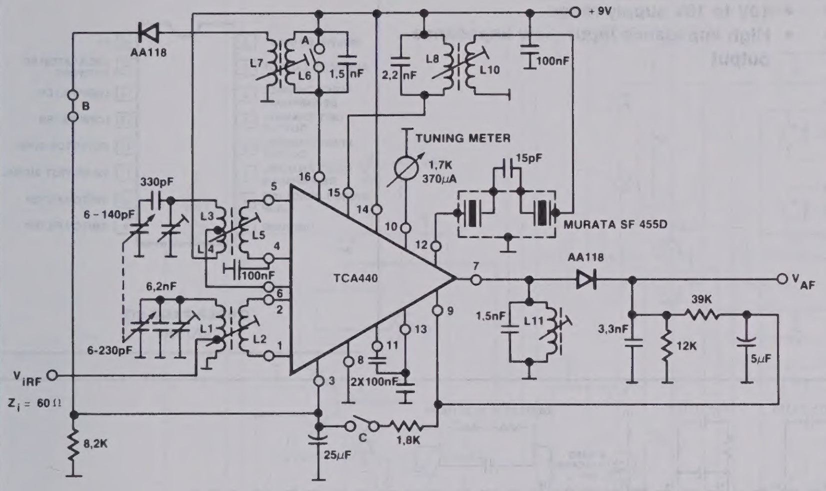
1.5kΩ	100µA
1.5kΩ	170µA
2kΩ	200µA
350Ω	500µA

TUNING METER VOLTAGE vs IF CONTROL VOLTAGE
(parameter is impedance of tuning meter)



TEST CIRCUITS

TEST CIRCUIT FOR NOISE FIGURE


+9V
AA118
B
A
L7
L6
1,5 nF
2,2 nF
L8
L10
100nF
TUNING METER
1,7K
370μA
15pF
MURATA SF 455D
330pF
6 - 140pF
L3
L4
L5
100nF
6,2nF
L1
L2
6-230pF
TCA440
16
15
14
10
12
5
4
6
2
1
7
9
13
11
8
3
2X100nF
AA118
1,5nF
L11
3,3nF
39K
12K
5μF
V_AF
V_IRF
Z_i = 60 Ω
8,2K
C
1,8K
25μF

L1-L2 M25 pot core
L3-L11 with Vogt coil set D41-2519

L1	2 + 6	turns	6 x 12 x 0.04 CuLS
L2	n		0.15 CuL
L3	90	turns	12 x 0.04 CuLS
L4	35	turns	12 x 0.04 CuLS
L5	15	turns	0.10 CuL
L6	70	turns	12 x 0.04 CuLS
L7	35	turns	12 x 0.04 CuLS
L8	60	turns	12 x 0.04 CuLS
L10	22	turns	12 x 0.04 CuLS
L11	68	turns	0.06 CuL

switch			
A	B	C	
off	on	off	separate RF stage control
on	off	on	RF stage control voltage derived from IF control voltage

f_i = 1MHz; m = 30%

n(turns)	$R_{Generator}(\Omega)$
1	15
2	60
4	240
6	540
9	1,2K
12	2,2K
18	4,8K

FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP µA758

µA758-N

DESCRIPTION

The µA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

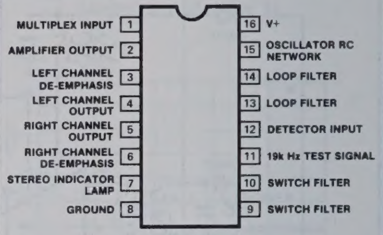
The µA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

FEATURES

- **45dB channel separation**
- **Automatic stereo/mono switching**
- **70dB SCA rejection**
- **10V to 16V supply range**
- **High impedance input—low impedance output**

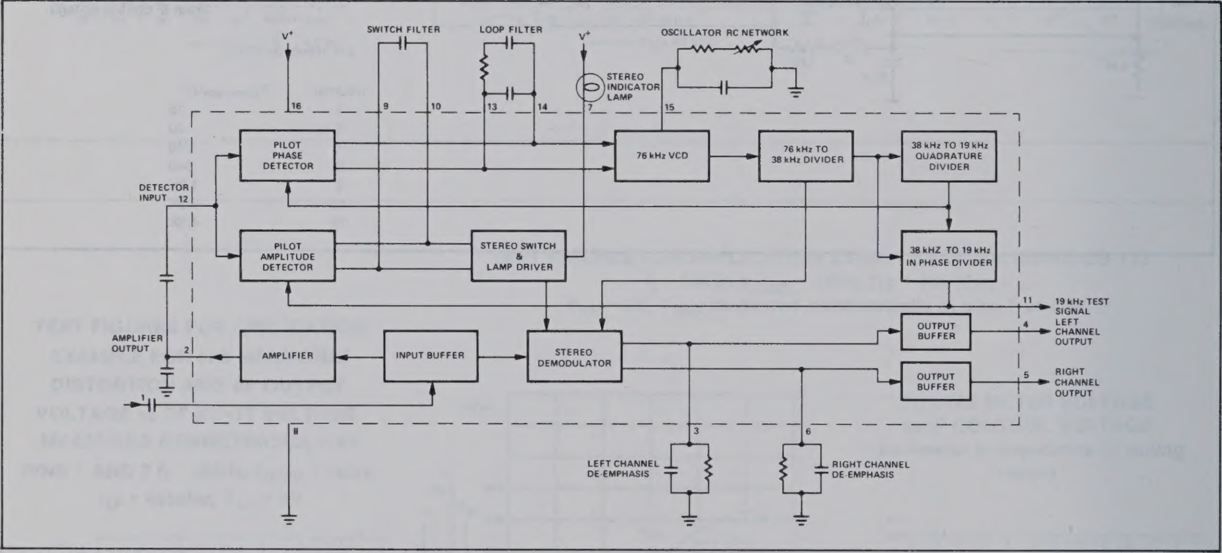
PIN CONFIGURATION

N PACKAGE


MULTIPLEX INPUT 1
AMPLIFIER OUTPUT 2
LEFT CHANNEL DE-EMPHASIS 3
LEFT CHANNEL OUTPUT 4
RIGHT CHANNEL OUTPUT 5
RIGHT CHANNEL DE-EMPHASIS 6
STEREO INDICATOR LAMP 7
GROUND 8
16 V+
15 OSCILLATOR RC NETWORK
14 LOOP FILTER
13 LOOP FILTER
12 DETECTOR INPUT
11 19k Hz TEST SIGNAL
10 SWITCH FILTER
9 SWITCH FILTER

ORDER PART NO.
µA758N

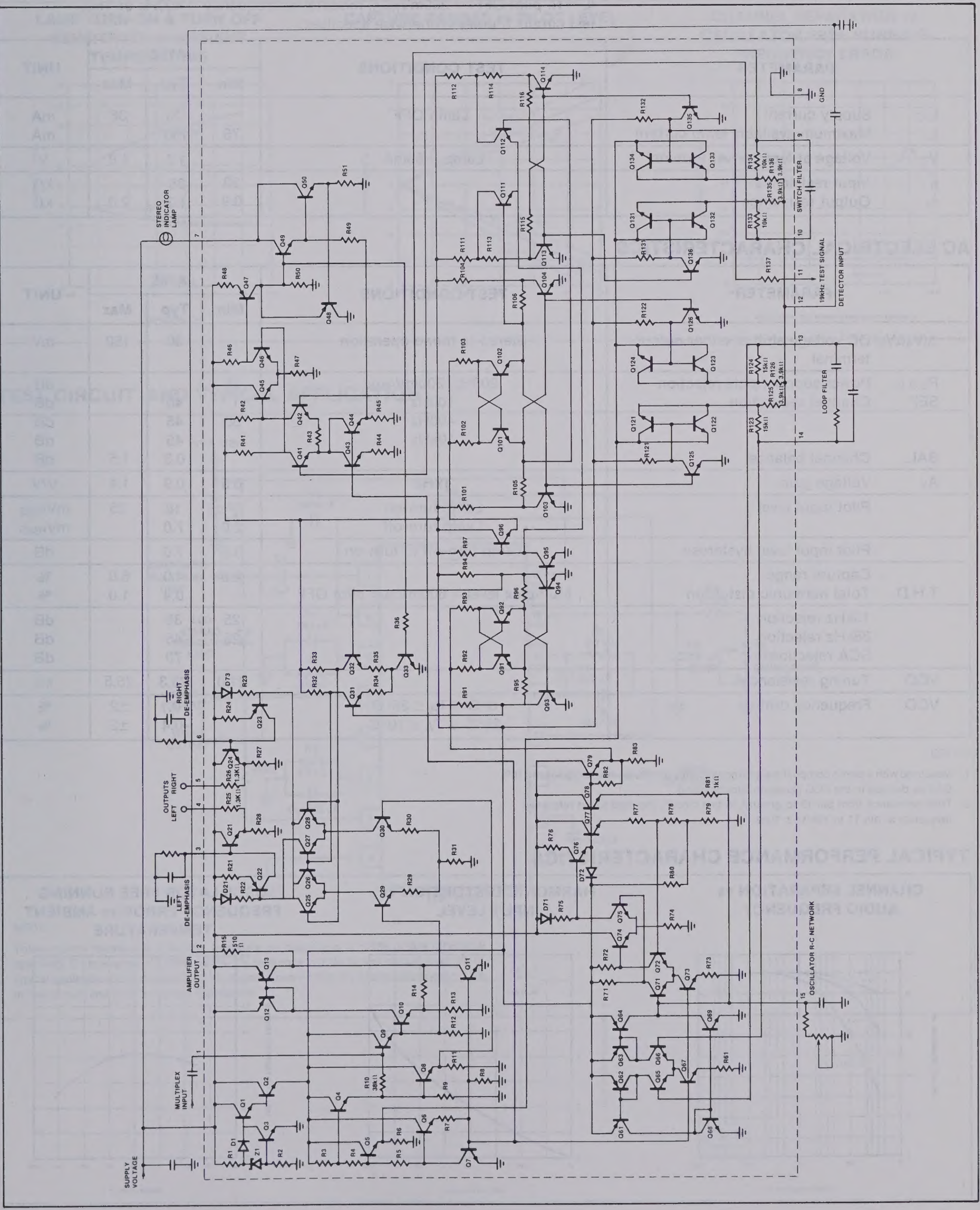
BLOCK DIAGRAM


V+
SWITCH FILTER
LOOP FILTER
V+
OSCILLATOR RC NETWORK
STEREO INDICATOR LAMP
16
9
10
13
14
7
15
PILOT PHASE DETECTOR
76 kHz VCD
76 kHz TO 38 kHz DIVIDER
38 kHz TO 19 kHz QUADRATURE DIVIDER
DETECTOR INPUT 12
PILOT AMPLITUDE DETECTOR
STEREO SWITCH & LAMP DRIVER
38 kHZ TO 19 kHz IN PHASE DIVIDER
11
19 kHz TEST SIGNAL
AMPLIFIER OUTPUT
2
AMPLIFIER
INPUT BUFFER
STEREO DEMODULATOR
OUTPUT BUFFER
4
LEFT CHANNEL OUTPUT
OUTPUT BUFFER
5
RIGHT CHANNEL OUTPUT
1
8
3
6
LEFT CHANNEL DE-EMPHASIS
RIGHT CHANNEL DE-EMPHASIS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+18	V
Supply voltage (≤ 15 seconds)	+22	V
Voltage at lamp driver terminal (Lamp OFF)	+22	V
Internal power dissipation	730	mW
Operating temperature range	-40 to +85	°C
Storage temperature range	-55 to +125	°C
Lead temperature (60sec)	300	°C

EQUIVALENT SCHEMATIC


SUPPLY VOLTAGE
MULTIPLEX INPUT
AMPLIFIER OUTPUT
LEFT DE-EMPHASIS
OUTPUTS LEFT RIGHT
RIGHT DE-EMPHASIS
STEREO INDICATOR LAMP
GND
SWITCH FILTER
19kHz TEST SIGNAL
DETECTOR INPUT
LOOP FILTER
OSCILLATOR R-C NETWORK
R10 38kΩ
R15 510Ω
R25 1.3KΩ
R26 1.3KΩ
R81 1kΩ
R123 15kΩ
R124 15kΩ
R125 3.9kΩ
R126 3.9kΩ
R133 10kΩ
R134 10kΩ
R135 3.9kΩ
R136 3.9kΩ
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V+ = +12V$, 19kHz pilot level = $30mV_{RMS}$, multiplex signal (L = R, pilot OFF) = $300mV_{RMS}$, modulation frequency = 400Hz or 1Hz, test circuit 1, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
I_{CC}	Supply current	Lamp OFF		31	38	mA
I_L	Maximum available lamp current		75	150		mA
V_7	Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
r_i	Input resistance		20	35		kΩ
r_o	Output resistance		0.9	1.3	2.0	kΩ

AC ELECTRICAL CHARACTERISTICS

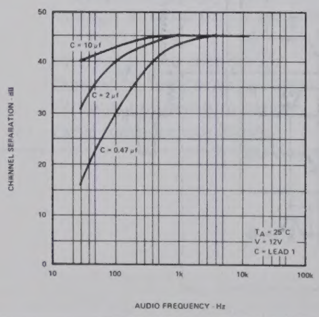
PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
$\Delta(V_4\&V_5)$	DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
$P_{S.R.R.}$	Power supply ripple rejection	200Hz, $200mV_{RMS}$	35			dB
SEP	Channel separation	100Hz		40		dB
		400Hz	30	45		dB
		10kHz		45		dB
BAL.	Channel balance			0.3	1.5	dB
A_V	Voltage gain	1kHz	0.5	0.9	1.4	V/V
	Pilot input level	Lamp turn-on		18	25	mV_{RMS}
		Lamp turn-off	2.0	7.0		mV_{RMS}
	Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
	Capture range		2.0	4.0	6.0	%
T.H.D.	Total harmonic distortion	Multiplex level = $600mV_{RMS}$ pilot OFF		0.4	1.0	%
	19kHz rejection		25	35		dB
	38kHz rejection		25	45		dB
	SCA rejection[1]			70		dB
VCO	Tuning resistance[2]		21.0	23.3	25.5	kΩ
VCO	Frequency drift	$0°C \leq T_A \leq 25°C$		+0.1	±2	%
		$25°C \leq T_A \leq 70°C$		-0.4	±2	%

NOTES

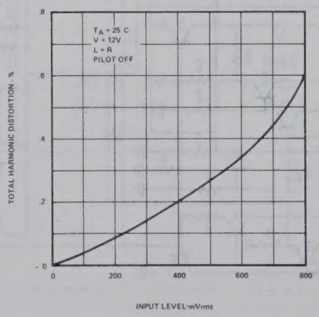
1. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit, required to set reference frequency at pin 11 to 19kHz ± 10hz.

TYPICAL PERFORMANCE CHARACTERISTICS

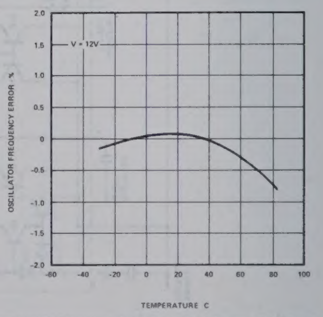
CHANNEL SEPARATION vs AUDIO FREQUENCY



HARMONIC DISTORTION vs INPUT LEVEL

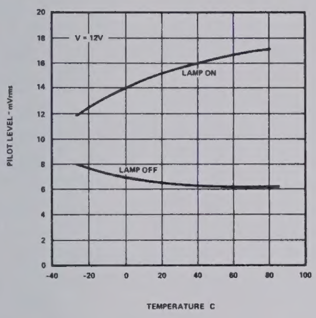


OSCILLATOR FREE RUNNING FREQUENCY ERROR vs AMBIENT TEMPERATURE

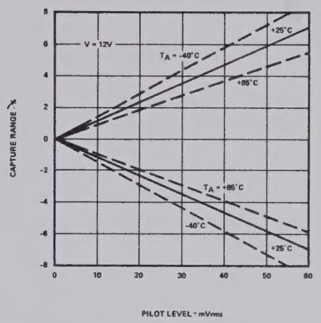


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

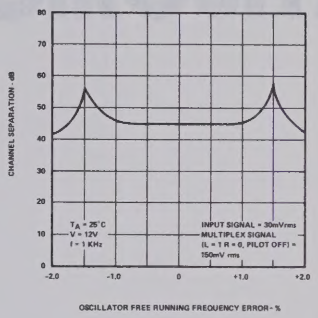
LAMP TURN ON & TURN OFF SENSITIVITY vs AMBIENT TEMPERATURE



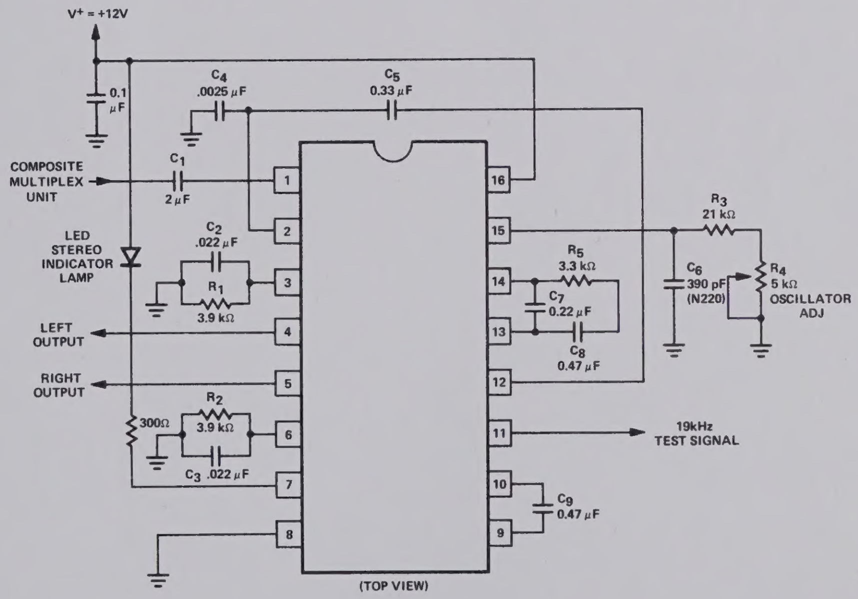
CAPTURE RANGES vs PILOT LEVEL



CHANNEL SEPARATION vs OSCILLATOR FREE RUNNING FREQUENCY ERROR



TEST CIRCUIT AND TYPICAL APPLICATION


V+ = +12V
0.1 μF
C4 .0025 μF
C5 0.33 μF
COMPOSITE MULTIPLEX UNIT
C1 2 μF
LED STEREO INDICATOR LAMP
C2 .022 μF
R1 3.9 kΩ
LEFT OUTPUT
RIGHT OUTPUT
300Ω
R2 3.9 kΩ
C3 .022 μF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
R3 21 kΩ
R5 3.3 kΩ
C6 390 pF (N220)
R4 5 kΩ OSCILLATOR ADJ
C7 0.22 μF
C8 0.47 μF
19kHz TEST SIGNAL
C9 0.47 μF
(TOP VIEW)

NOTE

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified. C_1 tolerance = +100%; -20%, C_6 tolerance = ±1% in test circuit and ±5% in typical applications, R_3 tolerance = ±1%, R_4 tolerance = ±10%, R_1 and R_2 tolerances = ±1% in test circuit and ±5% in typical application.

SECTION 12
TV CIRCUITS

Section 12—TV CIRCUITS

LM1880 Vertical/Horizontal Processor 395
TBA120S 8-Stage Amplifier with Balanced Demodulator 398
TBA1440G/1441G TV Video Amplifier with Demodulator 401
ULN2211 2-Watt TV/FM Sound Channel 405

LM1880-F

DESCRIPTION

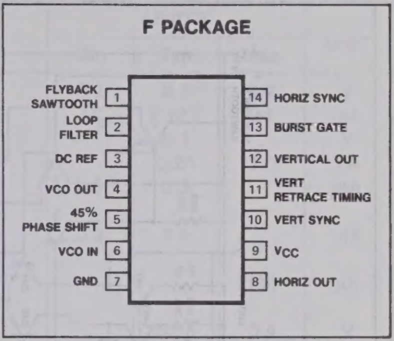
The LM1880 uses compatible Linear/I^{2}L technology to produce the first T.V. horizontal and vertical processing system which completely eliminates the hold controls. The heart of the system is a precision 32 times horizontal frequency VCO which is designed to use a low-cost ceramic resonator as a tuning element.

The VCO signal is divided down in the horizontal section to produce a pre-driver output which is locked to negative sync by means of an on-chip phases detector. The vertical output ramp is injection-locked by vertical sync subject to a sync window derived from the vertical countdown section. A gate pulse centered on the chroma burst is also provided.

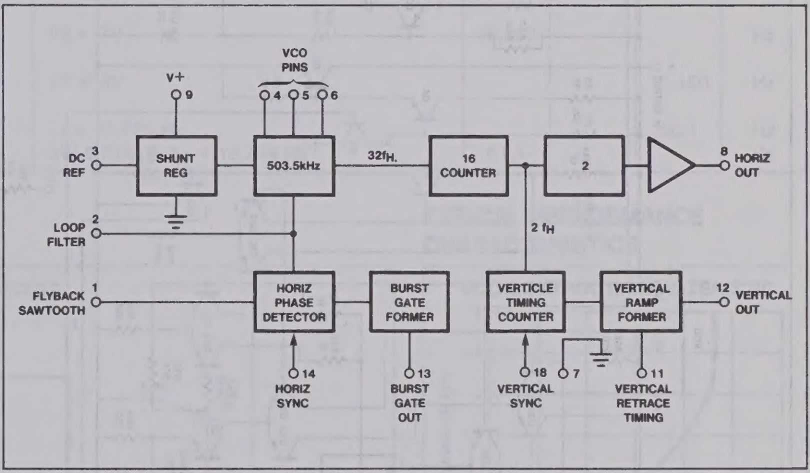
FEATURES

- **No frequency set-up required for horizontal or vertical**
- **Ceramic resonator frequency reference**
- **Accurate horizontal pre-driver duty cycle**
- **Vertical sync window referenced to horizontal**
- **Precise interlaced vertical output**
- **APC loop parameters completely adjustable**
- **Vertical retrace time adjustable**
- **Chroma burst gate output**
- **Internal voltage regulator**

PIN CONFIGURATION


F PACKAGE
FLYBACK SAWTOOTH 1
LOOP FILTER 2
DC REF 3
VCO OUT 4
45% PHASE SHIFT 5
VCO IN 6
GND 7
14 HORIZ SYNC
13 BURST GATE
12 VERTICAL OUT
11 VERT RETRACE TIMING
10 VERT SYNC
9 VCC
8 HORIZ OUT

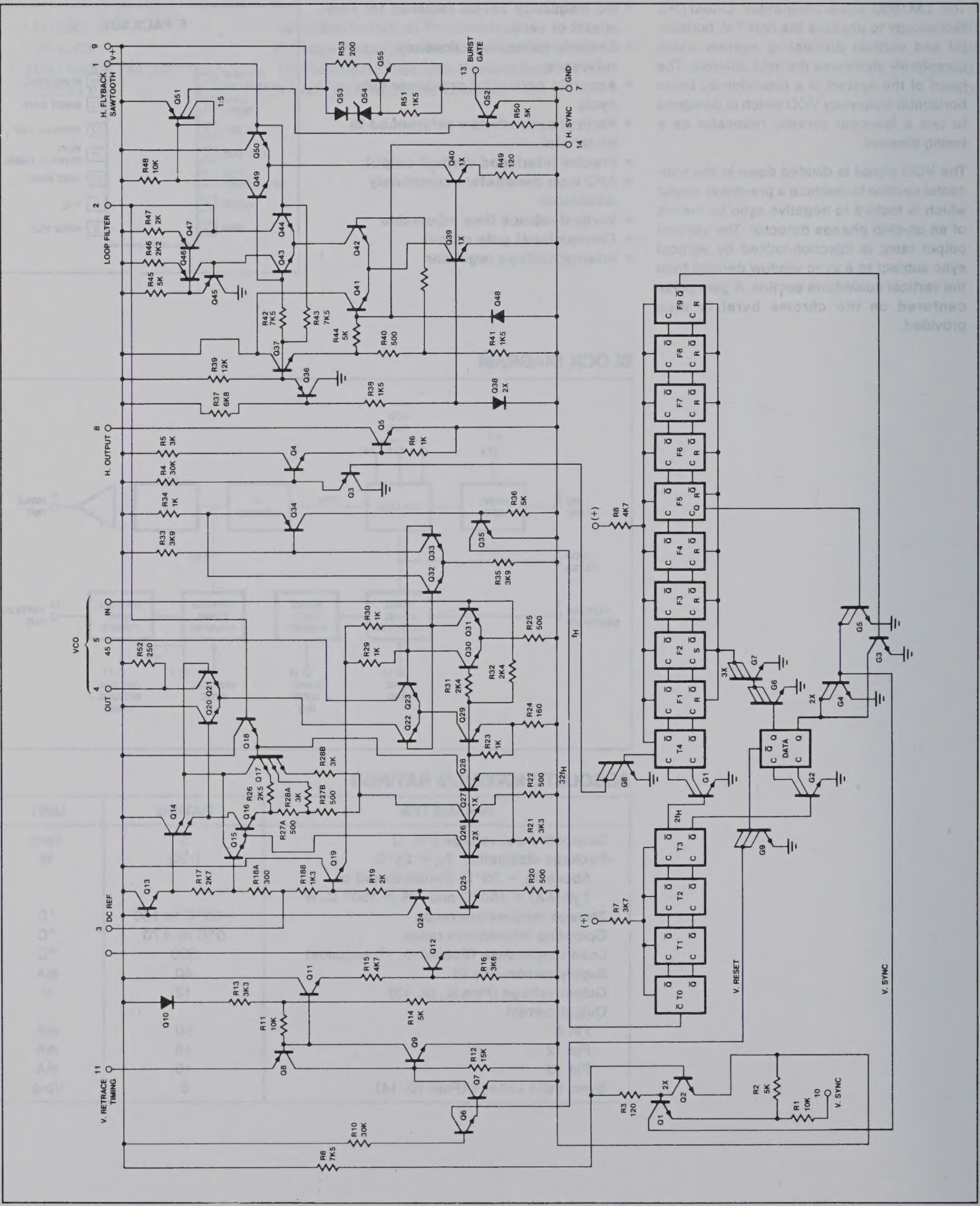
BLOCK DIAGRAM


V+
9
VCO PINS
4
5
6
DC REF 3
SHUNT REG
503.5kHz
32fH.
16 COUNTER
2
8 HORIZ OUT
LOOP FILTER 2
2 fH
FLYBACK SAWTOOTH 1
HORIZ PHASE DETECTOR
BURST GATE FORMER
VERTICLE TIMING COUNTER
VERTICAL RAMP FORMER
12 VERTICAL OUT
14 HORIZ SYNC
13 BURST GATE OUT
18 VERTICAL SYNC
7
11 VERTICAL RETRACE TIMING

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Sawtooth input voltage (Pin 1)	5	Vp-p
Package dissipation, T_A = 25°C	0.83	W
Above T_A = 25°C, Derate Based on T_J(MAX) = 150°C and θJA = 150° C/W		
Storage temperature range	−55°C to 150	°C
Operating temperature range	0°C to +70	°C
Lead temperature (Soldering, 10 seconds)	300	°C
Supply current (Pin 9)	40	mA
Output voltage (Pins 8, 12, 13)	12	V
Output current		
Pin 8	50	mA
Pin 12	15	mA
Pin 13	10	mA
Sync. input voltage (Pins 10, 14)	5	Vp-p

SCHEMATIC DIAGRAM


H. FLYBACK SAWTOOTH 1
V+ 9
LOOP FILTER 2
H. OUTPUT 8
VCO
IN 5
45
OUT 4
DC REF 3
V. RETRACE TIMING 11
BURST GATE 13
GND 7
H. SYNC 14
V. SYNC 10
V. RESET
V. SYNC
1:5
1H
2H
32H
DATA

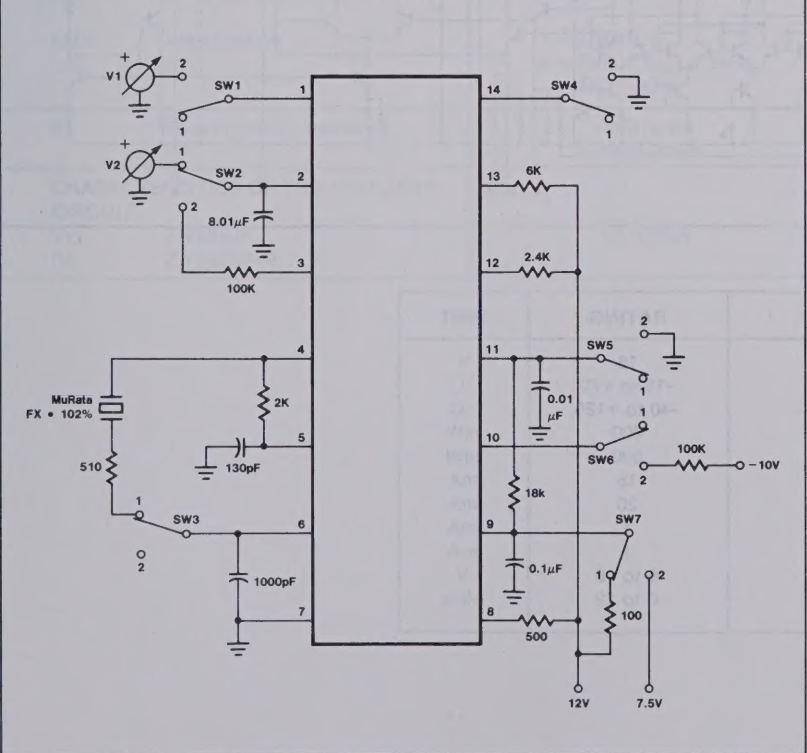
ELECTRICAL CHARACTERISTICS (Test circuit, all SW normally pos. 1, $T_A = 25°C$)

PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Regulated voltage (Pin 9)		8.2	8.7	9.2	V
Supply current (Pin 9)	SW 7 Pos. 2	12	18	24	mA
VCO reference voltage (Pin 3)			5.1		V
VCO control current (Pin 2)	V2 = 5V		0.25	1.0	μA
Horizontal phase detector sink current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 3.9V, V2 =5V	0.3	0.5		mA
Horizontal phase detector source current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 1.9V, V2 = 5V	0.3	0.5		mA
Horizontal output leakage (Pin 8, OFF Condition)	Change SW 3 to Pos. 2 with Pin 8 High			150	μA
Horizontal output saturation voltage (Pin 8, ON condition)	Change SW 3 to Pos. 2 with Pin 8 Low		0.15	0.4	V
Vertical output saturation voltage (Pin 12)	SW 3, SW 5 Pos. 2		0.25	0.5	V
Burst gate saturation voltage (Pin 13)	SW 1, SW 4 Pos. 2, V1 = 1.9V		0.15	0.4	V
Horizontal oscillator free-running Frequency (Pin 8)[1]	SW 2 Pos. 2	15,550	15,750	15,950	Hz
Horizontal oscillator maximum frequency (Pin 8)	V2 = 7V	16,300			Hz
Horizontal oscillator minimum frequency (Pin 8)	V2 = 3V			15,150	Hz
Vertical minimum lock frequency (Pin 12)	f_H = 15,734 Hz			58.1	Hz
Vertical maximum lock frequency (Pin 12)	SW 6 Pos. 2, f_H = 15,734 Hz	61.7			Hz

NOTE

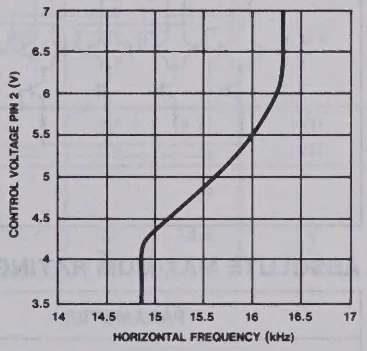
1. Assumes ceramic resonator f_R = 503.48kHz.

TEST CIRCUIT

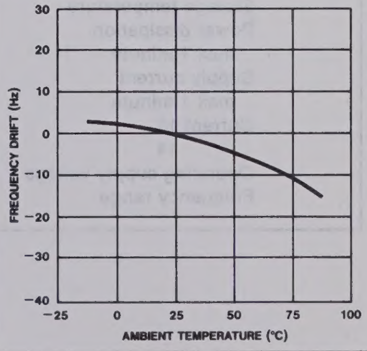

+
V1
2
SW1
1
+
V2
1
SW2
2
8.01μF
100K
1
2
3
4
5
6
7
MuRata
FX • 102%
2K
130pF
510
1
SW3
2
1000pF
14
SW4
2
1
13
6K
12
2.4K
11
SW5
2
1
0.01 μF
10
SW6
1
2
100K
−10V
18k
9
SW7
0.1μF
1
2
8
500
100
12V
7.5V

TYPICAL PERFORMANCE CHARACTERISTICS

VCO CONTROL CHARACTERISTIC



HORIZONTAL FREE-RUNNING FREQUENCY VS TEMPERATURE



8-STAGE AMPLIFIER WITH BALANCED DEMODULATOR TBA120S

TBA120S-N

DESCRIPTION

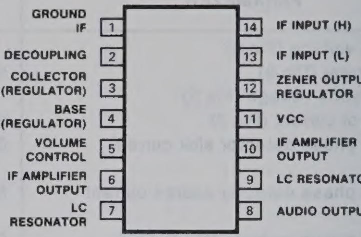
An eight stage amplifier with balanced demodulator for amplifying, limiting and the demodulation of FM signals, specially designed for the sound-IF in TV and RF-IF amplifier in radios. An electronic Volume Control for the audio outputsignal is also provided.

Groups:

TBA120 S is delivered in groups:
An attenuation of −30dB of the audio output signal requires a resistor from pin 5 to ground typ. value 1.8K to 3.4K.

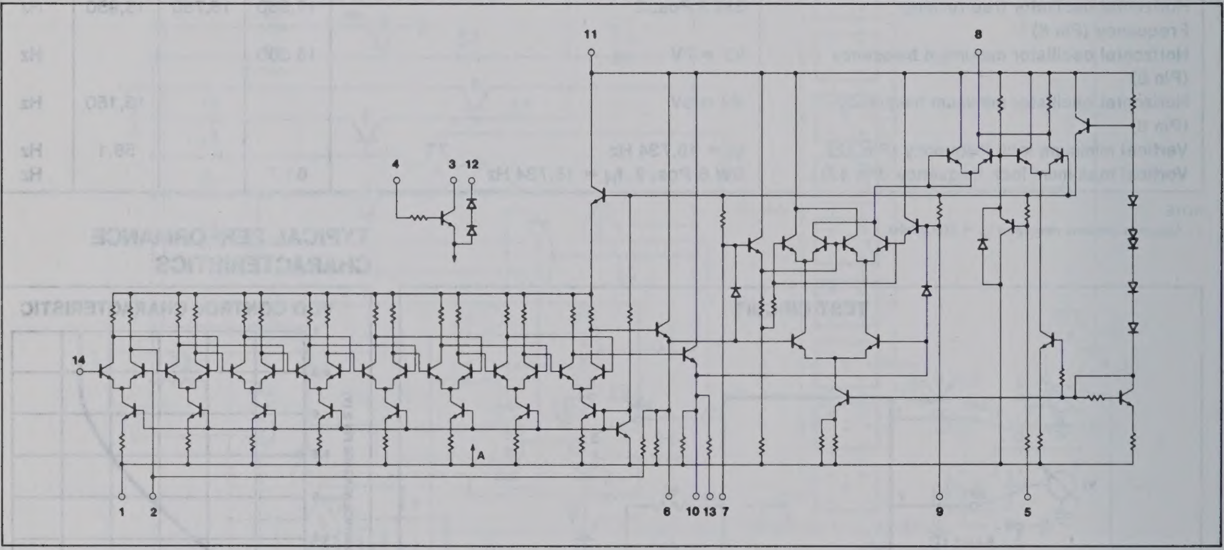
PIN CONFIGURATION

N PACKAGE


GROUND IF
1
DECOUPLING
2
COLLECTOR (REGULATOR)
3
BASE (REGULATOR)
4
VOLUME CONTROL
5
IF AMPLIFIER OUTPUT
6
LC RESONATOR
7
14
IF INPUT (H)
13
IF INPUT (L)
12
ZENER OUTPUT REGULATOR
11
VCC
10
IF AMPLIFIER OUTPUT
9
LC RESONATOR
8
AUDIO OUTPUT

ORDER PART NO.
TBA120SN (DIP),
TBA120ASN (QUAD-IN-LINE)

EQUIVALENT SCHEMATIC


11
8
4
3
12
14
A
1
2
6
10
13
7
9
5

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	18	V
Operating temperature range	-15 to +70	°C
Storage temperature	-40 to +125	°C
Power dissipation	400	mW
max 1 minute	500	mW
Supply current	15	mA
max 1 minute	20	mA
Current 13	1	mA
14	1	mA
Operating supply voltage	6 to 18	V
Frequency range	0 to 12	MHz

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 12V$; $T_{amb} = 25°C$)

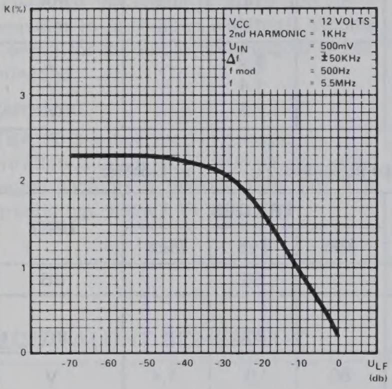
PARAMETER		TEST CONDITIONS	TBA120S			UNIT
			Min	Typ	Max	
I_{CC}	Total current requirement	$R_5 = \infty$		14	24	mA
		$R_5 = 0$		16	26	mA
V_8	dc-portion of the output signal	$V_1 = 0$		8.6		V
V_5	Voltage	-1dB down		2.4		V
		-70dB down		1.3		V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified. $F_C = 4.5$ or 5.5MHz.

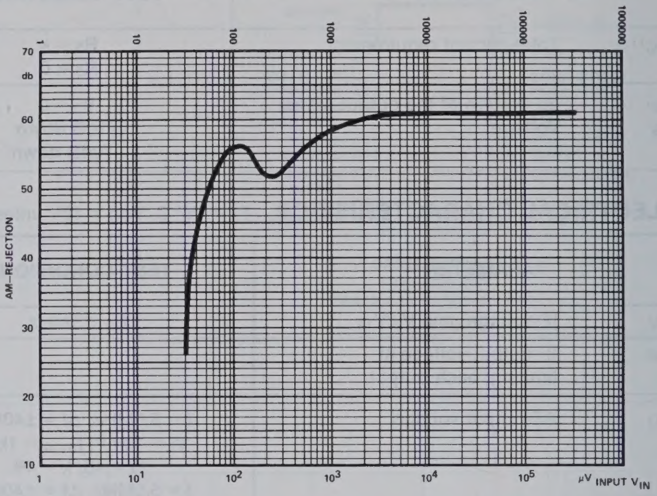
PARAMETER		TEST CONDITIONS	TBA120S			UNIT
			Min	Typ	Max	
A_V	IF-voltage gain V_6/V_{14}	f = 5.5MHz		68		dB
V_{IF}	IF-output voltage at limiting; each output			250		mV
V_O	AF-output voltage	f = 5.5MHz; $\Delta f = \pm 40kHz$; $V_I = 10mV$; $f_{mod} = 1kHz$; Q = 45; k = 4%	.50	.9	1.4	V
		f = 5.5MHz; $\Delta f = \pm 40kHz$; $V_I = 10mV$; $f_{mod} = 1kHz$; Q = 20; k = 1%		500		mV
V_{lim}	Input voltage starting limiting	$V_{out} = -3dB$		30	70	μV
Z_I	Input impedance	f = 5.5MHz		40/4.5		kΩ/pf
R_O	Output resistance	Pin 8		2.6		kΩ
VOL	Range of volume control			70		dB
AMR	AM-rejection	f = 5.5MHz $V_I = 500\mu V$; $f_{mod} = 1kHz$; MO = 30%	40	48		dB
R_5	Potentiometer resistance	-1dB down		3.7	4.7	kΩ
		-70dB down	1.0	1.4		kΩ
CHARACTERISTICS OF THE AUXILIARY CIRCUIT						
V_{12}	Z-voltage	$I_{12} = 5mA$	11.2	12	13.2	V
R_Z	Z-resistance			30		Ω

TYPICAL PERFORMANCE CHARACTERISTICS

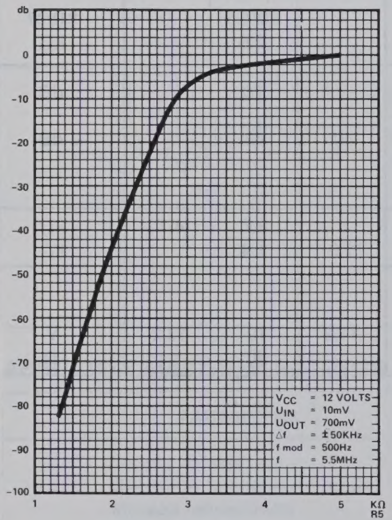
TYPICAL CURVE FROM PRODUCT SELECTION NR3.



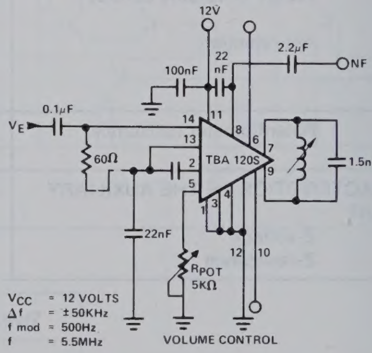
TYPICAL CURVE FROM PRODUCE-REFLECTION NR3.



VOLUME CONTROL SIGNETICS TBA120S



TEST CIRCUIT


12V
2.2μF
22 nF
100nF
NF
0.1μF
V_E
14
11
8
6
7
13
TBA 120S
60Ω
2
9
1.5nF
5
4
3
1
22nF
12
10
R_{POT} 5KΩ
V_{CC} = 12 VOLTS
Δf = ±50KHz
f mod = 500Hz
f = 5.5MHz
VOLUME CONTROL

DESCRIPTION

The TBA1440G (for pnp tuner pre-stages) and TBA 1441G (for npn tuner pre-stages) have been developed from the TBA440P/N. Their improvements are as follows:

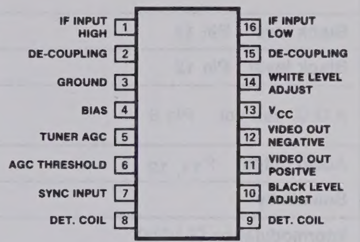
- Reduced residual IF at outputs 11 and 12
- Reduced residual IF at pin 13
- Considerably improved intermodulation distance
- Excellent tuning attitude even with low-ohmic tank circuit at demodulator

The IC's contain a high-amplifying controllable video IF amplifier, a controlled demodulator and two low-resistance video outputs with positive- and negative-going signals as well as the complete keyed control and delayed tuner control.

- Large control range with low noise and wide dynamic range
- High sensitivity
- Controlled demodulator, so minimum 1.07MHz disturbances
- Internal temperature stabilization
- The white levels of the video signals at the positive and negative video output are independent of the operating voltage
- The white and black levels can be adjusted separately

PIN CONFIGURATION

N PACKAGE



ORDER PART NO.

TBA1440G, TBA1441G

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{13}	Supply voltage	15*	V
V_4	Voltages	5	V
V_5		20	V
V_{14}		5	V
R_{8-9}	Ohmic resistance between pins 8 and 9	≤20	Ω
R_{THSA}	Thermal resistance (system-air)	100	K/W
T_J	Junction temperature	150	°C
T_S	Storage temperature	−40 to +125	°C
V_{13}	Supply voltage range	10.5 to 15	V
T_A	Ambient temperature in operation	−25 to +60	°C

NOTE
Briefly 16.5V

DC ELECTRICAL CHARACTERISTICS

$V_{13} = 12.4$, $T_A = 25°C$; all data with reference to ground, unless otherwise specified.

PARAMETER		TEST CONDITIONS	TBA1440G/1441			UNIT
			Min	Typ	Max	
I_{13}	Current consumption	$V_{13} = 15V$	34	47	60	mA
V_{11}	DC voltage at output 11	$V_{IN} = 0$ $R_{14-3} = 68k$ $R_{14-3} = 0$		4.5 6.4		V V
V_{12}	DC voltage at output 12	$V_{IN} = 0$ $R_{14-3} = 68K$ $R_{14-3} = 0$		1.9 3.5		V V
V_6	AGC threshold			2.4		V
V_4	IF control voltage	For max. gain $V_{IN} = 0$ For min. gain $V_{IO} = 0$	 2.5		.5	V V
V_7	Sync input			.7	1.2	V
I_{V5}	AGC leakage				.5	mA
ΔV_{11} ΔV_{12}		$V_{13} = 10.5$ to $15V$		100 50		mV/V mV/V

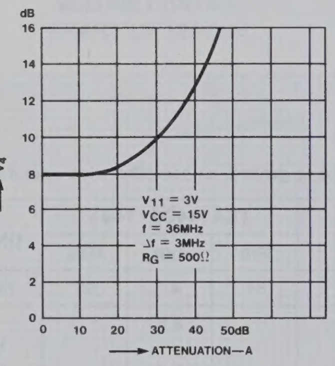
NOTES
1. According to test circuit; V_1 = effective sync pulse level at 60Ω.
2. Test level $a_{cc} = -3dB$
$a_{cc} = -20dB$ referring to picture carrier.

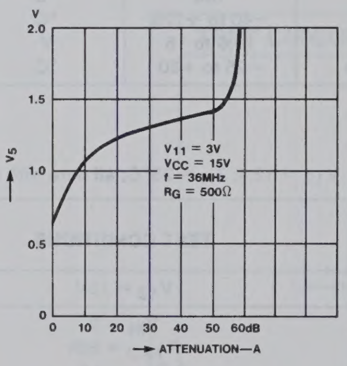
AC ELECTRICAL CHARACTERISTICS $V_{13} = 12.4$; fc = 45 MHz; fm = 1kHz; MOD = 78%

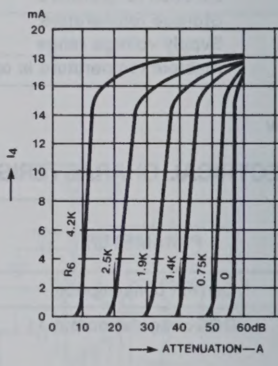
PARAMETER	TEST CONDITIONS	TBA1440G/1441G Min	Typ	Max	UNIT
Black level Pin 11	V_{IN} = 80 mv NO. MOD		.7		V
Black level Pin 12			5.8		V
A.G.C. sat. vol. Pin 5	1440G V_{IN} = 80 mv 1441G V_{IN} = 0		1.3	2.2	V
Audio output $P_{11, 12}$	V_{IN} = 80 mV	3.2	3.8	4.5	V_{PR}
Sensitivity	V_{OUT} – 3DB		240	750	µV
Intermodulation (3 MHz)			45		DB

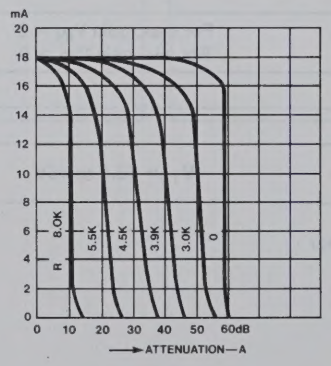
NOTES
1. According to test circuit; V_1 = effective sync pulse level at 60Ω.
2. Test level $a_{cc} = -3dB$
   $a_{cc} = -20dB$ referring to picture carrier.

TYPICAL PERFORMANCE CHARACTERISTICS

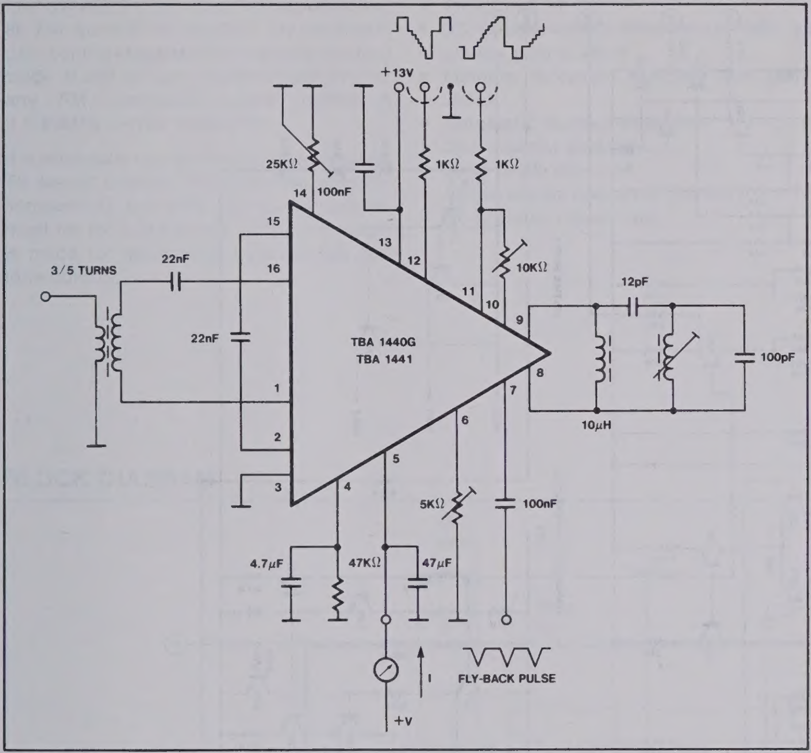

NOISE FIGURE vs ATTENUATION (MEASURED AD VIDEO FREQUENCY) $-V_{fb} = 3V$, $V_{CC} = 15V$, f = 36MHz, Δf = 3MHz, $R_G = 500\Omega$


CONTROL VOLTAGE vs ATTENUATION $-V_{fb} = 3V$, $V_{CC} = 15V$, f = 36MHz, $R_G = 500\Omega$

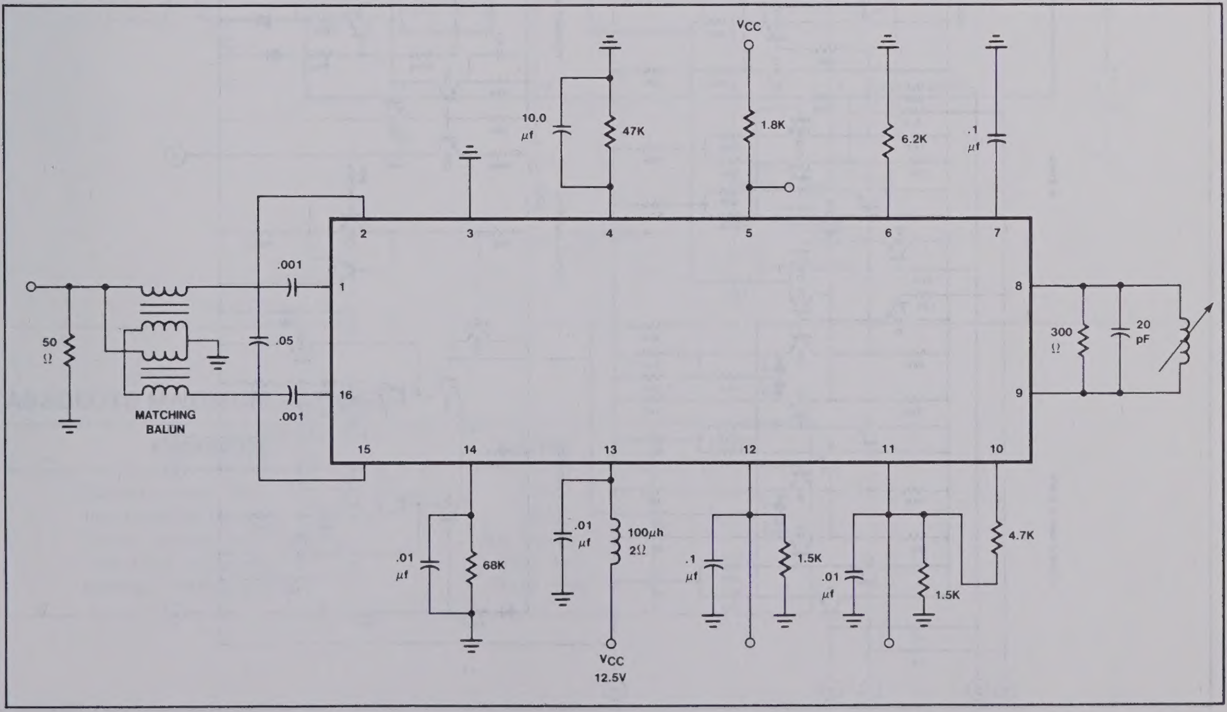

TUNER CONTROL CURRENT vs ATTENUATION R_G = PARAMETER TBA1440G


TUNER CONTROL CURRENT vs ATTENUATION R_G = PARAMETER TBA1441

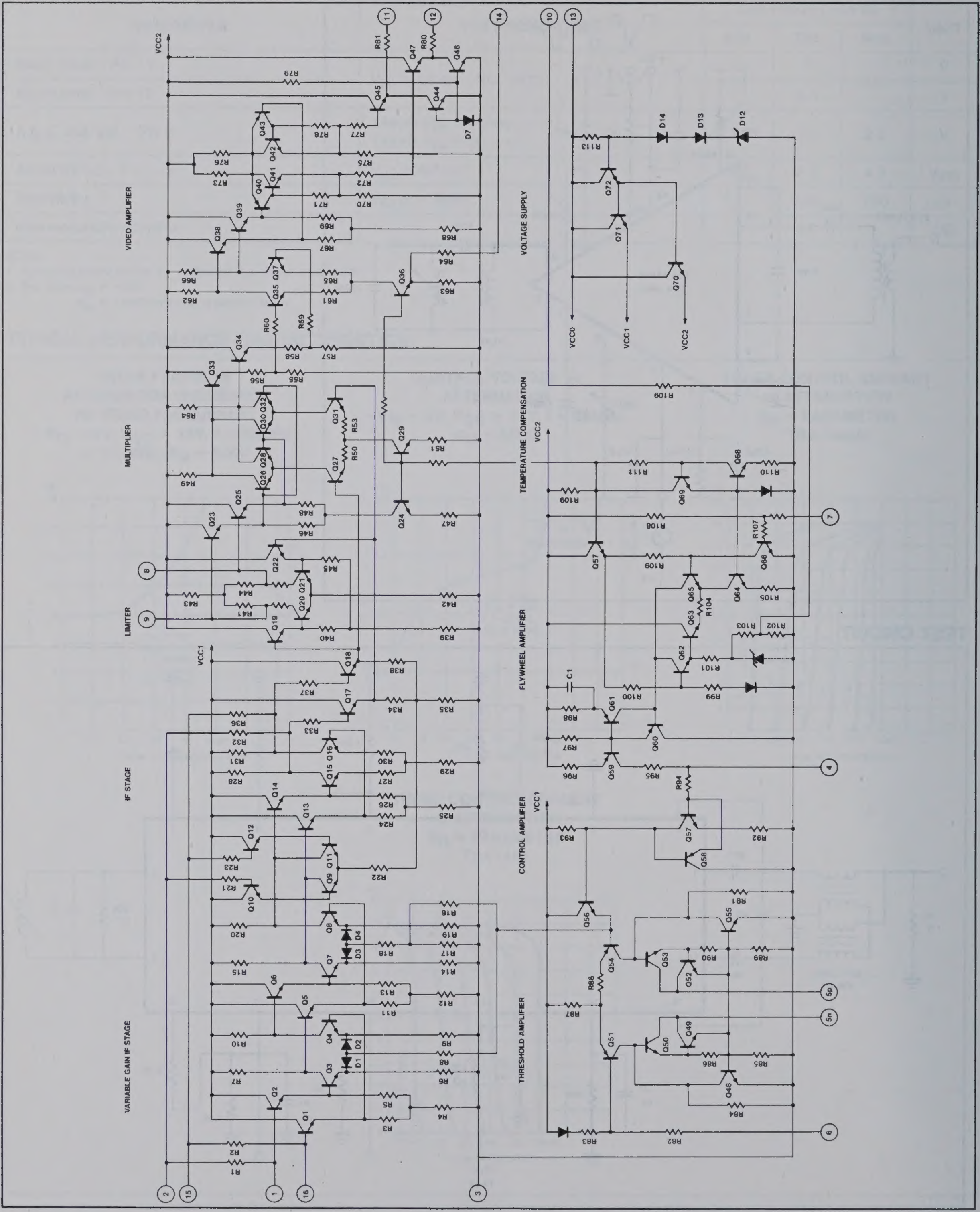
APPLICATION


+13V
25KΩ
100nF
1KΩ
1KΩ
14
15
16
13
12
11
10
9
8
7
6
5
4
3
2
1
3/5 TURNS
22nF
22nF
10KΩ
12pF
TBA 1440G
TBA 1441
100pF
10μH
5KΩ
100nF
4.7μF
47KΩ
47μF
I
FLY-BACK PULSE
+V

TEST CIRCUIT


VCC
10.0 μf
47K
1.8K
6.2K
.1 μf
2
3
4
5
6
7
.001
1
8
50 Ω
.05
300 Ω
20 pF
MATCHING BALUN
.001
16
9
15
14
13
12
11
10
.01 μf
68K
.01 μf
100μh 2Ω
.1 μf
1.5K
.01 μf
1.5K
4.7K
VCC 12.5V

EQUIVALENT SCHEMATIC


VARIABLE GAIN IF STAGE
IF STAGE
LIMITER
MULTIPLIER
VIDEO AMPLIFIER
VOLTAGE SUPPLY
TEMPERATURE COMPENSATION
FLYWHEEL AMPLIFIER
CONTROL AMPLIFIER
THRESHOLD AMPLIFIER
VCC0
VCC1
VCC2
1
2
3
4
5n
5p
6
7
8
9
10
11
12
13
14
15
16

2-WATT TV/FM SOUND CHANNEL ULN2211

ULN2211-N

DESCRIPTION

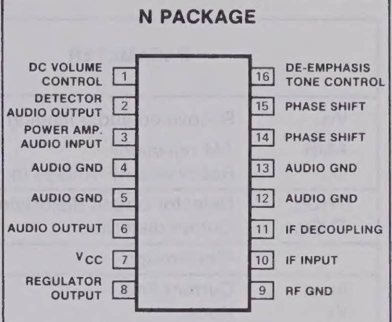
The ULN2211 contains a limiting amplifier, an FM quadrature detector, an electronic gain control stage and a 2-watt audio output stage. It can be used to detect and amplify any FM modulated signal having a 0.1-20MHz carrier frequency.

It is especially recommended as a complete TV sound channel requiring few external components and only one tuning adjustment for the 4.5MHz tank circuit. Provision is made for 6dB/octave de-emphasis and tone control.

FEATURES

- **2-watt output**
- **DC volume control attenuation, 70dB typ**
- **Limiter gain of 70dB**
- **Limiting threshold typically less than 200µV**
- **Automatic thermal shutdown**
- **Over-current limiting**
- **20dB ripple rejection**
- **Single supply operation (18-30V)**
- **No crossover distortion**

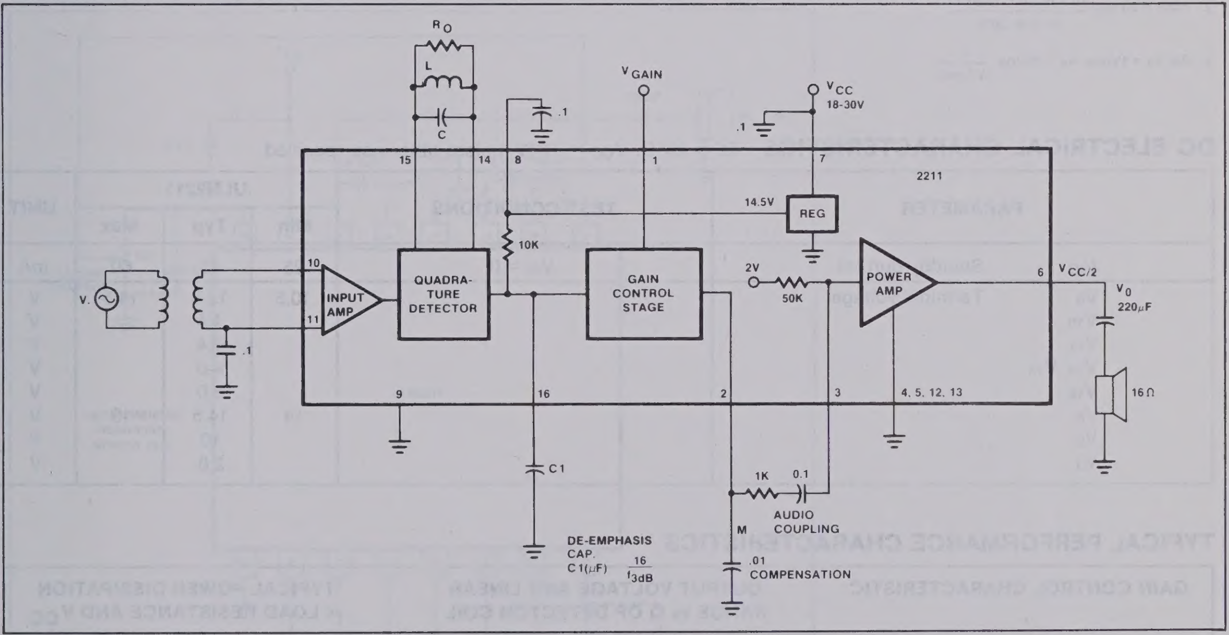
PIN CONFIGURATION


N PACKAGE
DC VOLUME CONTROL 1
DETECTOR AUDIO OUTPUT 2
POWER AMP. AUDIO INPUT 3
AUDIO GND 4
AUDIO GND 5
AUDIO OUTPUT 6
VCC 7
REGULATOR OUTPUT 8
16 DE-EMPHASIS TONE CONTROL
15 PHASE SHIFT
14 PHASE SHIFT
13 AUDIO GND
12 AUDIO GND
11 IF DECOUPLING
10 IF INPUT
9 RF GND

ORDER PART NO.
ULN2211N

NOTE: Internal power dissipation in watts.

BLOCK DIAGRAM


R O
L
C
.1
V GAIN
V CC
18-30V
.1
15
14
8
1
7
2211
14.5V
REG
10K
10
11
V.
.1
INPUT AMP
QUADRA-TURE DETECTOR
GAIN CONTROL STAGE
2V
50K
POWER AMP
6
V CC/2
V o
220µF
16 Ω
9
16
2
3
4, 5, 12, 13
C 1
1K
0.1
AUDIO COUPLING
M
DE-EMPHASIS CAP.
C 1(µF) 16/f3dB
.01
COMPENSATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	+30	V
Input voltage (pin 10)	+4.0	Vrms
Power consumption (internal)	See Figure 1	
Operating temperature	-25 to +70	°C
Storage temperature	-65 to +150	°C

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +24V; f_o = 4.5MHz, Δf = 25kHz, f_m = 400Hz unless otherwise specified.

PARAMETER		TEST CONDITIONS	ULN2211			UNIT
			Min	Typ	Max	
V_{TH}	Recovered audio limiting threshold[1]	Adjust V_1 for $V_O = 5.6V$ ($P_O = 2W$)		150	350	µV
AMR	AM rejection[2]	Adjust V_1 for 2W, $V_{IN} = 10mV$	30	55		dB
V_O	Recovered AF voltage (pin 16)	$V_{IN} = 10mV$, f = 25kHz	500	800		mVrms
THD_D	Detector output distortion	$V_{IN} = 10mV$, f = 25kHz		1.0	2.0	%
THD_O	Output distortion	$P_O = 2W$, $R_L = 16$		2	10	%
	Playthrough	$V_1 = 0$		10	15	mVrms
I_{MAX}	Current limit	$R_L = 0$		800		mA
V_N	Noise	$V_{IN} = 0$, $V_1 = +8V$		15	25	mVrms
A_V	Power AMP voltage gain[3]		25	27	29	dB
V_O/V_{CC}	Output tracking (V_6/V_7)	V_{CC} = 18 to 27V		0.5		V/V
Z_{IN}	Audio amp input impedance	f = 1kHz	40	50	60	kΩ

NOTES

1. Measured with output at -3dB, reference V_{IN} = 10mV, Δf = 25kHz
2. AMR = 20 log $\frac{V_0 \text{ (FM, } \Delta f = 7.5\text{kHz)}}{V_0 \text{ (AM, 30\%)}}$
3. Set V_0 = 1Vrms. A_V = 20 log $\frac{1}{(V3\text{rms})}$

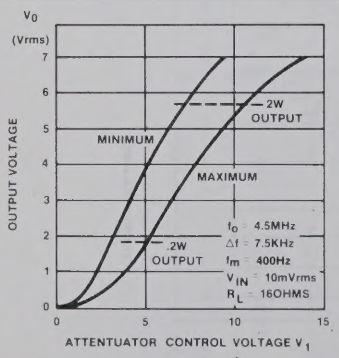
DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +24V unless otherwise specified.

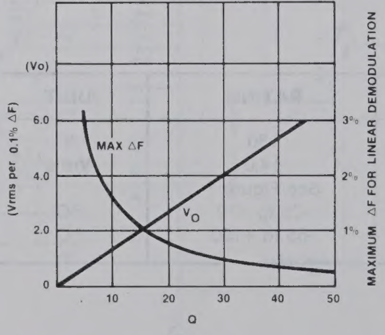
PARAMETER		TEST CONDITIONS	ULN2211			UNIT
			Min	Typ	Max	
I_{CC}	Standby current	$V_{IN} = 0$	25	45	60	mA
V_6	Terminal voltage		10.5	12.5	14.5	V
V_{10}				1.4		V
V_{11}				1.4		V
V_{14}, V_{15}				4.0		V
V_{16}				8.0		V
V_8			14	14.5	16	V
V_2				10		V
V_3				2.6		V

TYPICAL PERFORMANCE CHARACTERISTICS

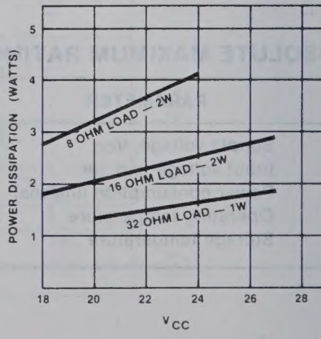
GAIN CONTROL CHARACTERISTIC



OUTPUT VOLTAGE AND LINEAR RANGE vs Q OF DETECTOR COIL



TYPICAL POWER DISSIPATION vs LOAD RESISTANCE AND V_{CC}



ULN2211-N

MAXIMUM ALLOWABLE POWER DISSIPATION

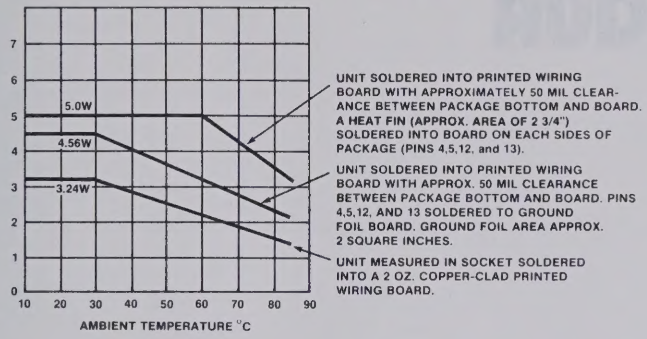


Figure 1

TYPICAL APPLICATION

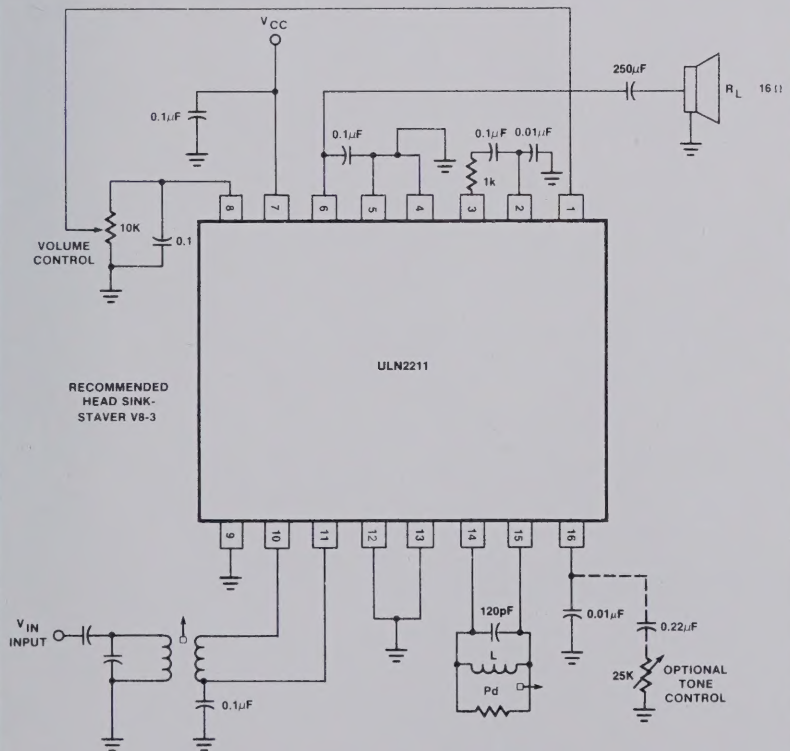

V_{CC}
250μF
R_L 16Ω
0.1μF
0.1μF
0.1μF 0.01μF
1k
10K
0.1
VOLUME CONTROL
8 7 6 5 4 3 2 1
ULN2211
RECOMMENDED HEAD SINK-STAVER V8-3
9 10 11 12 13 14 15 16
V_{IN} INPUT
120pF
L
Pd
0.01μF
0.22μF
25K
OPTIONAL TONE CONTROL
0.1μF

Table 1

f_o	L	R_D
4.5mHz	10-14μH	∞
10./mHz	1-3μH	5K

Figure 2

SECTION 13
AUDIO CIRCUITS

Section 13—AUDIO CIRCUITS

LM387 Dual Low-Noise Preamp 411
NE/SE540 Power Driver 415
NE542 Dual Low Noise Preamp 420
NE545* Dolby Noise Reduction Processor ....
NE570/571/SA571 Compandor 423
NE572 Programmable Analog Compandor 425
NE645B/646B-N Dolby Noise Reduction Processor 427

NEW PRODUCT

SD5340 4-Input/2-Output Audio Source Selector—Available 2nd Quarter 1981

NOTE
*This data sheet may be obtained by writing Publication Services at Signetics,
811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-2111.

DUAL LOW-NOISE PREAMP LM387

LM387-N

DESCRIPTION

The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110dB supply rejection and 60dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} - 2V p-p), and wide power bandwidth (75kHz, 20V p-p). The LM387 operates from a single supply across the wide range of 9 to 40V.

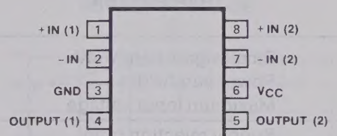
The amplifiers are internally compensated for all gains greater than 10. The LM387 is available in an 8 lead dual-in-line package.

FEATURES

- **Low noise—0.8μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 40V**
- **Power supply rejection—110dB**
- **Large output voltage swing (VCC - 2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 75kHz, 20V p-p**
- **Internally compensated**
- **Short circuit protected**

PIN CONFIGURATION

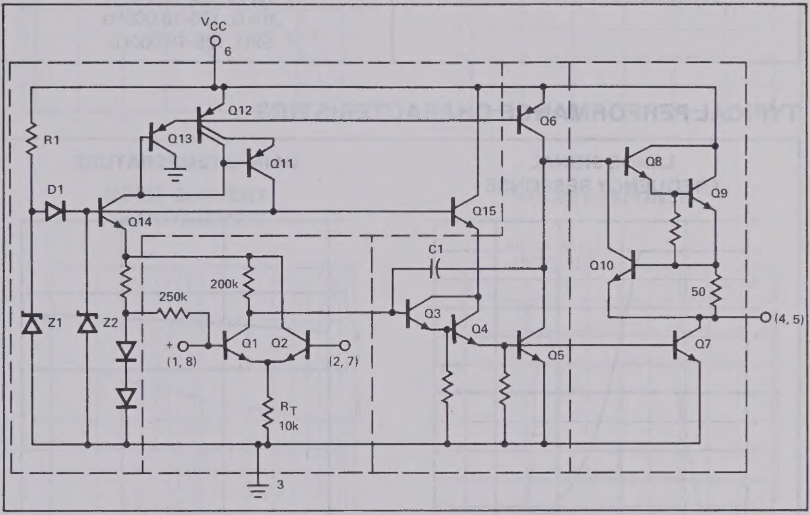
N PACKAGE



ORDER PART NO.

LM387N

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

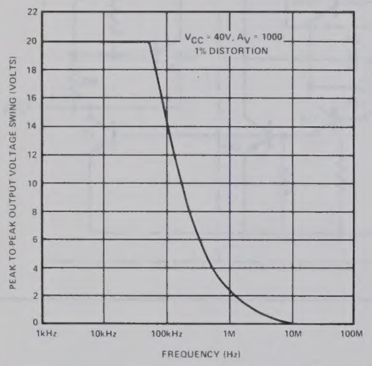
PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Supply current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input resistance	Positive input		100		kΩ
	Negative input		200		kΩ
Input current	Negative input		0.5		μA
Output resistance	Open loop		150		Ω
Output current	Source		8		mA
	Sink		2		mA
Output voltage swing	Peak-to-peak		V_{CC}-2		V

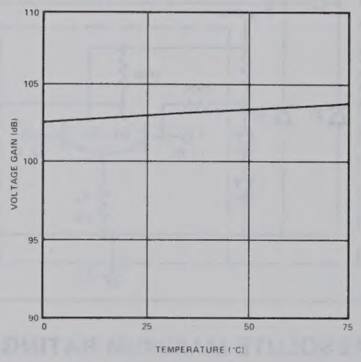
LM387-N

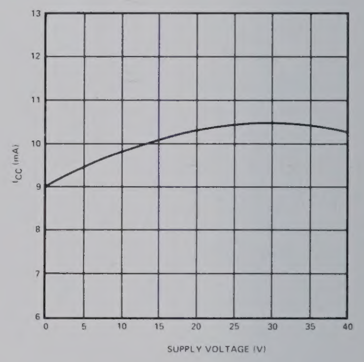
AC ELECTRICAL CHARACTERISTICS $T_A = 25\,°C$, $V_{CC} = 14V$ unless otherwise specified.

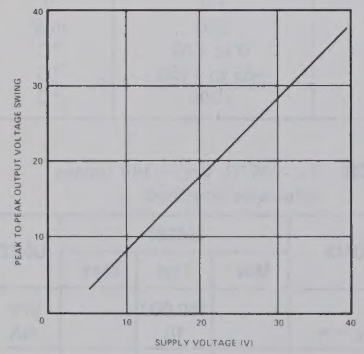
PARAMETER	TEST CONDITIONS	LM387 Min	LM387 Typ	LM387 Max	UNIT
Small signal bandwidth			15		MHz
Power bandwidth	20V p-p ($V_{CC} = 24V$)		75		kHz
Maximum input voltage	Linear operation			300	μVrms
Supply rejection ratio	f = 1kHz		110		dB
Channel separation	f = 1kHz		60		dB
Total harmonic distortion	75dB gain, f = 1kHz		0.1		%
Total equivalent input noise	$R_S = 600\Omega$, 100-10,000Hz		0.8	1.4	μVrms
Noise figure	50kΩ, 100-10,000Hz		1.0		dB
	10kΩ, 100-10,000Hz		1.6		dB
	5kΩ, 100-10,000Hz		2.8		dB

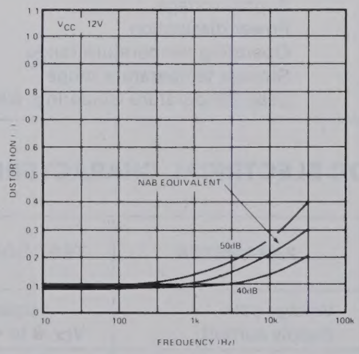
TYPICAL PERFORMANCE CHARACTERISTICS

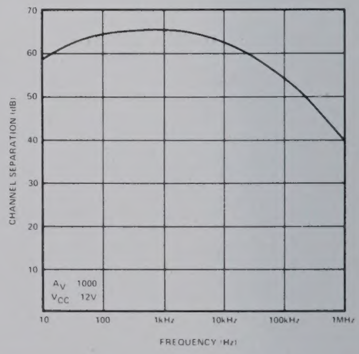

LARGE SIGNAL FREQUENCY RESPONSE


GAIN vs TEMPERATURE


V_{CC} vs I_{CC}


P-P OUTPUT VOLTAGE SWING vs V_{CC}

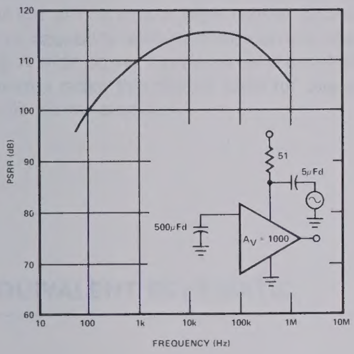

% DISTORTION


CHANNEL SEPARATION

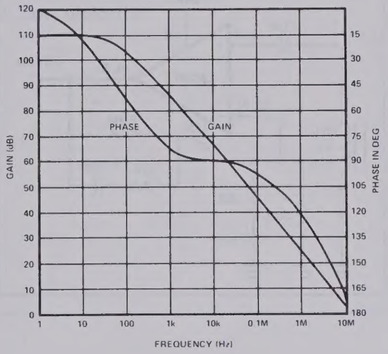
LM387-N

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

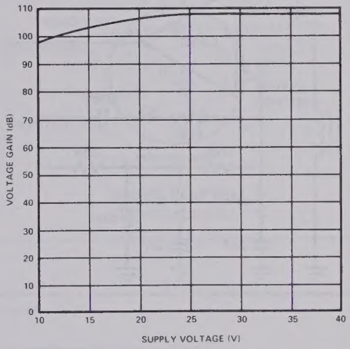
PSRR vs FREQUENCY



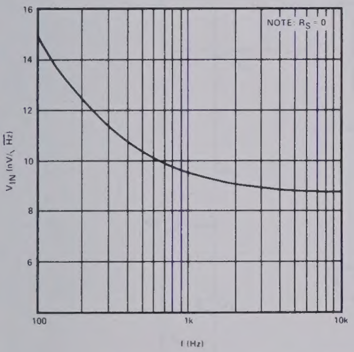
GAIN AND PHASE RESPONSE



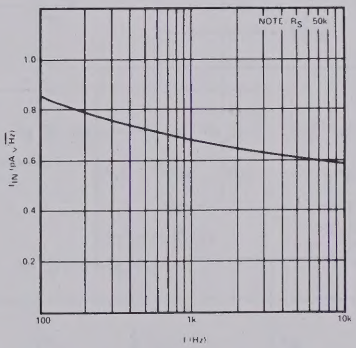
VOLTAGE GAIN vs SUPPLY VOLTAGE



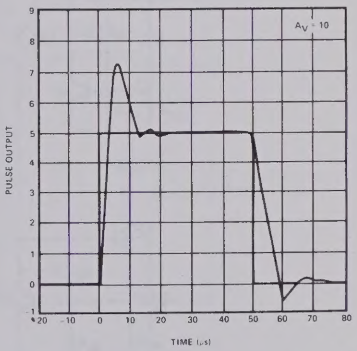
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

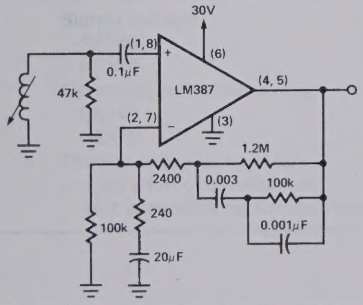


PULSE RESPONSE

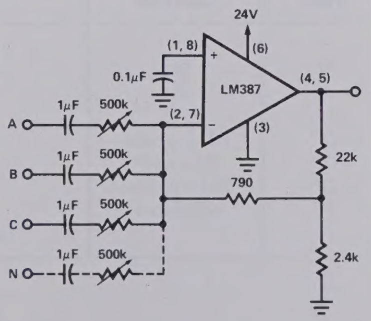


TYPICAL APPLICATIONS

TYPICAL MAGNETIC PHONO PREAMPLIFIER

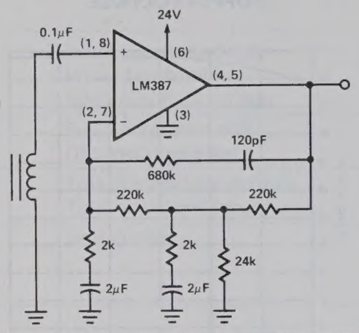

30V
(1,8)
+
(6)
0.1μF
47k
LM387
(4, 5)
(2, 7)
−
(3)
1.2M
2400
0.003
100k
240
100k
0.001μF
20μF

AUDIO MIXER

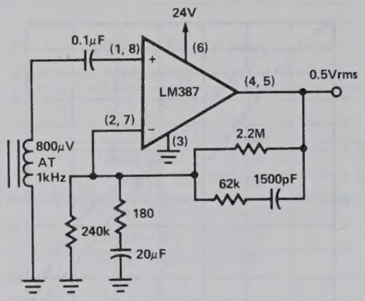

24V
(1, 8)
+
(6)
0.1μF
LM387
(4, 5)
(2, 7)
−
(3)
A
B
C
N
1μF
500k
1μF
500k
1μF
500k
1μF
500k
22k
790
2.4k

TYPICAL APPLICATIONS (Cont'd)

TWO-POLE FAST TURN-ON NAB TAPE PREAMPLIFIER


24V
0.1μF
(1, 8)
+
(6)
LM387
(4, 5)
(2, 7)
–
(3)
120pF
680k
220k
220k
2k
2k
24k
2μF
2μF

TYPICAL TAPE PLAYBACK AMPLIFIER


24V
0.1μF
(1, 8)
+
(6)
LM387
(4, 5)
0.5Vrms
(2, 7)
–
(3)
2.2M
800μV
AT
1kHz
62k
1500pF
180
240k
20μF

NE/SE540-H

DESCRIPTION

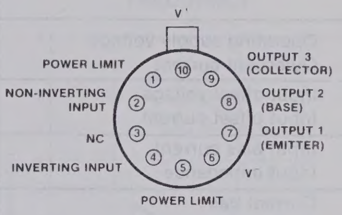
The NE/SE540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use an audio power amplifier.

FEATURES

- **Internal current limiting**
- **Low standby current**
- **High output current capability**
- **Wide power bandwidth**
- **Low distortion**

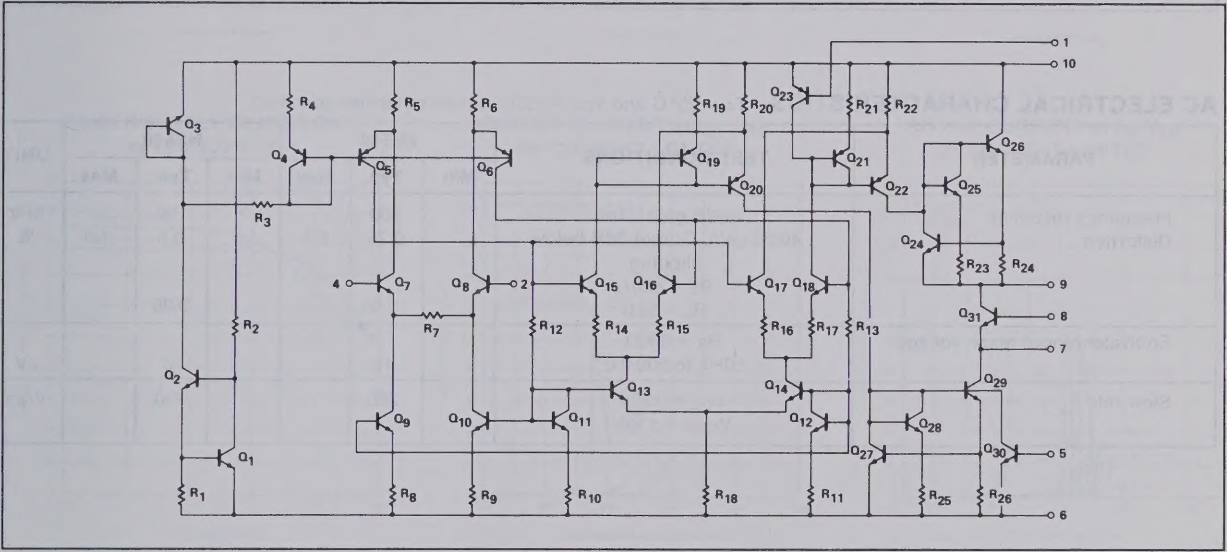
PIN CONFIGURATION

H PACKAGE


V⁺
POWER LIMIT
NON-INVERTING INPUT
NC
INVERTING INPUT
POWER LIMIT
OUTPUT 3 (COLLECTOR)
OUTPUT 2 (BASE)
OUTPUT 1 (EMITTER)
V⁻
1
2
3
4
5
6
7
8
9
10

ORDER PART NO.
NE540H, SE540H

EQUIVALENT SCHEMATIC


1
10
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
4
2
9
8
7
5
6

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE540	±27	V
NE540	±22	V
Operating temperature range		
SE540	-55 to +125	°C
NE540	0 to +70	°C
Storage temperature range	-65 to +150	°C
Output short circuit duration (Not exceeding maximum dissipation.)	Indefinite	

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = ±20V$ unless otherwise specified.

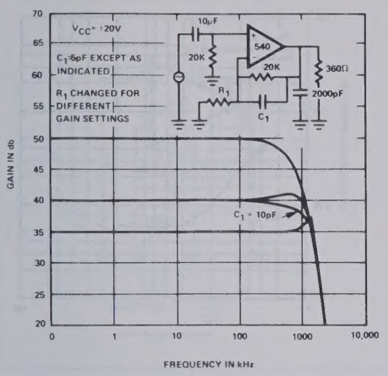
PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Operating supply voltage		±5		±25	±5		±20	V
Quiescent current			13	20		13	20	mA
Input offset voltage			5	7		7	10	mV
Input offset current			0.3	0.7		0.5	1	μA
Input bias current			1.5	3		2	5	μA
Input impedance			20			20		kΩ
Current gain		80	100		70	90		dB
Gain variation over temperature range	40dB gain		±0.1			±0.1		dB
Power supply rejection ratio	40dB gain	80	90		60	80		dB
Common mode rejection ratio			110			90		dB
Output drive current		±120	±150		±80	±100		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = ±20V$ unless otherwise specified.

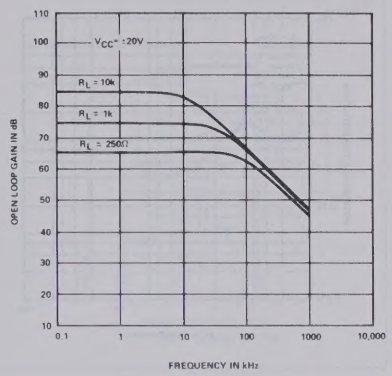
PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Frequency response	40dB gain ±1dB		500			100		kHz
Distortion	40dB gain, Output 3dB below clipping		0.25	0.5		0.5	1.0	%
	$R_L = 600Ω$							
	$R_L = 2kΩ$		0.06			0.06		
Equivalent input noise voltage	$R_S = 600Ω$ 50Hz to 500kHz		10			10		μV
Slew rate	$V_{CC} = ±20V$ $V_{OUT} = ±15V$		200			200		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

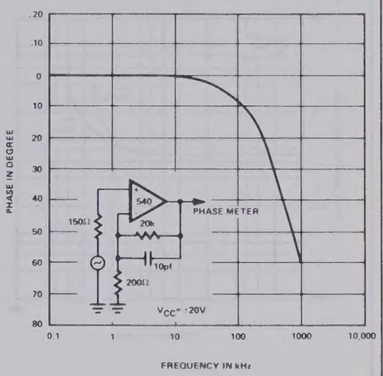
CLOSED LOOP FREQUENCY RESPONSE



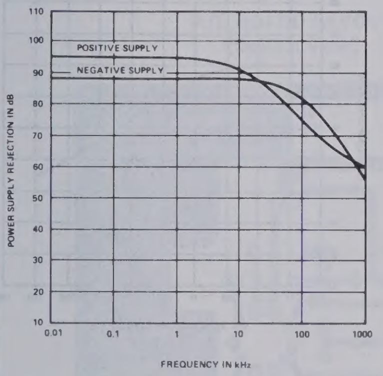
OPEN LOOP GAIN AND FREQUENCY RESPONSE



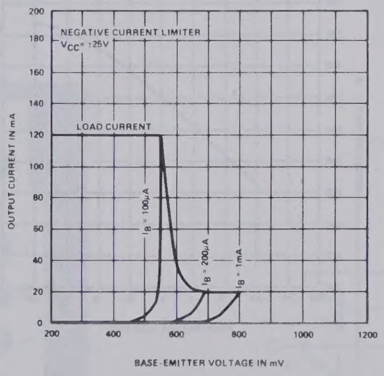
PHASE RESPONSE vs FREQUENCY



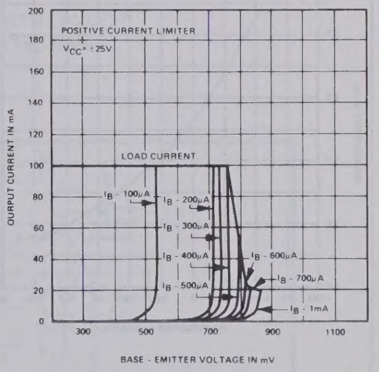
POWER SUPPLY REJECTION vs FREQUENCY



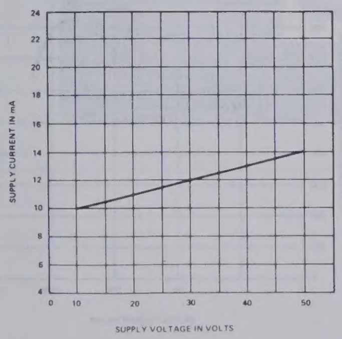
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



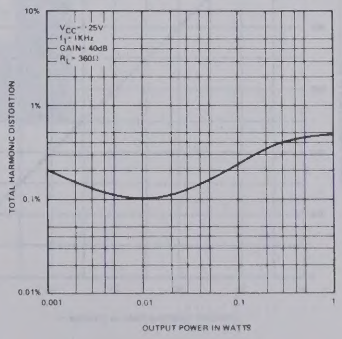
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



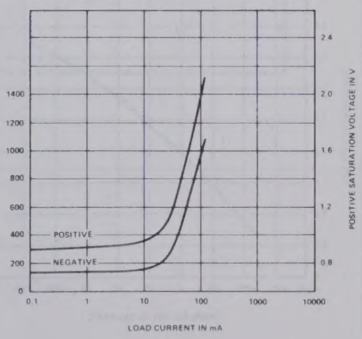
QUIESCENT CURRENT vs SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs OUTPUT

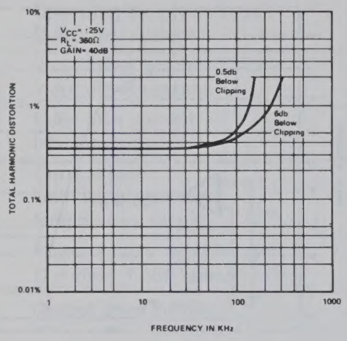


OUTPUT SATURATION VOLTAGE vs LOAD

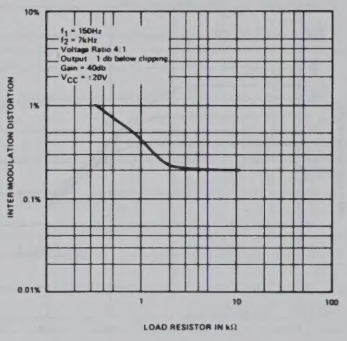


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

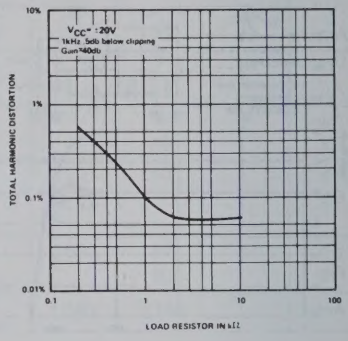
TOTAL HARMONIC DISTORTION vs FREQUENCY



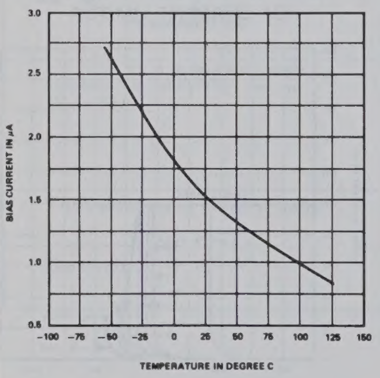
INTERMODULATION DISTORTION vs LOAD



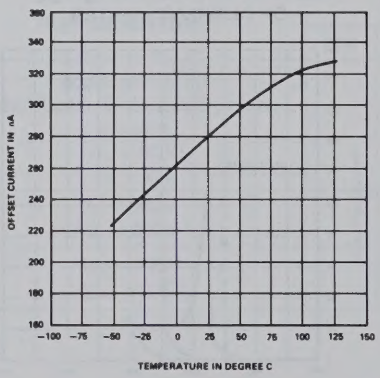
TOTAL HARMONIC DISTORTION vs LOAD



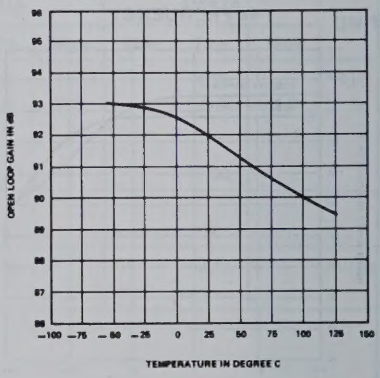
BIAS CURRENT vs TEMPERATURE



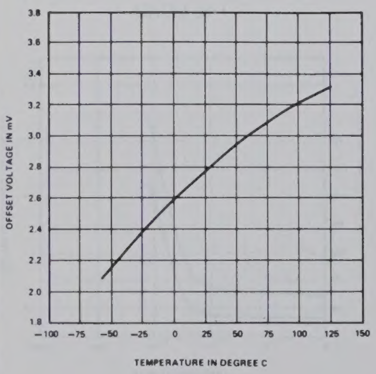
OFFSET CURRENT vs TEMPERATURE



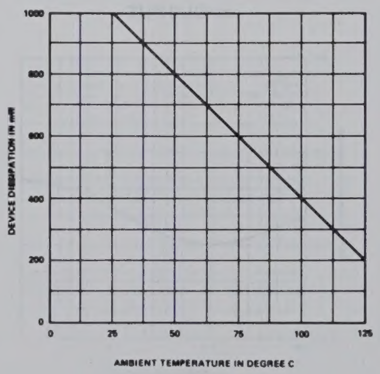
OPEN LOOP GAIN vs TEMPERATURE



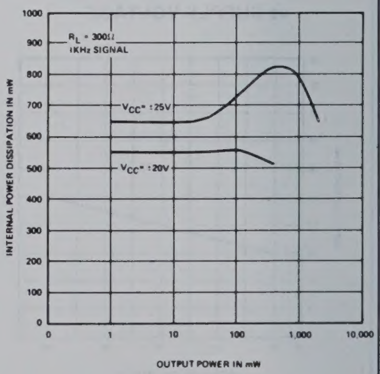
OFFSET VOLTAGE vs TEMPERATURE



MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE

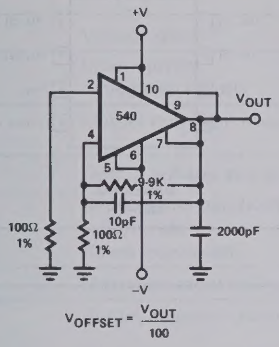


INTERNAL POWER DISSIPATION vs LOAD POWER



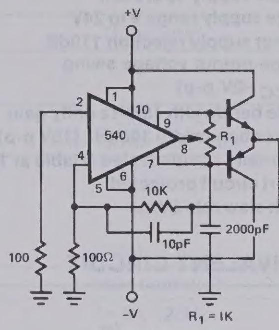
TEST CIRCUITS

OFFSET VOLTAGE MEASUREMENT


+V
1
2
10
540
9
VOUT
8
4
7
5
6
9.9K
1%
10pF
100Ω
1%
100Ω
1%
2000pF
−V

$V_{OFFSET} = \frac{V_{OUT}}{100}$

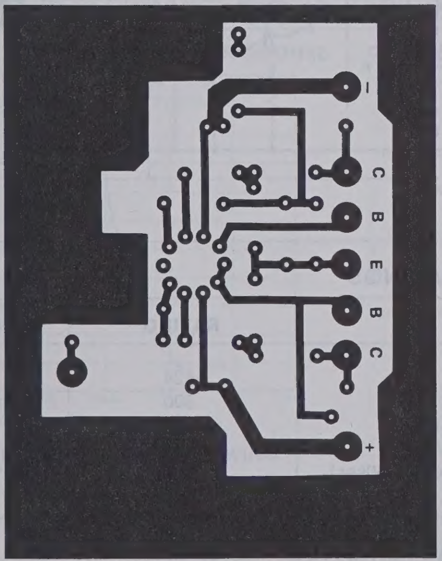
OUTPUT BIAS CONTROL


+V
1
2
10
540
9
R1
8
4
7
5
6
10K
10pF
2000pF
100
100Ω
−V
R1 = IK

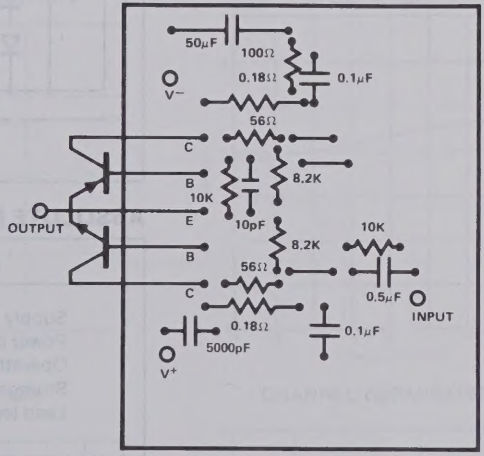
BIAS CONTROL FOR OUTPUT TRANSISTORS

35 WATT AMPLIFIER

P.C. BOARD LAYOUT (Bottom View)



PARTS LAYOUT (Top View)


50μF
100Ω
0.18Ω
0.1μF
V−
56Ω
C
B
10K
8.2K
OUTPUT
E
10pF
8.2K
10K
B
56Ω
C
0.5μF
INPUT
0.18Ω
0.1μF
5000pF
V+

DUAL LOW-NOISE PREAMP — NE542

NE542-N

DESCRIPTION

The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} -2Vp-p), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

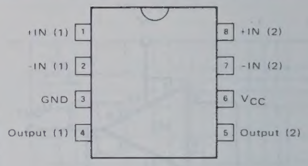
The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplication of small signals.

FEATURES

- **Low noise—.7μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC} -2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz (15V p-p)**
- **Internally compensated (stable at 10dB)**
- **Short circuit protected**
- **High slew rate 5V/μs**

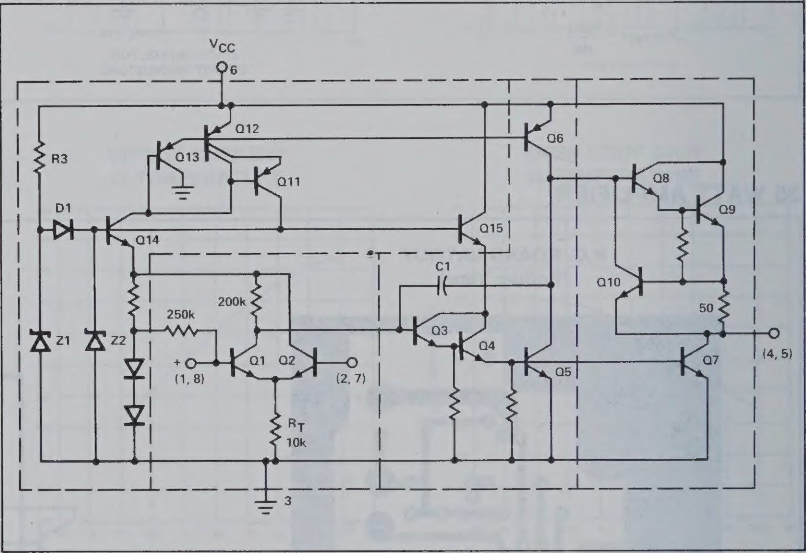
PIN CONFIGURATION

N PACKAGE



ORDER NO.
NE542N

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage		9		24	V
Supply current	V_{CC} = 9 to 18V, $R_L = \infty$		9	15	mA
Input resistance					
Positive input			100		kΩ
Negative input			200		kΩ
Output resistance	Open loop		150		Ω

NE542-N

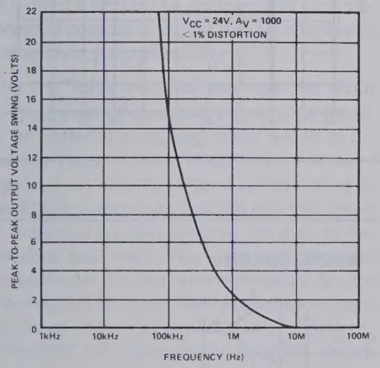
AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 14V unless otherwise specified.

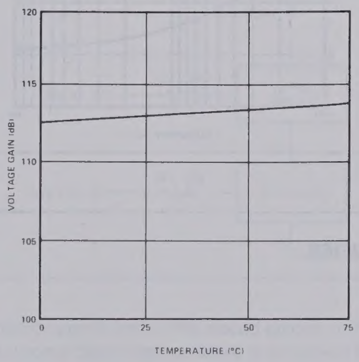
PARAMETER	TEST CONDITIONS	NE542 Min	NE542 Typ	NE542 Max	UNIT
Voltage gain	Open loop		160,000		V/V
Input current Negative input			.5		µA
Output current	Source	8	14		mA
	Sink (linear operation)	2	3		mA
Output voltage swing		V_{CC} -2.5	V_{CC} -2		V
Small signal bandwidth			15		MHz
Slew rate			5		V/µs
Power bandwidth	15V p-p		100		kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio	f = 60, 120Hz		100		dB
	f = 1kHz		110		dB
Channel separation	f = 1kHz		70		dB
Total harmonic distortion	75dB gain, f = 1kHz		.1		%
Total equivalent input Noise	RS = 600Ω, 100 - 10,000Hz		.7	1.2	µVrms
Noise figure	RS = 50kΩ, 10 - 10,000Hz		1.2		dB
	RS = 20kΩ, 10 10,000Hz		1.2		dB
	RS = 10kΩ, 10 - 10,000Hz		1.5		dB
	RS = 5kΩ, 10 - 10,000Hz		2.4		dB

TYPICAL PERFORMANCE CHARACTERISTICS

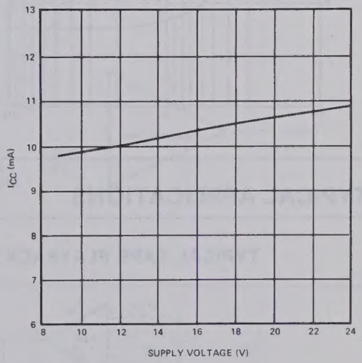
LARGE SIGNAL FREQUENCY RESPONSE



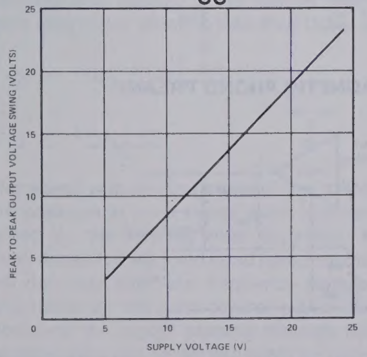
GAIN vs TEMPERATURE



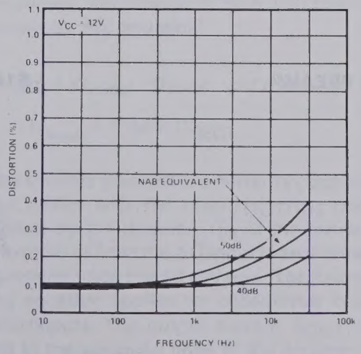
V_{CC} vs I_{CC}



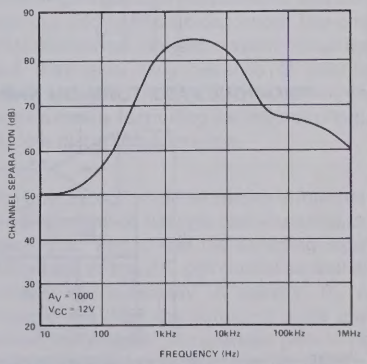
P-P OUTPUT VOLTAGE SWING vs V_{CC}



% DISTORTION

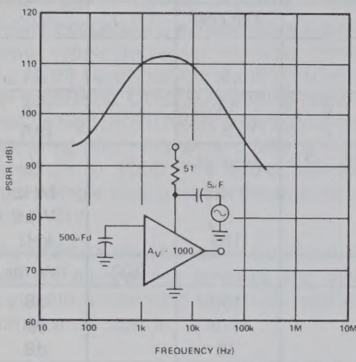


CHANNEL SEPARATION

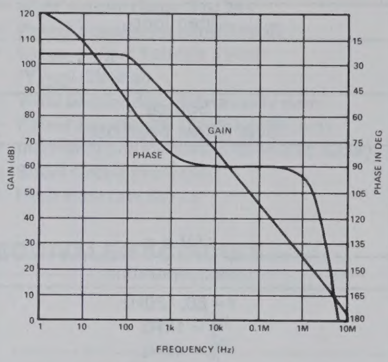


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

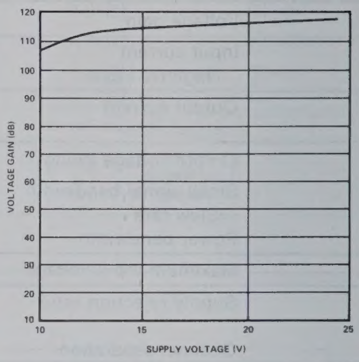
PSRR vs FREQUENCY



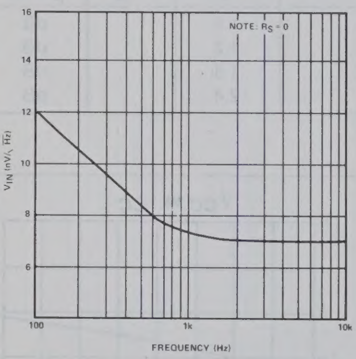
GAIN AND PHASE RESPONSE



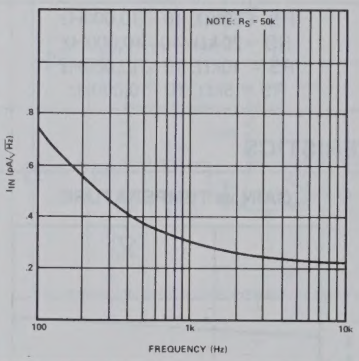
VOLTAGE GAIN vs SUPPLY VOLTAGE



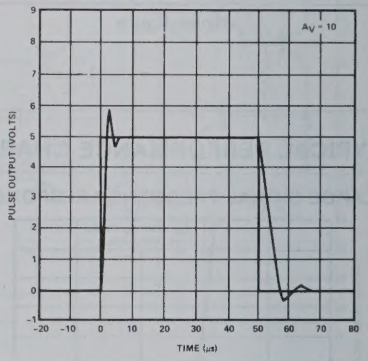
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

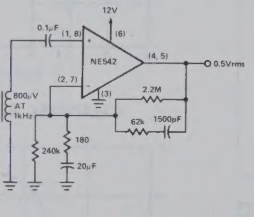


PULSE RESPONSE

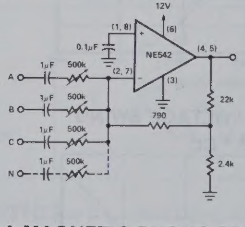


TYPICAL APPLICATIONS

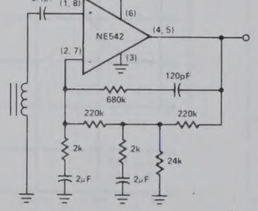
TYPICAL TAPE PLAYBACK AMPLIFIER


12V
0.1μF
(1, 8)
(6)
NE542
(4, 5)
0.5Vrms
(2, 7)
(3)
2.2M
800μV
AT
1kHz
62k
1500pF
180
240k
20μF

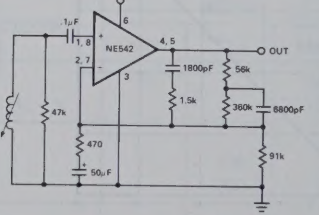
AUDIO MIXER


12V
(1, 8)
(6)
0.1μF
NE542
(4, 5)
(2, 7)
(3)
A
B
C
N
1μF
500k
1μF
500k
1μF
500k
1μF
500k
22k
790
2.4k

TWO-POLE FAST TURN-ON NAB TAPE PREAMP


12V
0.1μF
(1, 8)
(6)
NE542
(4, 5)
(2, 7)
(3)
120pF
680k
220k
220k
2k
2k
24k
2μF
2μF

R1AA MAGNETIC PHONO PREAMP


VCC = +16V
6
.1μF
1, 8
NE542
4, 5
OUT
2, 7
3
1800pF
56k
1.5k
360k
6800pF
47k
470
50μF
91k

NOTE: All resistors values are typical and in ohms.

NE570/571-F,N
SA571-F,N

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

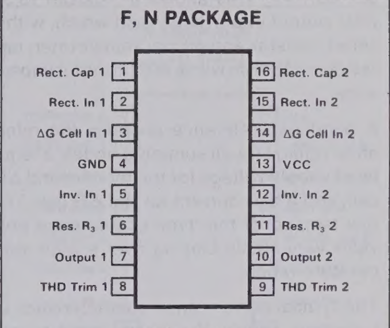
FEATURES

- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

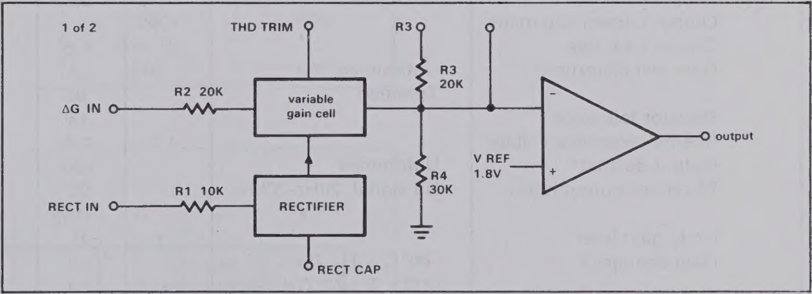


Order Part No.
NE570 F,N
NE571 F,N
SA571 F,N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ \text{ave}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\ \text{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

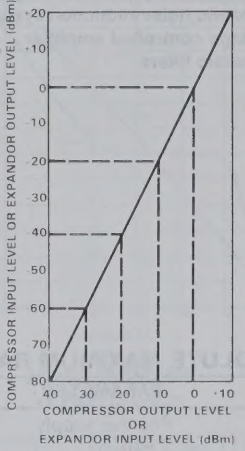
The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

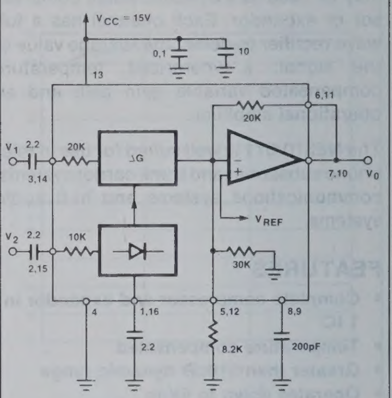
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

BASIC INPUT-OUTPUT TRANSFER CURVE



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 15V$[1]

PARAMETER	TEST CONDITIONS	NE570			NE/SA571[6]			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0		3.2	4.8	mA
Output current capability		±20						mA
Output slew rate			±.5					V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 20Hz-20kHz		20					μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBm
Gain change[2,4]	-40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	-40°C < T < 70°C		+2, -25	-10, -40		+2, -25	+20, -50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	-40°C < T < 70°C		+8,-0					%
	0°C < T < 70°C		+1,-0					
Tracking error [5], input V_1 = OdBm	Rectifier input, V_2 =							dB
	+6dBm		±.2					
	-10dBm		+.2	-.2,+.4		+.2	-.2,+.5	
	-20dBm		+.2	-.3,+.6		+.2	-.4,+.7	
	-30dBm		+.2	-.5,+1		+.2	-1,+1.5	
	-40dBm		+.2,-.4			+.2,-.4		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at OdBm,1kHz
3. Expandor ac input change from no signal to OdBm
4. Relative to value at $T_A = 25°C$
5. Relative to OdBm
6. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.

PROGRAMMABLE ANALOG COMPANDOR NE572

PRELIMINARY SPECIFICATION

NE572-N

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic gain compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

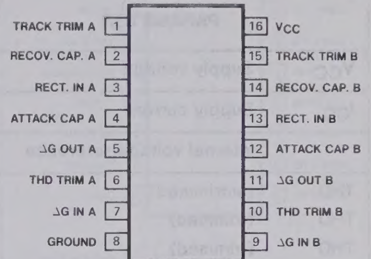
- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise**
- **Wide supply voltage range—down to 6V.**
- **System level adjustable with external components.**

APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

PIN CONFIGURATION

N PACKAGE
(Top view)

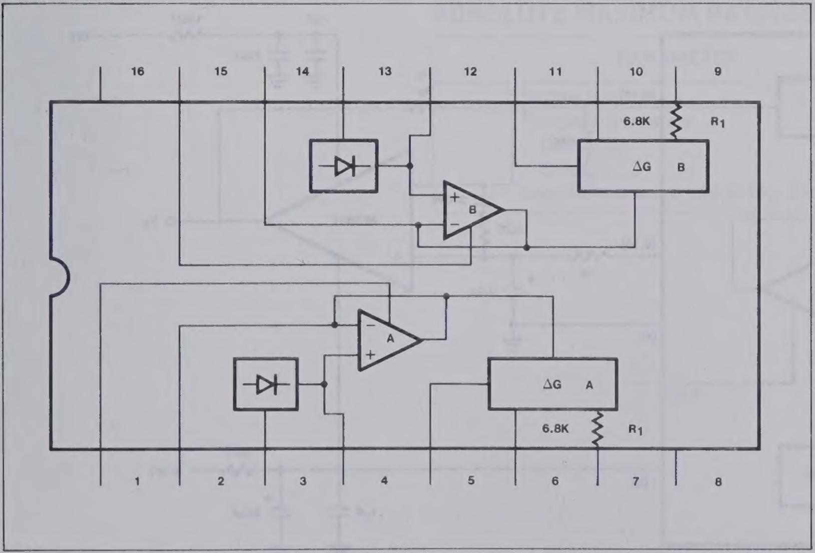

TRACK TRIM A 1
RECOV. CAP. A 2
RECT. IN A 3
ATTACK CAP A 4
ΔG OUT A 5
THD TRIM A 6
ΔG IN A 7
GROUND 8
16 V_{CC}
15 TRACK TRIM B
14 RECOV. CAP. B
13 RECT. IN B
12 ATTACK CAP B
11 ΔG OUT B
10 THD TRIM B
9 ΔG IN B

ORDER PART NO.
NE572N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM

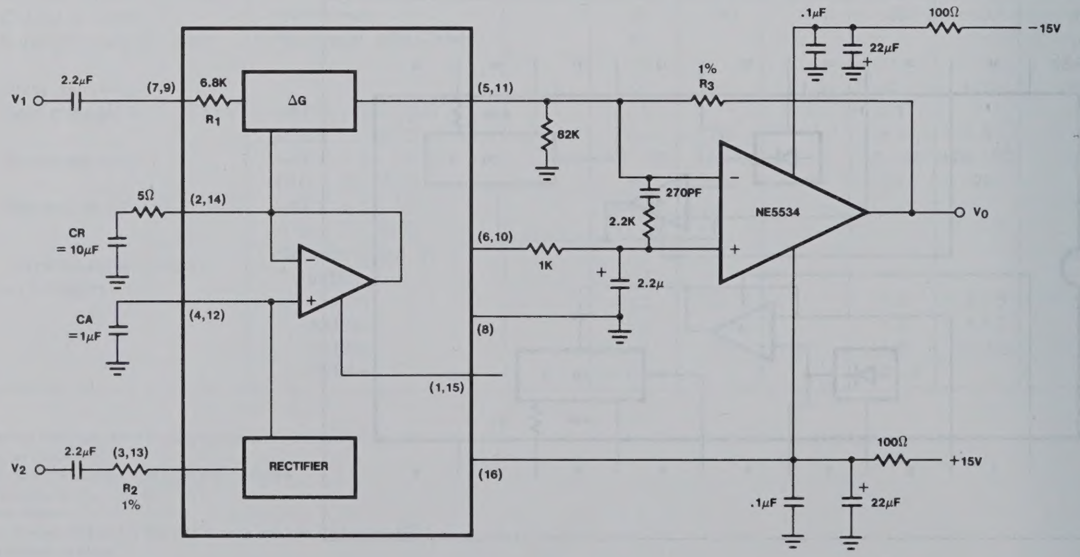

16
15
14
13
12
11
10
9
6.8K
R1
ΔG B
B
+
−
−
A
+
ΔG A
6.8K
R1
1
2
3
4
5
6
7
8

ELECTRICAL CHARACTERISTICS

Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K R_3 = 17.3K

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD THD THD	(untrimmed) (trimmed) (trimmed)	1kHz $C_A = 1.0\mu F$ 1kHz $C_R = 10\mu F$ 100Hz		.2 .05 .25	1.0	% % %
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		10	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		1.0	3.0	%
	Tracking error measured relative to value at unity gain output	Rectifier input V_2 = +6dB −30dB		±.2 ±.5	 −1.5 +.8	dB
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		60		dB

TEST CIRCUIT


V1
2.2μF
(7,9)
6.8K
R1
ΔG
(5,11)
82K
1%
R3
.1μF
100Ω
−15V
22μF
5Ω
(2,14)
CR
= 10μF
270PF
2.2K
NE5534
Vo
(6,10)
1K
2.2μ
CA
=1μF
(4,12)
(8)
(1,15)
V2
2.2μF
(3,13)
R2
1%
RECTIFIER
(16)
100Ω
+15V
.1μF
22μF

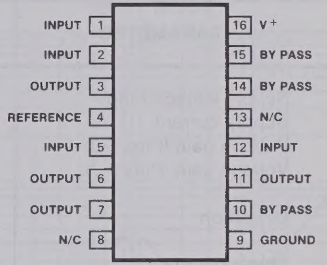
DESCRIPTION

The NE645B/646B is a monolithic audio noise reduction system circuit. This circuit is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is intended for use in a Dolby* B-type noise reduction system and is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco.

NOTE
*T.M. Dolby Laboratories

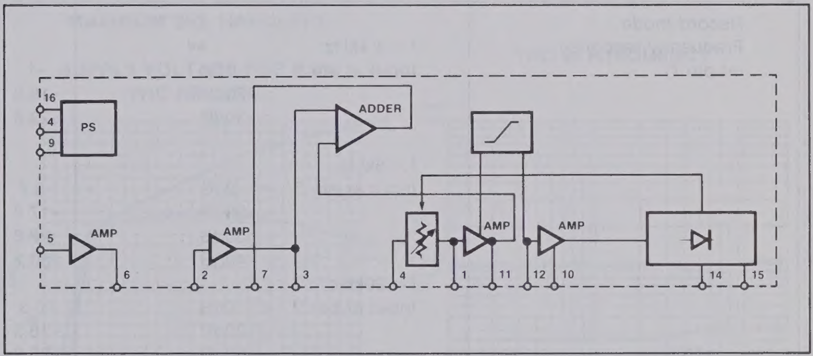
PIN CONFIGURATION (Top View)

N PACKAGE


INPUT 1
INPUT 2
OUTPUT 3
REFERENCE 4
INPUT 5
OUTPUT 6
OUTPUT 7
N/C 8
16 V+
15 BY PASS
14 BY PASS
13 N/C
12 INPUT
11 OUTPUT
10 BY PASS
9 GROUND

Order Part No. NE645BN/646BN

BLOCK DIAGRAM


16
4
9
PS
ADDER
5
AMP
6
AMP
2
7
3
4
AMP
1
11
AMP
12
10
14
15

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		°C
Operating	0 to +70	
Storage	-65 to +150	
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12 volts, f = 20Hz to 20kHz.
All levels referenced to 580mVrms (0dB) at Pin 3, T_A = +25°C
unless otherwise noted.

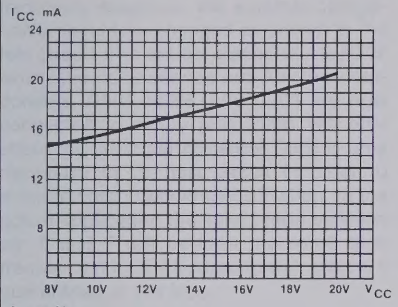
PARAMETER	TEST CONDITIONS	NE645B			NE646B			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage range		8		20	8		20	V
Supply current			16	24		16	24	mA
Voltage gain (Pins 5-3)	f = 1kHz (Pins 6 & 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (Pins 3-7)	f = 1kHz, 0dB at pin 3, Noise reduction out	-0.5	0	+0.5	-0.5	0	+0.5	dB
Distortion	f = 20Hz -20kHz 0db		0.05	0.1		0.05	0.2	%
	f = 20Hz -15kHz, +10db		0.15	0.3		0.2	0.5	%
Signal handling	f = 1kHz distortion <0.3%	+10	+14					dB
Signal handling	f = 1kHz distortion < 0.5%				+10	+12		dB
*Signal-to-noise ratio	Record (Pins 6 & 2 connected)	67	72		64	68		dB
	Record (Input on pin 2)	67	72		64	68		dB
	Playback (Pins 6 & 2 connected)	77	82		74	78		dB
	Playback (Input on pin 2)	77	82		74	78		dB
Record mode								
Frequency response	f = 1.4kHz							
(at pin 7)	Input at pin 5 = 0dB	-1	0	+1	-1.5	0	+1.5	dB
	= -20dB	-16.6	-15.6	-14.6	-17.1	-15.6	-14.1	dB
	= -30dB	-23.5	-22.5	-21.5	-24.0	-22.5	-21.0	dB
	f = 5kHz							
	Input at pin 5 = 0dB	-0.7	+0.3	+1.3	-1.2	+0.3	+1.8	dB
	= -20dB	-17.8	-16.8	-15.8	-18.3	-16.8	-15.3	dB
	= -30dB	-22.8	-21.8	-20.8	-23.8	-21.8	-20.3	dB
	= -40dB	-30.2	-29.7	-28.7	-30.2	-29.7	-28.2	dB
	f = 20kHz							
	Input at pin 5 = 0dB	-0.3	+0.7	+1.7	-0.8	+0.7	+2.2	dB
	= -20dB	-18.3	-17.3	-16.3	-18.8	-17.3	-15.8	dB
	= -30dB	-25.2	-24.2	-23.2	-25.7	-24.2	-22.7	dB
Back-to-back frequency Response	Using typical record Mode response	-1	0	+1	-1.5	0	+1.5	dB
Input resistance	Pin 5	35	50	65	35	50	65	kΩ
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	kΩ
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	kΩ
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω

NOTE

* All noise levels are measured CCIR/ARM weighted and 10K source with respect to Dolby level. See Dolby Laboratories bulletin 19.

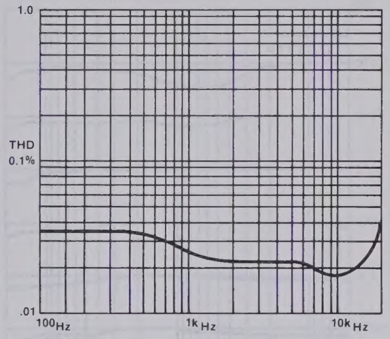
PERFORMANCE CHARACTERISTICS NE645B

ICC vs SUPPLY VOLTAGE



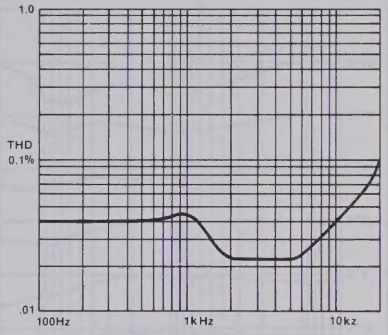
I_{CC} vs V_{CC}

THD vs FREQUENCY RECORD MODE



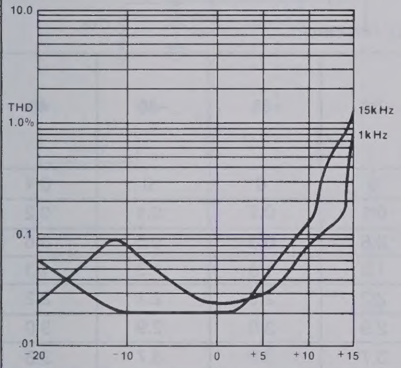
0dB Dolby record
V_{CC} = 12V

THD vs FREQUENCY PLAY MODE



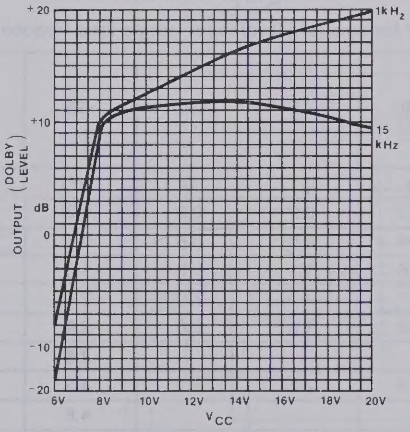
0dB Dolby play
V_{CC} = 12V

THD vs OUTPUTS

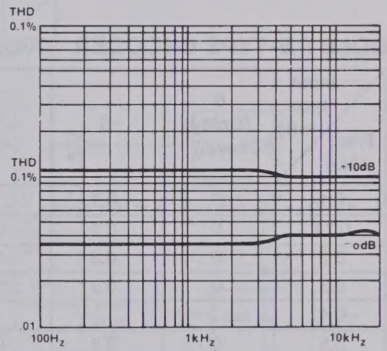


THD vs Output and f_0 record
V_{CC} = 12V

MAXIMUM SIG. HANDLING vs SUPPLY VOLTAGE FOR 0.3% THD RECORD

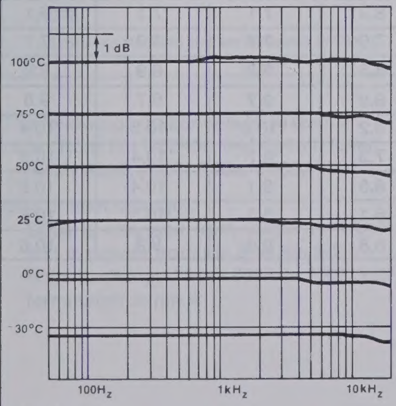


THD vs FREQUENCY



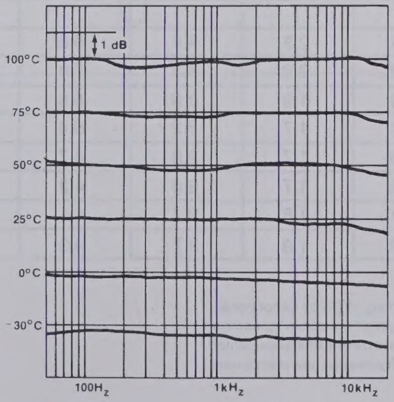
Noise reduction off
V_{CC} = 12V

BACK TO BACK RESPONSE vs TEMP AND FREQUENCY



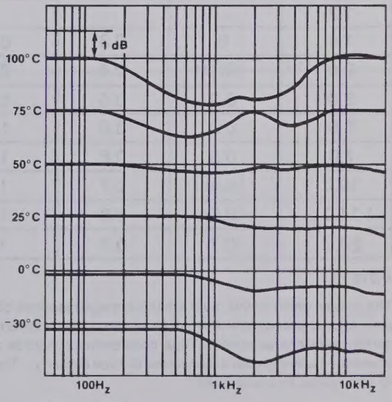
0dB Dolby level
V_{CC} = 12V
Decode = 25°C

BACK TO BACK RESPONSE vs TEMP AND FREQUENCY



-10dB Dolby level
V_{CC} = 12V
Decode = 25°C

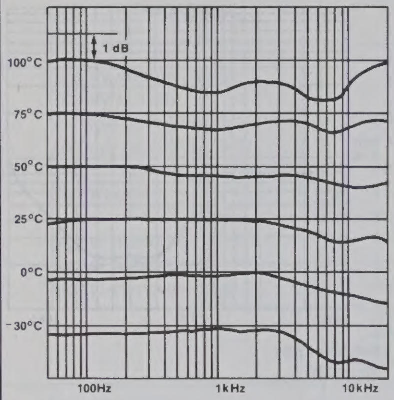
BACK TO BACK RESPONSE vs TEMP AND FREQUENCY



-20dB Dolby level
V_{CC} = 12V
Decode = 25°C

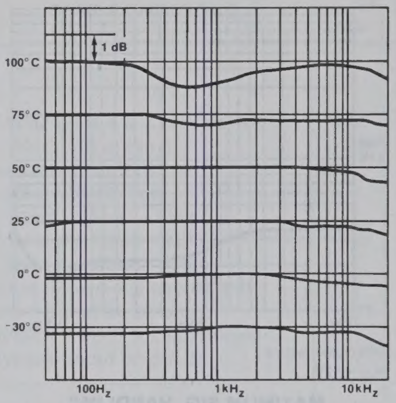
PERFORMANCE CHARACTERISTICS NE645B (cont'd)

BACK TO BACK RESPONSE vs TEMP AND FREQUENCY



-30dB Dolby level
V_{CC} = 12V
Decode = 25°C

BACK TO BACK RESPONSE vs TEMP AND FREQUENCY



-40dB Dolby level
V_{CC} = 12V
Decode = 25°C

DOLBY B-TYPE ENCODER Output for constant level input (single tone frequency response)

Input level (dB) / Freq. (kHz)	0 (Dolby Level)	−5	−10	−15	−20	−25	−30	−35	−40	−45
0.1	0	0.1	0	0.1	0	0	0	0	0	0.1
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1	0.2
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.3	0.5	0.6
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1	2.2
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9	3.0
0.6						3.6	3.7	3.8	3.7	3.8
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4	4.6
0.8						4.8	5.0	5.3	5.1	5.2
0.9							5.6	5.8	5.6	5.8
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2	6.3
1.2							6.9	7.1	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7	9.8
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3	10.4
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4	10.6
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4	10.6
14.0	0.5	0.8	1.1	1.8	2.7	4.1	6.1	8.5	10.3	10.6
20.0	0.7	0.7	1.2	1.9	2.7	4.0	5.8	8.0	9.9	10.6

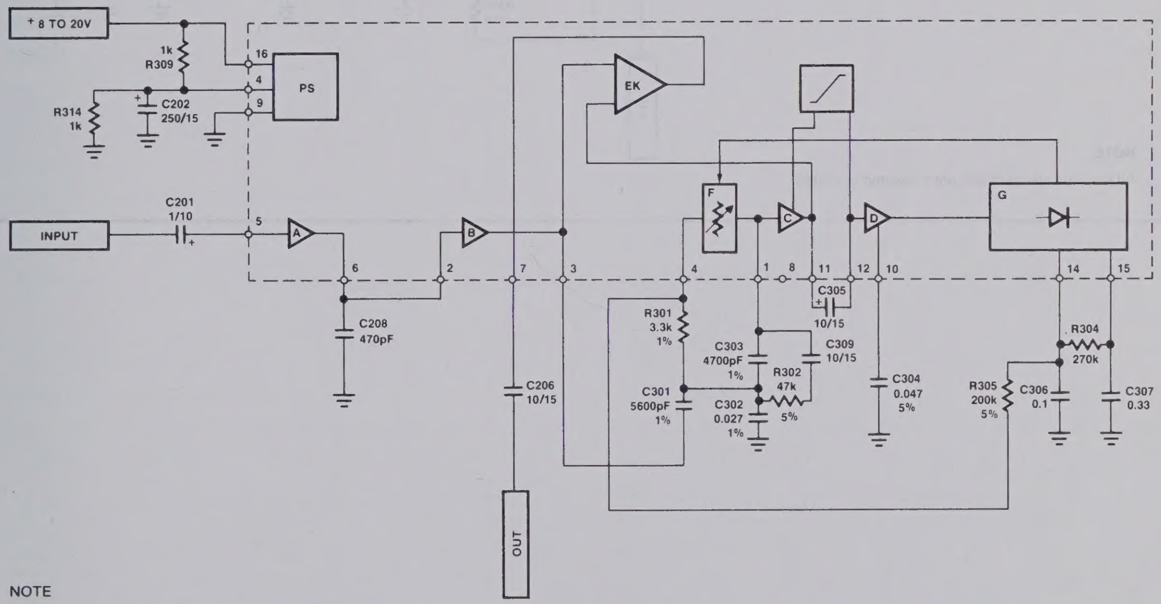
NOTE

The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must maintain in consumer B-Type circuitry. The figures can however be used to plot typical characteristics.

APPLICATION INFORMATION

The NE645B/646B is a direct replacement for the NE545B. For a ±1dB back-to-back frequency response, the external components should be changed as shown in the test circuit. The critical component is R307 which should be shorted out. All other components, R303, R308, and C308 are now connected to empty pins. D301 will only effect the burst performance. C208 is only necessary in the test circuit in order to eliminate high frequency oscillation. In the actual application the 19kHz filter between pin 6 and 2 will perform the same high frequency roll off. All curcuit parameters are guaranteed at 12V V_{CC}.

TEST CIRCUIT NE645B/646B


+ 8 TO 20V
1k
R309
R314
1k
C202
250/15
16
4
9
PS
INPUT
C201
1/10
5
A
B
EK
F
C
D
G
6
2
7
3
4
1
8
11
12
10
14
15
C208
470pF
C206
10/15
OUT
R301
3.3k
1%
C301
5600pF
1%
C303
4700pF
1%
C302
0.027
1%
R302
47k
5%
C305
10/15
C309
10/15
C304
0.047
5%
R304
270k
R305
200k
5%
C306
0.1
C307
0.33

NOTE

All resistors standard and are measured in OHMS

The following components have been eliminated from the NE545B test circuit: (over)

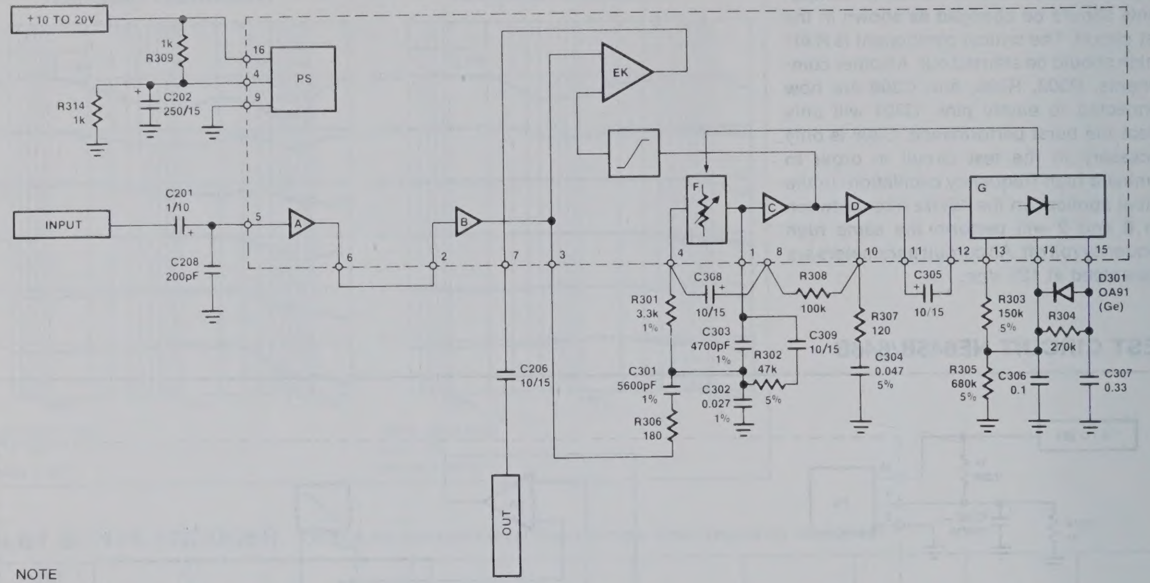
R303, R306, R307, R308, C308, D301

Component changes:

C208 is changed from 200pF to 470pF and is moved from pin 5 to pin 6/2

R305 is changed from 680K to 200K and terminated at pin 4

TEST CIRCUIT NE545B


+10 TO 20V
1k
R309
R314
1k
C202
250/15
16
4
9
PS
INPUT
C201
1/10
C208
200pF
5
A
6
B
2
7
3
EK
F
C
D
G
4
1
8
10
11
12
13
14
15
C308
10/15
R308
100k
C305
10/15
D301
OA91
(Ge)
R301
3.3k
1%
C303
4700pF
1%
C309
10/15
R307
120
C304
0.047
5%
R303
150k
5%
R304
270k
C206
10/15
C301
5600pF
1%
R306
180
R302
47k
5%
C302
0.027
1%
R305
680k
5%
C306
0.1
C307
0.33
OUT

NOTE
All resistors standard and are measured in OHMS.

SECTION 14
PHASE LOCKED LOOPS

Section 14—PHASE LOCKED LOOPS

NE/SE564 Phase Locked Loop 436
NE/SE565 Phase Locked Loop 443
NE/SE566 Function Generator 448
NE/SE567 Tone Decoder/Phase Locked Loop 451

PHASE LOCKED LOOPS DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

FREE-RUNNING FREQUENCY (f_o', ω_o').

Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_o' and ω_o' which are used for the general oscillator frequency. (Many references use f_o' and ω_o' for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). The appropriate units for f_o' and ω_o' are Hz and radians per second respectively.

LOCK RANGE ($2f_L$, $2\omega_L$).*

The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_o'. The deviations from f_o' are referred to as the *Tracking Range* or *Hold-in Range.* (See figure 1.6). The tracking range is therefore one-half of the lock range.

CAPTURE RANGE ($2f_C$, $2\omega_C$).**

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_o' with the equal deviations called the *Lock-in* or *Pull-in Ranges.* The capture range can never exceed the lock range.

LOCK-UP TIME (t_L).***

The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lock-up time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

PHASE COMPARATOR CONVERSION GAIN (K_d).

The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

VCO CONVERSION GAIN (K_o).

The conversion constant relating the oscillators frequency shift from f_o' to the applied input voltage. K_o has units of radians per second per volt (rad/sec/volt). K_o is a linear function of ω_o' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_o'.

LOOP GAIN (K_v).

The product of K_d, K_o, and the low-pass filters gain at dc. K_d is evaluated at the appropriate input signal level and K_o at the appropriate ω_o'. K_v has units of $(\text{sec})^{-1}$.

CLOSED LOOP GAIN (CLG).

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_v}{1 + K_v} \qquad \text{(Equation 1.4)}$$

NATURAL FREQUENCY (ω_n).

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_o' and at which the phase error swing is the greatest.

DAMPING FACTOR (ζ).

The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

LOOP NOISE BANDWIDTH (B_L).

A loop property relating ω_n and τ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

* Also called Synchronization Range.

** Also called Acquisition Range.

*** Also called Acquisition Time.

NOTE

Refer to Section 10 of the 1979 Analog Applications Manual for an in-depth explanation of Phase Locked Loops and their applications.

NE/SE564-D,F,N

DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

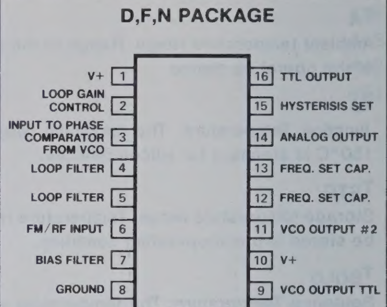
APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators

FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (Externally Controlled)

PIN CONFIGURATION

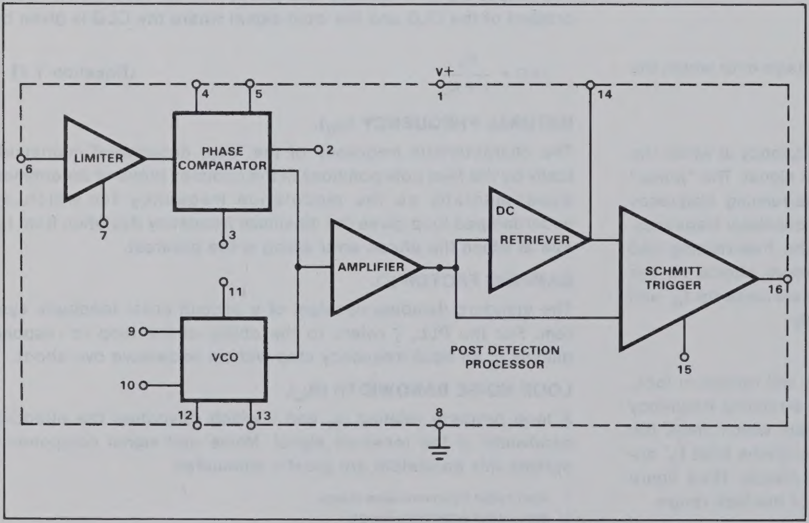

D,F,N PACKAGE
V+ 1
LOOP GAIN CONTROL 2
INPUT TO PHASE COMPARATOR FROM VCO 3
LOOP FILTER 4
LOOP FILTER 5
FM/RF INPUT 6
BIAS FILTER 7
GROUND 8
16 TTL OUTPUT
15 HYSTERISIS SET
14 ANALOG OUTPUT
13 FREQ. SET CAP.
12 FREQ. SET CAP.
11 VCO OUTPUT #2
10 V+
9 VCO OUTPUT TTL

ORDER PART NO.
NE/SE564F
NE/SE564N
NE/SE564D

ABSOLUTE MAXIMUM RATINGS

	PARAMETER		RATING	UNIT
V+	Supply voltage			V
	Pin 1		14	
	Pin 10		6	
P_D	Power dissipation		400	mW
T_A	Operating temperature	NE	0 to 70	°C
	Operating temperature	SE	−55 to +125	
t_{stg}	Storage temperature		−65 to 150	°C

BLOCK DIAGRAM


V+
1
4
5
14
LIMITER
6
7
PHASE COMPARATOR
2
3
DC RETRIEVER
AMPLIFIER
SCHMITT TRIGGER
16
15
11
9
VCO
10
12
13
8
POST DETECTION PROCESSOR

FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}} \qquad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO (see figure 7)
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is

ELECTRICAL CHARACTERISTICS

V+ = 5V, T_A = 25°C, fo = 5MHz, I_B = −200µA unless otherwise specified.
Test Circuit: Figure 1

PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency		50	65		45	60		MHz
Lock range	Input ≥ 200mVrms, T_A = 25°C	60	90		60	90		% of fo
	= 125°C	30	50					
	= −55°C	120	150					
	= 0°C				100	120		
	= 70°C				50	70		
Capture range	Input ≥ 200mVrms, R2 = 27Ω	25	35		25	35		% of fo
	= 100Ω	35	50		35	50		
VCO frequency drift with temperature	fo = 5MHz, T_A = −55°C to 125°C		400	1000				PPM/°C
	= 0°C to 70°C					400	1250	
	fo = 500kHz, T_A = −55°C to 125°C		250	500				
	= 0°C to 70°C					400	850	
VCO frequency change with supply voltage	V+ = 4.5V to 5.5V		3	6		3	6	% of fo
Demodulated output voltage	Modulation frequency: 1kHz, fo = 5MHz							
	Input deviation: 10%, T = 25°C	120	140		120	140		mVrms
	1%, T = 25°C	10	14		10	14		mVrms
	T = 0°C				9	13		mVrms
	= −55°C	8	12					mVrms
	= 70°C				13	15		mVrms
	= 125°C	14	16					mVrms
Linearity	Deviation: 1% to 8%		1	3		1	3	%
Signal to noise ratio			40			40		dB
AM rejection			35			35		dB
Supply current	V+ = 5V		35	50		35	50	mA
Leakage current	Pin 9		1	10		1	10	µA
Output current	Pin 9			6			6	mA
Supply voltage	Pin 1	4.5		12	4.5		12	V
	Pin 10	4.5		5.5	4.5		5.5	V

accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysterisis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25}-Q_{26}$ form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

$$f_o = \frac{1}{16R_CC_1} \qquad \text{Equation 2}$$

$R_C = R_{19} = R_{20}$ = 100Ω (INTERNAL)
C_1 = external frequency setting capacitor

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysterisis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier $Q_{42}-Q_{43}$ together with an external capacitor which is connected at the amplifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_m}{C_2} \quad V_{in}dt \qquad \text{Equation 3}$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of $Q_{49}-Q_{50}$ with positive feedback being provided by $Q_{47}-Q_{48}$. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_o = \frac{1}{16R_cC_1} \text{ in Hz} \qquad \text{Equation 4}$$

R_c = 100Ω
C_1 = external cap in farads

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \qquad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function

$$\text{at } \omega = \frac{1}{RC_3}.$$

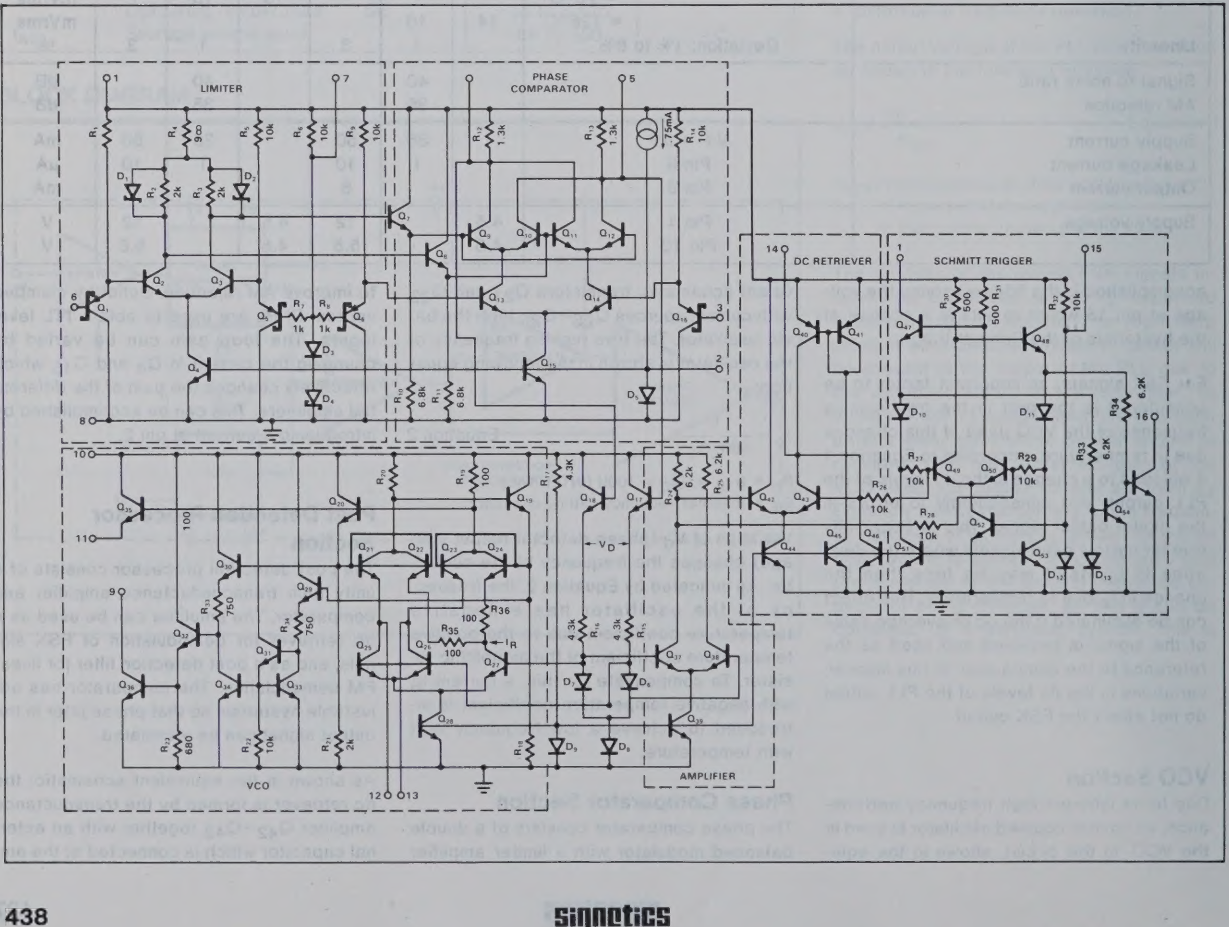
FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1% or higher).

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

EQUIVALENT SCHEMATIC



FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 6 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

Figure 9 indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies.

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

SE/NE 564 TEST CIRCUIT

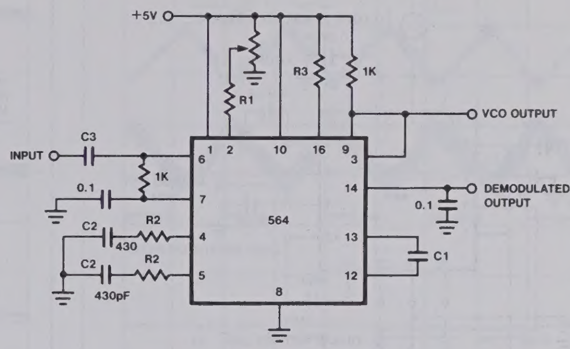

+5V
R1
R3
1K
VCO OUTPUT
C3
INPUT
1K
0.1
C2
430
R2
C2
430pF
R2
1
2
10
16
9
3
6
7
4
5
14
13
12
8
564
0.1
DEMODULATED OUTPUT
C1

Figure 1

FM DEMODULATOR AT 5V

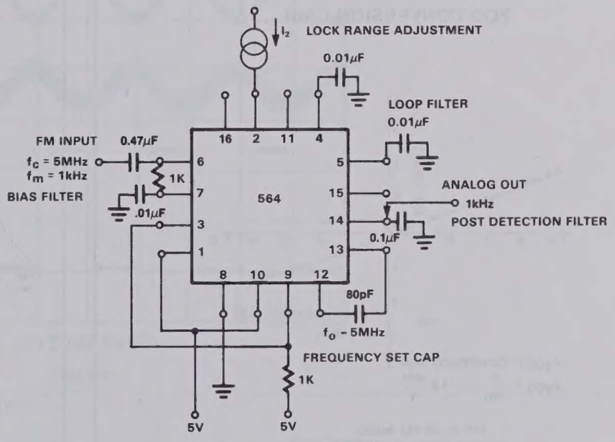

I_2
LOCK RANGE ADJUSTMENT
0.01μF
LOOP FILTER
0.01μF
FM INPUT
0.47μF
f_c = 5MHz
f_m = 1kHz
1K
BIAS FILTER
.01μF
16
2
11
4
6
7
3
1
5
15
14
13
8
10
9
12
564
ANALOG OUT
1kHz
POST DETECTION FILTER
0.1μF
80pF
f_o ~ 5MHz
FREQUENCY SET CAP
1K
5V
5V

Figure 2

FM DEMODULATOR AT 12V

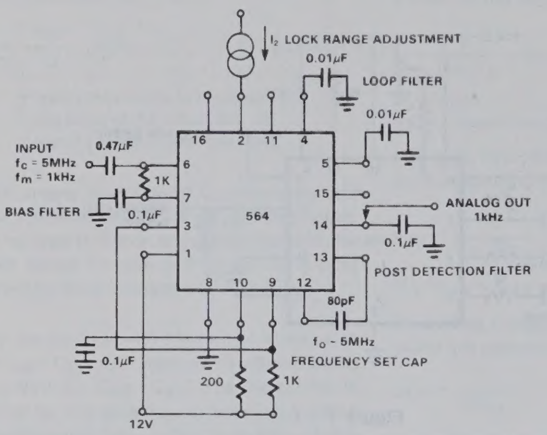

I₂ LOCK RANGE ADJUSTMENT
0.01μF
LOOP FILTER
0.01μF
INPUT
fc = 5MHz
fm = 1kHz
0.47μF
1K
BIAS FILTER
0.1μF
564
16
2
11
4
6
7
3
1
5
15
14
13
8
10
9
12
ANALOG OUT
1kHz
0.1μF
POST DETECTION FILTER
80pF
fo ~ 5MHz
FREQUENCY SET CAP
0.1μF
200
1K
12V

Figure 3

MODULATOR

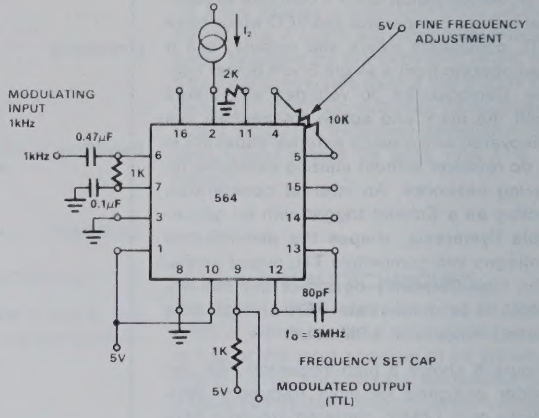
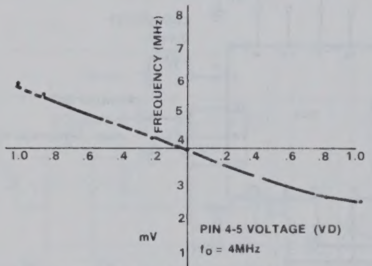

5V
FINE FREQUENCY ADJUSTMENT
I₂
2K
10K
MODULATING INPUT
1kHz
0.47μF
1kHz
1K
0.1μF
564
16
2
11
4
6
7
3
1
5
15
14
13
8
10
9
12
80pF
fo = 5MHz
5V
1K
5V
FREQUENCY SET CAP
MODULATED OUTPUT
(TTL)

Figure 4

VCO CONVERSION GAIN



K_{VCO} = CONVERSION GAIN

$$K_{VCO} = \frac{\Delta f}{\Delta V_D} \simeq -1.8 \frac{MHz}{V}$$

FOR K_O OF PLL MODEL

$$K_O = \frac{(\Delta f/fo)}{VOLT} = \frac{-(1.8MHz/4MHz)}{1VOLT}$$

$$= \frac{-0.45 \text{ RADIANS}}{VOLT}$$

$$= -4.5\times10^{-4} \text{ RADIANS/mV}$$

Figure 5

10.8MHz FSK DECODER USING THE 564

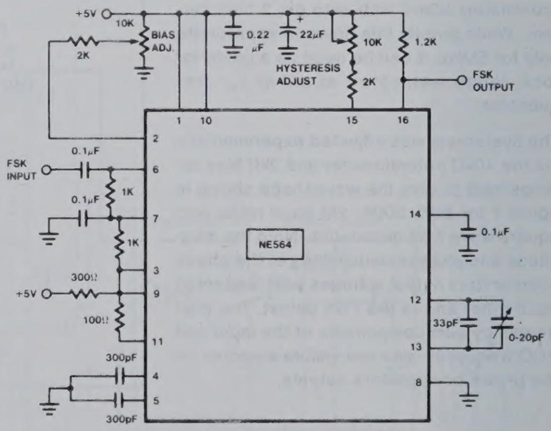
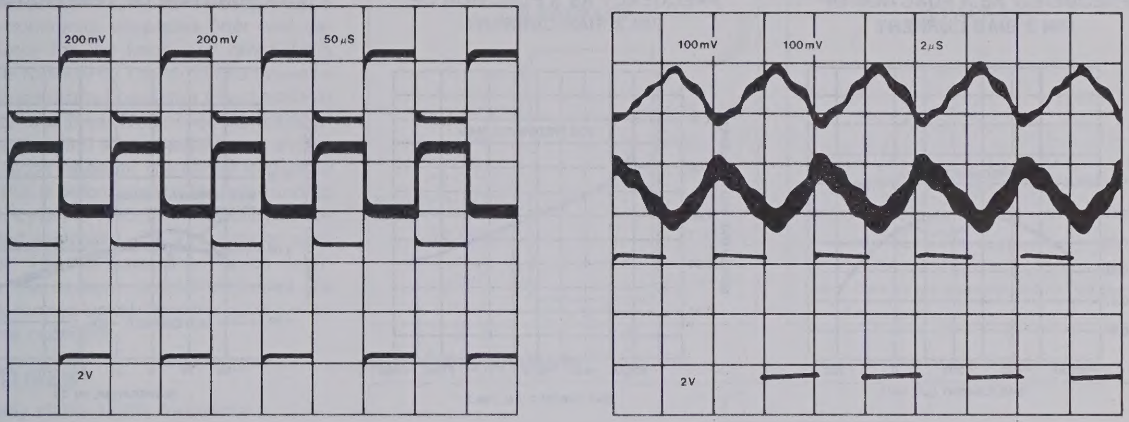
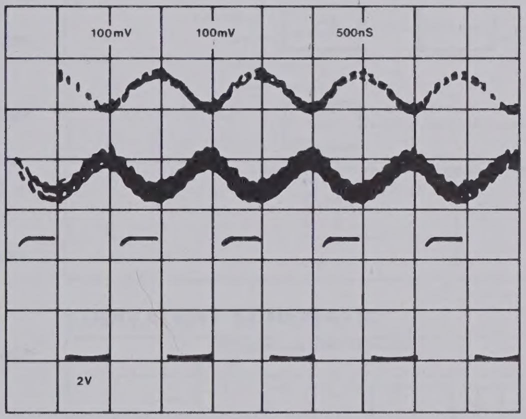

+5V
10K
BIAS ADJ.
2K
0.22 μF
22μF
10K
1.2K
HYSTERESIS ADJUST
2K
FSK OUTPUT
1
10
15
16
2
FSK INPUT
0.1μF
6
1K
0.1μF
7
1K
3
300Ω
+5V
9
100Ω
11
300pF
4
5
300pF
NE564
14
0.1μF
12
33pF
0-20pF
13
8

Figure 6

PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



(a) 20K BAUD (b) 500K BAUD

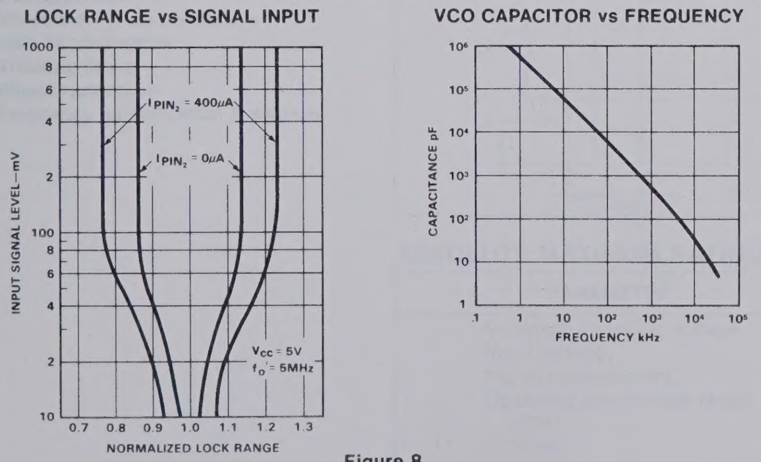


NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

(c) 2.0M BAUD

Figure 7

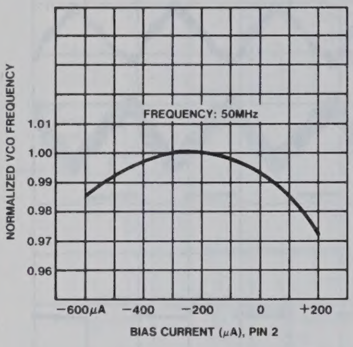
TYPICAL PERFORMANCE CHARACTERISTICS



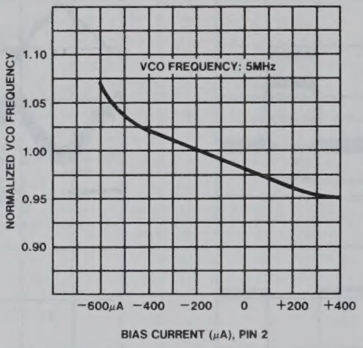
LOCK RANGE vs SIGNAL INPUT

VCO CAPACITOR vs FREQUENCY

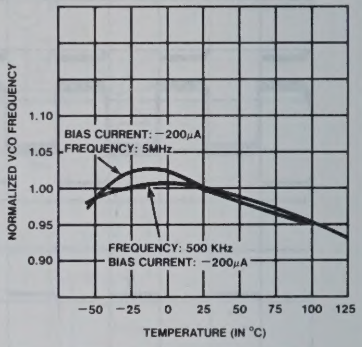
Figure 8



TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE

DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

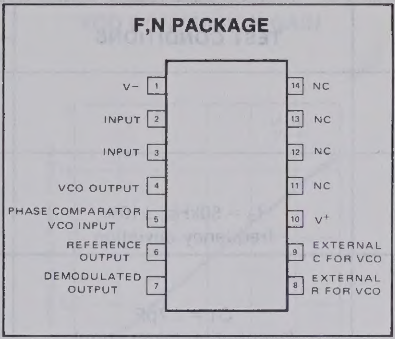
FEATURES

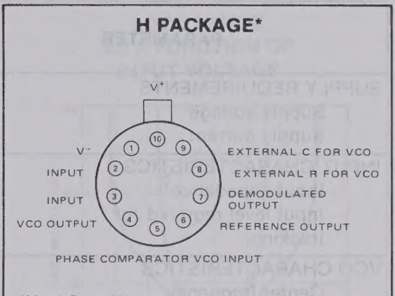
- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (±6 to ±12 volts)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from < ±1% to > ±60%**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wideband FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

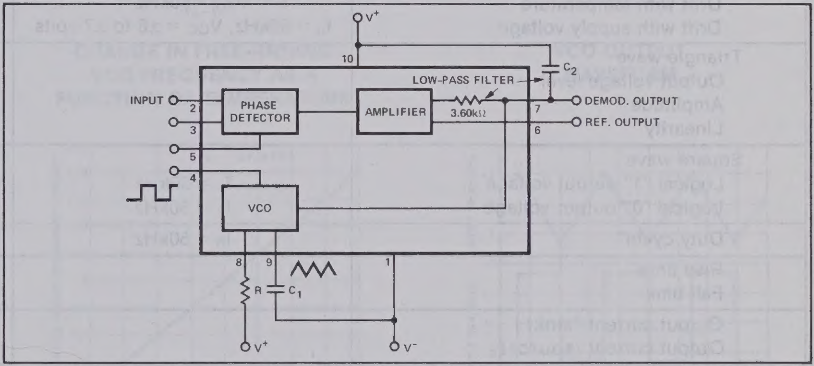
PIN CONFIGURATIONS


F,N PACKAGE
V− 1
INPUT 2
INPUT 3
VCO OUTPUT 4
PHASE COMPARATOR VCO INPUT 5
REFERENCE OUTPUT 6
DEMODULATED OUTPUT 7
14 NC
13 NC
12 NC
11 NC
10 V+
9 EXTERNAL C FOR VCO
8 EXTERNAL R FOR VCO

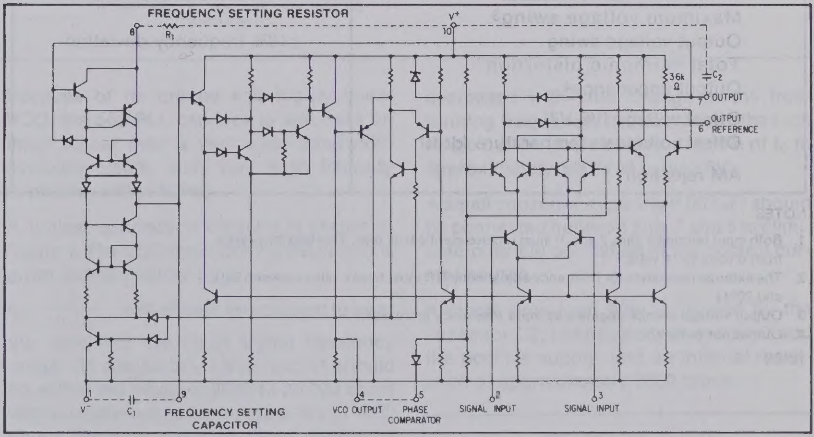

H PACKAGE*
V+
10
V− 1
INPUT 2
INPUT 3
VCO OUTPUT 4
5
PHASE COMPARATOR VCO INPUT
9 EXTERNAL C FOR VCO
8 EXTERNAL R FOR VCO
7 DEMODULATED OUTPUT
6 REFERENCE OUTPUT

*Metal Cans (H) not recommended for new designs

BLOCK DIAGRAM


V+
10
C2
LOW-PASS FILTER
INPUT
2
3
5
4
PHASE DETECTOR
AMPLIFIER
3.60kΩ
7
DEMOD. OUTPUT
6
REF. OUTPUT
VCO
8
9
1
R
C1
V+
V−

EQUIVALENT SCHEMATIC


FREQUENCY SETTING RESISTOR
8
R1
V+
10
3.6k Ω
C2
7 OUTPUT
OUTPUT REFERENCE 6
1
V−
C1
9
FREQUENCY SETTING CAPACITOR
4
VCO OUTPUT
5
PHASE COMPARATOR
2
SIGNAL INPUT
3
SIGNAL INPUT

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	Vp-p
Storage temperature	-65 to +150	°C
Operating temperature range		
NE565	0 to +70	°C
SE565	-55 to +125	°C
Power dissipation	300	mW

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = \pm6V$ unless otherwise specified.

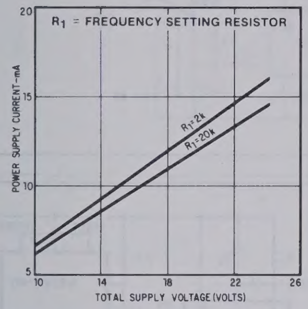
PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
		Min	Typ	Max	Min	Typ	Max	
SUPPLY REQUIREMENTS								
Supply voltage		12		±12	±6		±12	V
Supply current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input impedance[1]		7	10		5	10		kΩ
Input level required for tracking	$f_o = 50kHz$, ±10% frequency deviation	10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center frequency								
Maximum value	$C_1 = 2.7pF$	300	500			500		kHz
Distribution[2]	Distribution taken about $f_o = 50kHz$, $R_1 = 5.0k\Omega$, $C_1 = 1200pF$	-10	0	+10	-30	0	+30	%
Drift with temperature	$f_o = 50kHz$		200			300		ppm/°C
Drift with supply voltage	$f_o = 50kHz$, $V_{CC} = \pm6$ to ±7 volts		0.1	1.0		0.2	1.5	%/V
Triangle wave								
Output voltage level		1.9	0		1.9	0		V
Amplitude			2.4	3		2.4	3	Vp-p
Linearity			0.2			0.5		%
Square wave								
Logical "1" output voltage	$f_o = 50kHz$	+4.9	+5.2		+4.9	+5.2		V
Logical "0" output voltage	$f_o = 50kHz$		-0.2	+0.2		-0.2	+0.2	V
Duty cycle	$f_o = 50kHz$	45	50	55	40	50	60	%
Rise time			20	100		20		ns
Fall time			50	200		50		ns
Output current (sink)		0.6	1		0.6	1		mA
Output current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output voltage level	Measured at pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum voltage swing[3]			2			2		Vp-p
Output voltage swing	±10% frequency deviation	250	300		200	300		mVp-p
Total harmonic distortion			0.2	0.75		0.4	1.5	%
Output impedance[4]			3.6			3.6		kΩ
Offset voltage (V6-V7)			30	100		50	200	mV
Offset voltage vs temperature (drift)			50			100		μV/°C
AM rejection		30	40			40		dB

NOTES

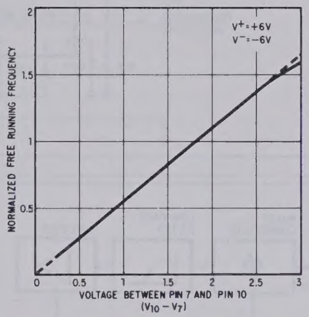
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

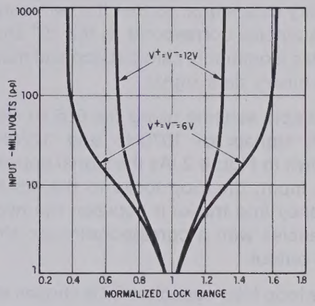
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



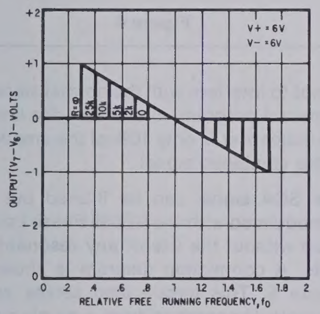
VCO CONVERSION GAIN



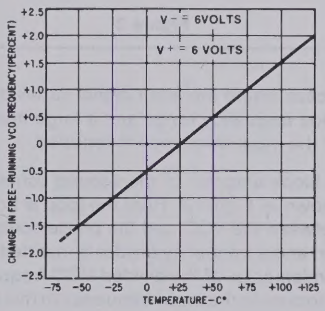
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



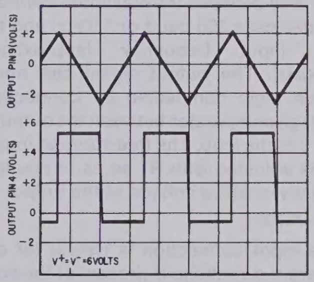
LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6-7)



CHANGE IN FREE-RNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM



DESIGN FORMULAS
(See Figure 1)

Free-running frequency of VCO: $f_o \simeq \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm\frac{8f_o}{V_{CC}}$ in Hz

Capture-range: $f_C \simeq \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6\text{X}10^3)\ \text{X}\ C_2$

TYPICAL APPLICATIONS
FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_o = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

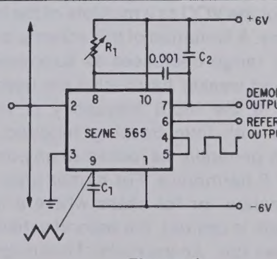


Figure 1

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

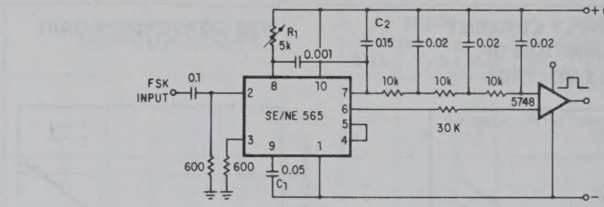


Figure 2

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

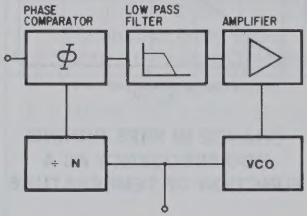


Figure 3

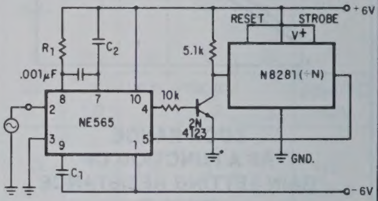


Figure 4

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commerical use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

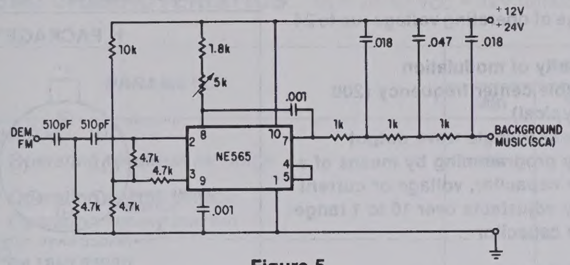

+12V
+24V
10k
1.8k
5k
.018
.047
.018
.001
DEM FM
510pF
510pF
4.7k
4.7k
4.7k
4.7k
NE565
2
8
10
7
4
5
1
3
9
.001
1k
1k
1k
BACKGROUND MUSIC (SCA)

Figure 5

FUNCTION GENERATOR NE/SE566

NE/SE566-F,N,H

DESCRIPTION

The NE/SE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

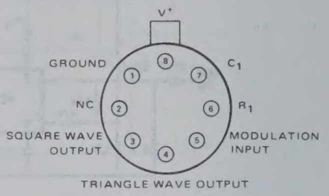
- **Wide range of operating voltage (up to 24 volts)**
- **High linearity of modulation**
- **Highly stable center frequency (200 ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

PIN CONFIGURATIONS

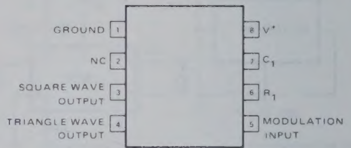
H PACKAGE*


V+
8
GROUND 1
C1 7
NC 2
R1 6
SQUARE WAVE OUTPUT 3
MODULATION INPUT 5
4
TRIANGLE WAVE OUTPUT

ORDER PART NO.
NE/SE566H

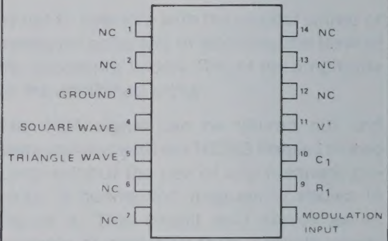
*Metal cans (H) not recommended for new designs

N PACKAGE


GROUND 1
NC 2
SQUARE WAVE OUTPUT 3
TRIANGLE WAVE OUTPUT 4
8 V+
7 C1
6 R1
5 MODULATION INPUT

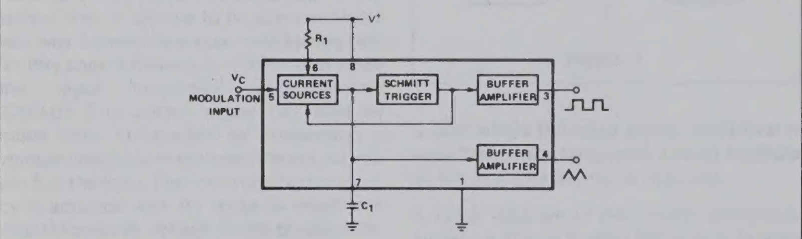
ORDER PART NO.
NE/SE566N

F PACKAGE

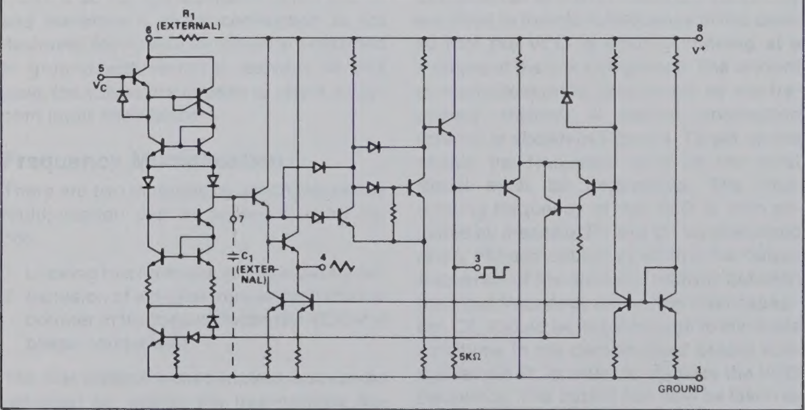

NC 1
NC 2
GROUND 3
SQUARE WAVE 4
TRIANGLE WAVE 5
NC 6
NC 7
14 NC
13 NC
12 NC
11 V+
10 C1
9 R1
MODULATION INPUT

ORDER PART NO.
NE/SE566F

BLOCK DIAGRAM


V+
R1
6
8
VC
MODULATION INPUT
5
CURRENT SOURCES
SCHMITT TRIGGER
BUFFER AMPLIFIER
3
BUFFER AMPLIFIER
4
7
1
C1

EQUIVALENT SCHEMATIC


R1 (EXTERNAL)
6
5
VC
8
V+
7
C1 (EXTERNAL)
4
3
5KΩ
1
GROUND

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V_{P-P}
Storage temperature	-65 to +150	°C
Operating temperature range		
NE566	0 to +70	°C
SE566	-55 to +125	°C
Power dissipation	300	mW

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = 12V$ unless otherwise specified.

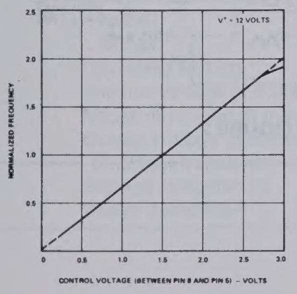
PARAMETER	SE566			NE566			UNIT
	Min	Typ	Max	Min	Typ	Max	
GENERAL							
Operating temperature range	-55		125	0		70	°C
Operating supply voltage			24			24	V
Operating supply current		7	12.5		7	12.5	mA
VCO[1]							
Maximum operating frequency		1			1		MHz
Frequency drift with temperature		200			300		ppm/°C
Frequency drift with supply voltage		1			2		%/V
Control terminal input impedance[2]		1			1		MΩ
FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
Maximum sweep rate		1			1		MHz
Sweep range		10:1			10:1		
OUTPUT							
Triangle wave output							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		Vpp
Linearity		0.2			0.5		%
Square wave input							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		Vpp
Duty Cycle	45	50	55	40	50	60	%
Rise time		20			20		ns
Fall Time		50			50		ns

NOTES

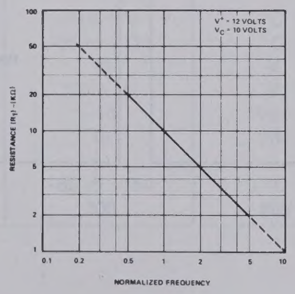
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20KΩ.
2. The bias voltage (V_c) applied to the control terminal (pin 5) should be in the range $3/4V^+ \leq V_c \leq V^+$.

TYPICAL PERFORMANCE CHARACTERISTICS

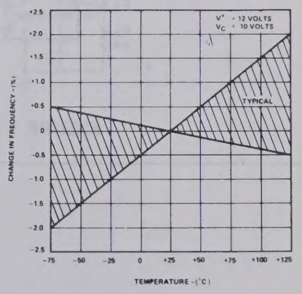
NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R1)

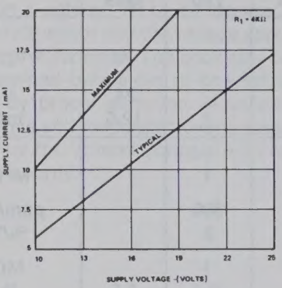


CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE

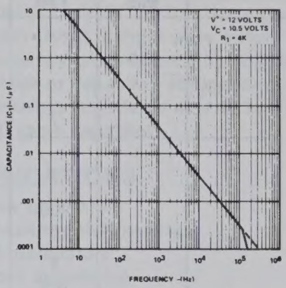


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

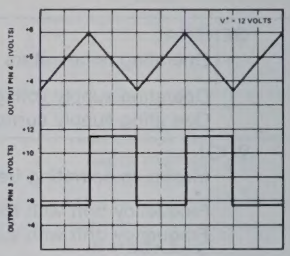
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY AS A FUNCTION OF CAPACITANCE (C1)



VCO OUTPUT WAVEFORMS



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (V_C) in the range

$$3/4\ V^{+} \leq V_C \leq V^{+}$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then ac coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_O \simeq \frac{2[(V^{+}) - (V_C)]}{R_1 C_1 V^{+}}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically 0.001μf) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T^2L gates, which require a current sink of more than 1mA, it is usually necessary to connect a 5kΩ resistor between pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T^2L circuitry which requires a fast fall time (<50ns) and a large current sinking capability.

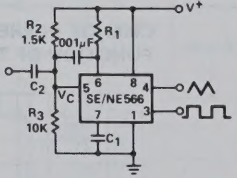


FIGURE 1

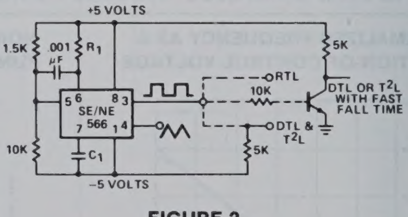


FIGURE 2

TONE DECODER/PHASE LOCKED LOOP — NE/SE567

NE/SE567-F,N,H

DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

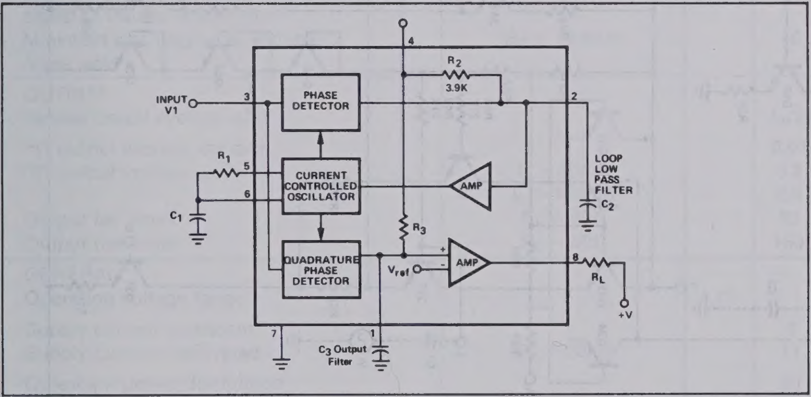
FEATURES

- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14 percent)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20 to 1 range with an external resistor**
- **Military processing available**

APPLICATIONS

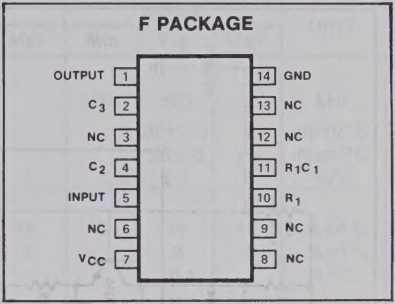
- **Touch Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

BLOCK DIAGRAM

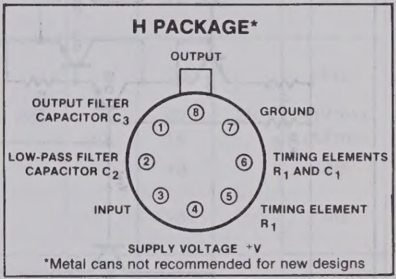


INPUT V1
3
PHASE DETECTOR
4
R2
3.9K
2
LOOP LOW PASS FILTER
C2
R1
5
6
C1
CURRENT CONTROLLED OSCILLATOR
AMP
R3
QUADRATURE PHASE DETECTOR
Vref
+
-
AMP
8
RL
+V
7
1
C3 Output Filter

PIN CONFIGURATIONS

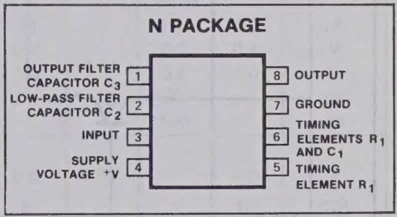


F PACKAGE
OUTPUT 1
C3 2
NC 3
C2 4
INPUT 5
NC 6
VCC 7
14 GND
13 NC
12 NC
11 R1C1
10 R1
9 NC
8 NC



H PACKAGE*
OUTPUT
OUTPUT FILTER CAPACITOR C3
GROUND
LOW-PASS FILTER CAPACITOR C2
TIMING ELEMENTS R1 AND C1
INPUT
TIMING ELEMENT R1
SUPPLY VOLTAGE +V
1
2
3
4
5
6
7
8

*Metal cans not recommended for new designs

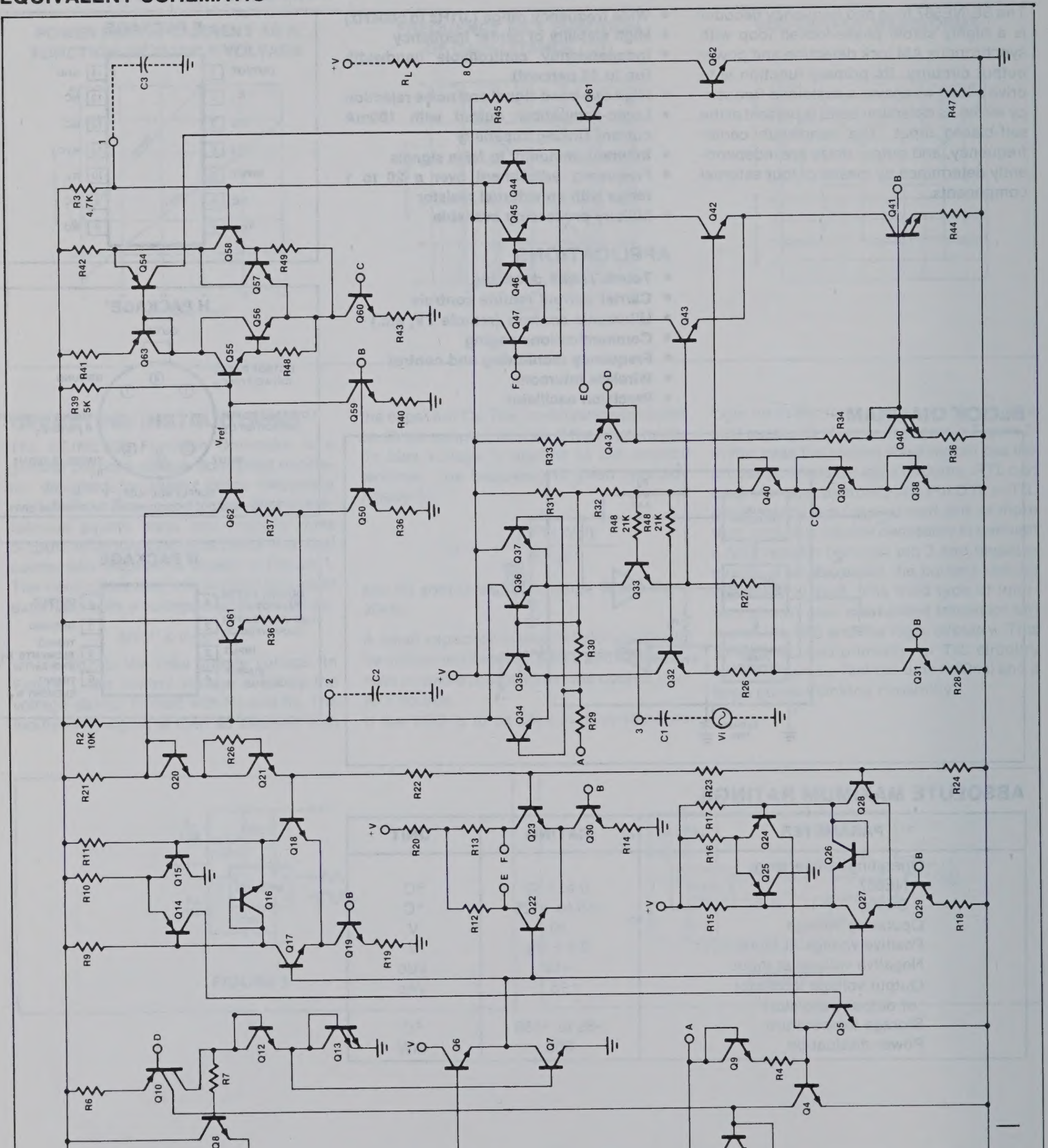


N PACKAGE
OUTPUT FILTER CAPACITOR C3 1
LOW-PASS FILTER CAPACITOR C2 2
INPUT 3
SUPPLY VOLTAGE +V 4
8 OUTPUT
7 GROUND
6 TIMING ELEMENTS R1 AND C1
5 TIMING ELEMENT R1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature		
NE567	0 to +70	°C
SE567	-55 to +125	°C
Operating voltage	10	V
Positive voltage at input	0.5 + V_S	V
Negative voltage at input	-10	Vdc
Output voltage (collector of output transistor)	15	Vdc
Storage temperature	-65 to +150	°C
Power dissipation	300	mW

EQUIVALENT SCHEMATIC


+V
RL
8
Q62
R47
Q61
R45
C3
1
R3
4.7K
Q44
Q45
Q42
Q41
R44
R42
Q54
Q58
Q57
R49
Q46
C
Q60
R43
Q47
Q43
Q63
Q56
Q55
R48
R41
R39
5K
B
Q59
R40
F
E
D
Vref
R33
R34
Q40
R36
Q62
R37
Q50
R36
R31
R32
R48
21K
Q40
Q30
Q38
Q37
Q33
R27
Q36
Q61
R36
R30
Q35
Q32
R26
Q31
R28
2
C2
Q34
R29
A
3
C1
Vi
R2
10K
R26
Q20
Q21
R21
R22
R23
R24
Q23
Q30
R14
R17
Q24
Q28
R20
R13
R16
Q26
R11
Q15
Q18
Q25
R10
Q16
Q14
Q19
R19
R12
Q22
R15
Q27
Q29
R18
R9
Q17
Q5
Q12
Q13
Q6
Q7
-V
Q9
R4
R7
Q10
R6
Q4
Q8
Q3
R5
Q1
Q2
4
5
R1
6
7

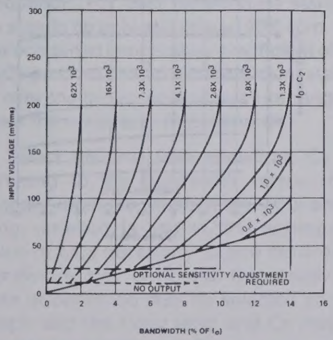
DC ELECTRICAL CHARACTERISTICS (V+ = 5.0V; T_A = 25°C unless otherwise specified.)

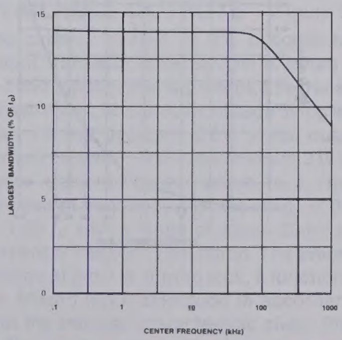
PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
		Min	Typ	Max	Min	Typ	Max	
CENTER FREQUENCY[1]								
Highest center frequency (f_o)		100	500		100	500		kHz
Center frequency stability[2]	-55 to +125°C		35±140			35±140		ppm/°C
	0 to +70°C		35±60			35±60		ppm/°C
Center frequency shift with supply voltage	f_o = 100kHz		0.5	1		0.7	2	%/V
DETECTION BANDWIDTH								
Largest detection bandwidth	f_o = 100kHz	12	14	16	10	14	18	% of f_o
Largest detection bandwidth skew			2	4		3	6	% of f_o
Largest detection bandwidth—variation with temperature	V_i = 300mVrms		±0.1			±0.1		%/°C
Largest detection bandwidth—variation with supply voltage	V_i = 300mVrms		±2			±2		%/V
INPUT								
Input resistance			20			20		kΩ
Smallest detectable input voltage (V_i)	I_L = 100mA, $f_i = f_o$		20	25		20	25	mVrms
Largest no-output input voltage	I_L = 100mA, $f_i = f_o$	10	15		10	15		mVrms
Greatest simultaneous outband signal to inband signal ratio			+6			+6		dB
Minimum input signal to wideband noise ratio	B_n = 140kHz		-6			-6		dB
OUTPUT								
Fastest on-off cycling rate			$f_o/20$			$f_o/20$		
"1" output leakage current			0.01	25		0.01	25	μA
"0" output voltage	I_L = 30mA		0.2	0.4		0.2	0.4	V
	I_L = 100mA		0.6	1.0		0.6	1.0	V
Output fall time[3]	R_L = 50Ω		30			30		ns
Output rise time[3]	R_L = 50Ω		150			150		ns
GENERAL								
Operating voltage range		4.75		9.0	4.75		9.0	V
Supply current quiescent			6	8		7	10	mA
Supply current—activated	R_L = 20kΩ		11	13		12	15	mA
Quiescent power dissipation			30			35		mW

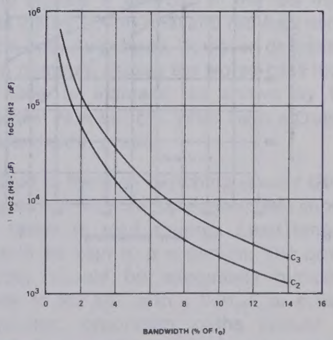
NOTES

1. Frequency determining resistor R_1 should be between 1 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

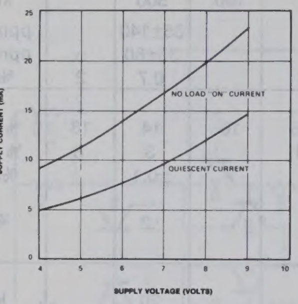
TYPICAL PERFORMANCE CHARACTERISTICS

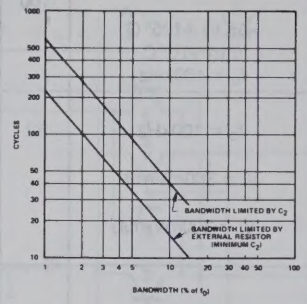

BANDWIDTH vs INPUT SIGNAL AMPLITUDE

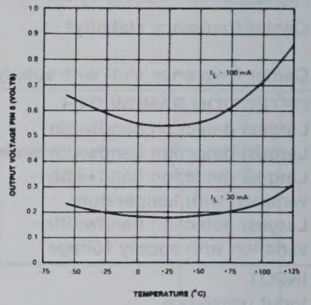

LARGEST DETECTION BANDWIDTH vs OPERATING FREQUENCY

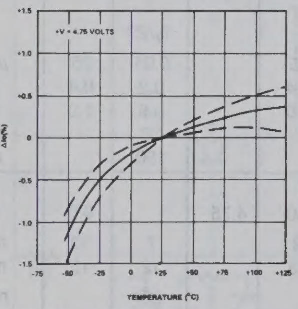

DETECTION BANDWIDTH AS A FUNCTION OF C2 and C3

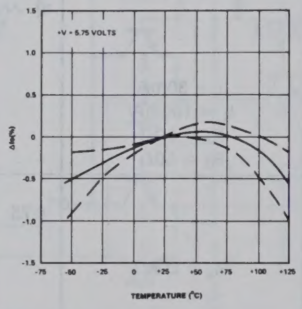
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

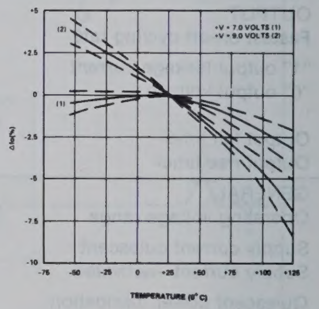

TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE

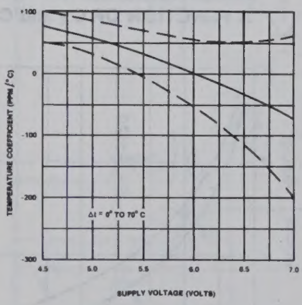

GREATEST NUMBER OF CYCLES BEFORE OUTPUT

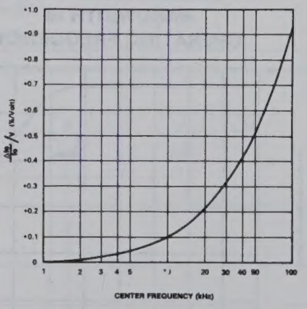

TYPICAL OUTPUT VOLTAGE vs TEMPERATURE

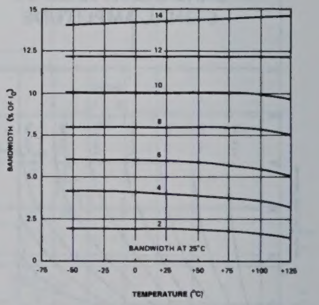

TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)


TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)


TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)


CENTER FREQUENCY TEMPERATURE COEFFICIENT (MEAN AND S.D.)


CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE vs OPERATING FREQUENCY


TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE

DESIGN FORMULAS

$$f_0 \approx \frac{1.1}{R_1C_1}$$

$$BW \approx 1070\sqrt{\frac{V_i}{f_0C_2}} \text{ in \% of } f_0, V_i \leq 200\text{mVrms}$$

Where

V_i = Input Voltage (Vrms)
C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (fo)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/2f_0$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

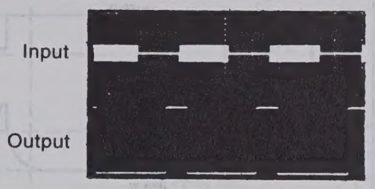
OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

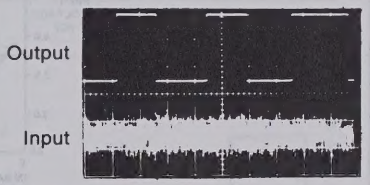
1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_0C_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_0C_2 product (f_0 (Hz), C_2 (μ fd)).

TYPICAL RESPONSE



Response to 100mVrms tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = -6db R_L = 100 ohms
Noise Bandwidth = 140Hz

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to elminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to translent frequencies.) A typical minimum value for C_3 is $2C_2$.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_0 with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{be}) \approx (+V - 1.4V)$ having a dc average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

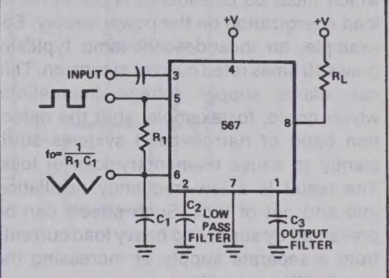


Figure 1

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_0/3$, $f_0/5$, etc.

2. The 567 will lock onto signals near $(2n + 1)\,f_0$, and will give an output for signals near $(4n + 1)\,f_0$ where n = 0, 1, 2, etc. Thus, signals at $5f_0$ and $9f_0$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and

unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmiter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

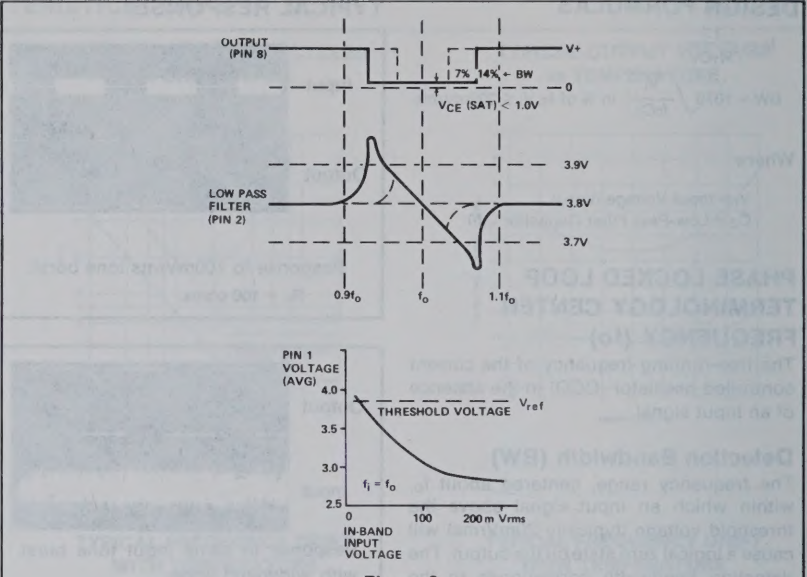


Figure 2

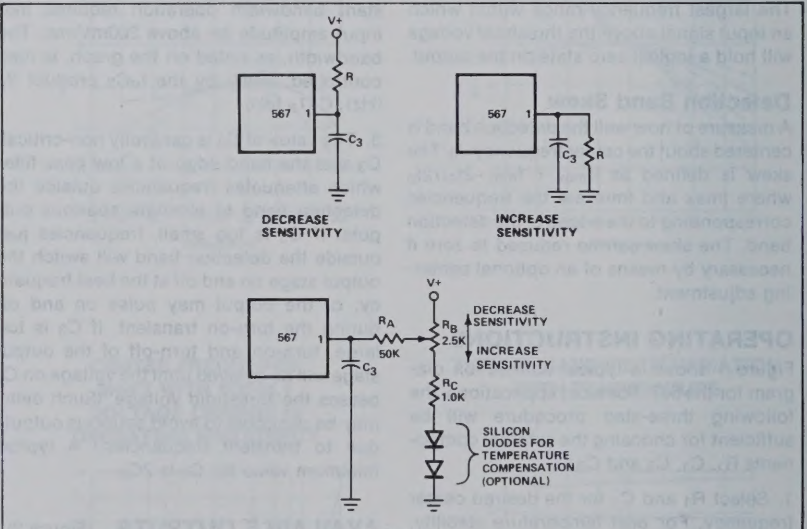


Figure 3

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

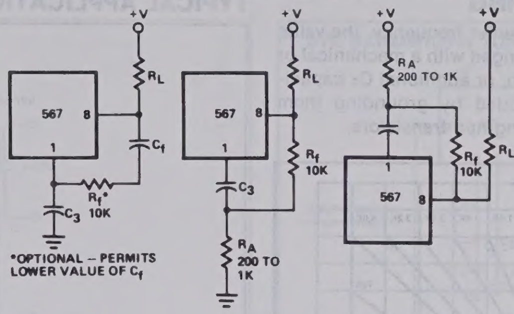


Figure 4

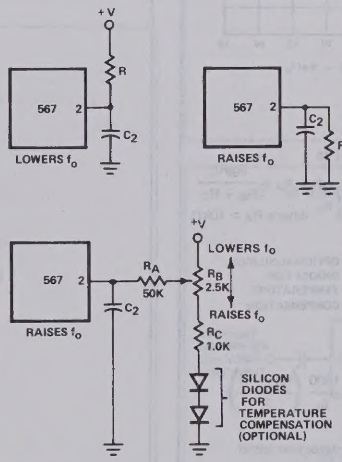


Figure 5

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

REDUCTION OF C1 VALUE

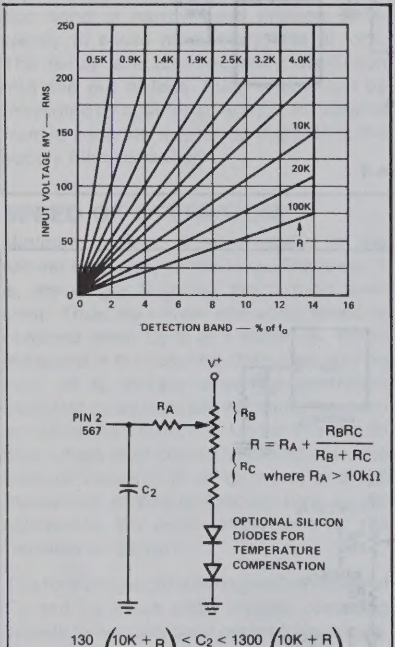
(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

14

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.



$$\frac{130}{f_o}\left(\frac{10K + R}{R}\right) < C_2 < \frac{1300}{f_o}\left(\frac{10K + R}{R}\right)$$

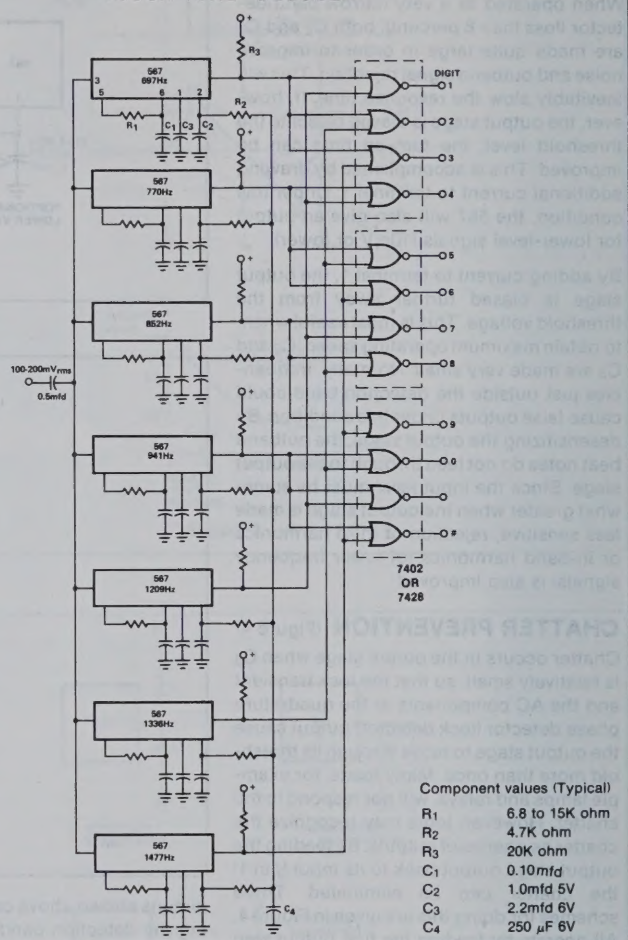
NOTE

Adjust control for symmetry of detection band edges about f_o.

Figure 6

TYPICAL APPLICATIONS

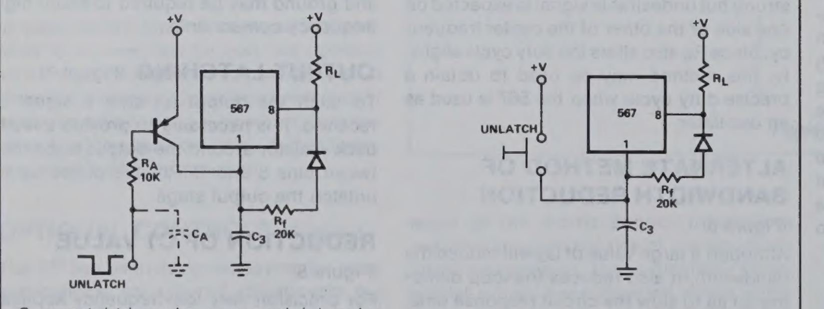
TOUCH-TONE® DECODER


+
R3
567 697Hz
3 5 6 1 2
R1
C1 C3 C2
R2
DIGIT
1
2
3
4
5
6
7
8
9
0
#
567 770Hz
567 852Hz
100-200mVrms
0.5mfd
567 941Hz
567 1209Hz
567 1336Hz
567 1477Hz
C4
7402 OR 7426

Component values (Typical)

R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10mfd
C_2	1.0mfd 5V
C_3	2.2mfd 6V
C_4	250 μF 6V

OUTPUT LATCHING


+V
+V
RL
567
8
1
RA 10K
Rf 20K
CA
C3
UNLATCH
+V
+V
RL
567
8
1
UNLATCH
Rf 20K
C3

CA prevents latch-up when power supply is turned on.

Figure 7

PRECISION VLF

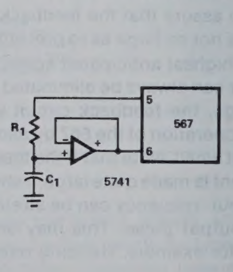
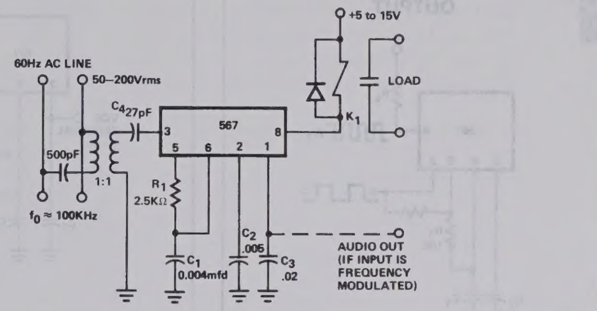

+V
RL
R1
5
567
6
C1
5741

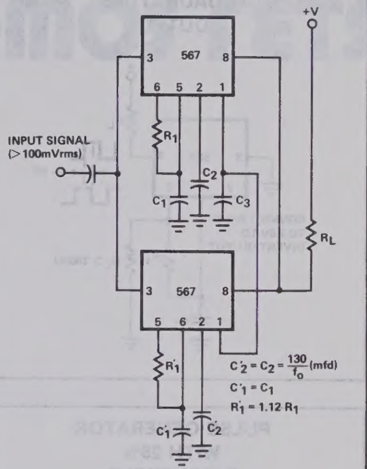
Figure 8

TYPICAL APPLICATIONS (Cont'd)

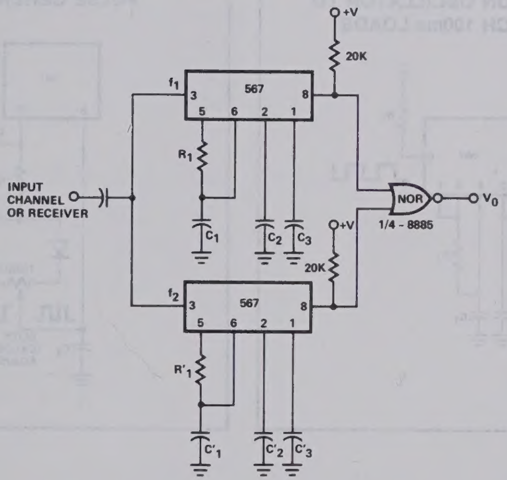
CARRIER-CURRENT REMOTE CONTROL OR INTERCOM


+5 to 15V
LOAD
K1
60Hz AC LINE
50–200Vrms
C4 27pF
567
3
8
5
6
2
1
500pF
1:1
f0 ≈ 100KHz
R1 2.5KΩ
C2 .005
C1 0.004mfd
C3 .02
AUDIO OUT (IF INPUT IS FREQUENCY MODULATED)

24% BANDWIDTH TONE DECODER

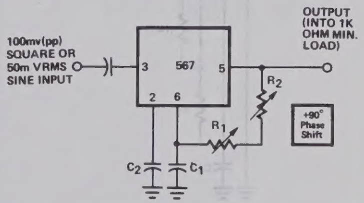

+V
567
3
8
6
5
2
1
INPUT SIGNAL (>100mVrms)
R1
C1
C2
C3
RL
567
3
8
5
6
2
1
R'1
C'1
C'2
C'2 = C2 = 130/fo (mfd)
C'1 = C1
R'1 = 1.12 R1

DUAL-TONE DECODER


+V
20K
f1
567
3
8
5
6
2
1
R1
C1
C2
C3
INPUT CHANNEL OR RECEIVER
NOR
V0
1/4 - 8885
+V
20K
f2
567
3
8
5
6
2
1
R'1
C'1
C'2
C'3

1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

0° to 180° PHASE SHIFTER

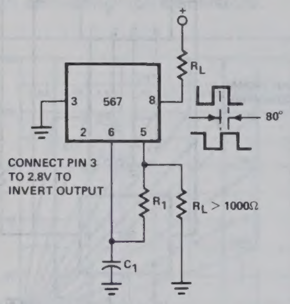

100mv(pp) SQUARE OR 50m VRMS SINE INPUT
567
3
5
2
6
OUTPUT (INTO 1K OHM MIN. LOAD)
R2
R1
+90° Phase Shift
C2
C1

$R_2 \approx R_1/5$

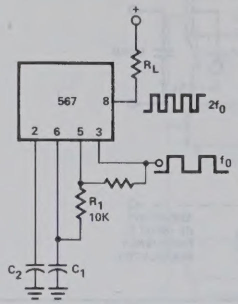
Adjust R_1 so that ϕ = 90° with control midway

TYPICAL APPLICATIONS (Cont'd)

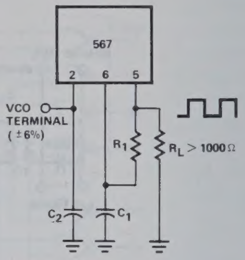
OSCILLATOR WITH QUADRATURE OUTPUT


+
R_L
567
3
8
2
6
5
80°
CONNECT PIN 3 TO 2.8V TO INVERT OUTPUT
R_1
$R_L > 1000\Omega$
C_1

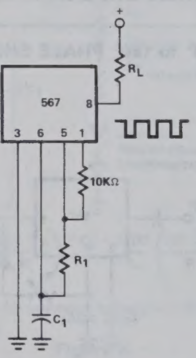
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT


+
R_L
567
8
$2f_0$
2
6
5
3
f_0
R_1
10K
C_2
C_1

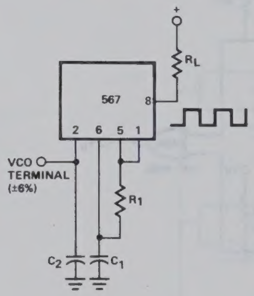
PRECISION OSCILLATOR WITH 20ns SWITCHING


567
2
6
5
VCO TERMINAL (±6%)
R_1
$R_L > 1000\Omega$
C_2
C_1

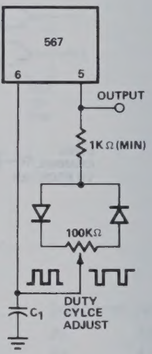
PULSE GENERATOR WITH 25% DUTY CYCLE


+
R_L
567
8
3
6
5
1
10KΩ
R_1
C_1

PRECISION OSCILLATOR TO SWITCH 100ma LOADS


+
R_L
567
8
2
6
5
1
VCO TERMINAL (±6%)
R_1
C_2
C_1

PULSE GENERATOR


567
6
5
OUTPUT
1K Ω (MIN)
100KΩ
C_1
DUTY CYLCE ADJUST

NOTE

Application information available on request.

SECTION 15
D-MOS FETS

Section 15—D-MOS

SD210/211/212/213/214/215 D-MOS FET Switch N-Channel Enhancement 463
SD300/303/304 D-MOS FET Dual Gate N-Channel Enhancement 468
SD305/306 D-MOS FET Dual Gate N-Channel Enhancement 475
SD5000/5001/5002 D-MOS FET Quad Analog Switch Arrays and Multiplexers 484

D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

SD210/SD211
SD212/SD213/SD214/SD215

SD210/211/212/213/214/215-EE

DESCRIPTION

The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of -0.3V to +30V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for ±10V switch driver applications. Other characteristics allow them to be used as ±5V switches. The SD214 and 215 are designed to switch signals up to ±10V and the SD212 and 213 are designed to switch signals up to ±5V.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

FEATURES

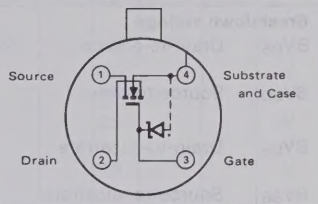
- **Low feedback capacitance: 0.30pF**
- **Low drain node capacitance: 1.3pF**
- **Low gate node capacitance: 2.4pF**
- **Low feedthrough and feedback transients**
- **Ion-implanted for greater reliability**
- **Excellent isolation from input to output: -120dB**
- **35V drain-to-source voltage for SD210/211**
- **Military qualifications pending**

APPLICATIONS

- **Switch driver**
- **Analog switch**
- **Multiplexers**
- **Digital switch**
- **Sample and hold**
- **Choppers**
- **A-TO-D converters**
- **D-TO-A converters**

PIN CONFIGURATION (Top View)

EE PACKAGE

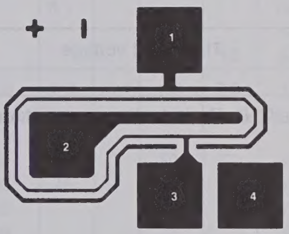


*Diode protection on SD 211/213/215 only.

ORDER PART NO.

SD210EE, SD211EE, SD212EE
SD213EE, SD214EE, SD215EE

CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	SOURCE
2	DRAIN
3	GATE
4	DIODE

Die size 19X22

For SD211, 213, 215 bond gate and diode to same point.

ABSOLUTE MAXIMUM RATINGS (all devices)

PARAMETER	RATING	UNIT
Drain current (I_D)	50	mA
Ambient temperature range		
Storage	-65 to +175	°C
Operating	-55 to +125	°C
Transistor dissipation (P_T)		
At 25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
At 25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.*

PARAMETER		SD210	SD211	SD212	SD213	SD214	SD215	UNIT
V_{DS}	Drain-to-source	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+30	+15	+15	+25	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	Gate-to-source	±40	-15 +25	±40	-15 +25	±40	-25 +30	Vdc
V_{GB}	Gate-to-substrate	±40	-0.3 +25	±40	-0.3 +25	±40	-0.3 +30	Vdc
V_{GD}	Gate-to-drain	±40	-30 +25	±40	-15 +25	±40	-25 +30	Vdc

*NOTE

Refer to test conditions specified in Electrical Characteristics Table.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD210			SD211			SD212			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage												
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$	30	35		30	35					V
		$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		10	25		10	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			10			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			15			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			15			V
Leakage current												
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$		1	10		1	10		1	10	nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$		1	10		1	10		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = \pm 40V$			0.1						0.1	nA
		$V_{GB} = +25V$						10				μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.5	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$										
		$V_{GS} = +5V$		50	70		50	70		50	70	Ω
		$V_{GS} = +10V$		30	45		30	45		30	45	Ω
		$V_{GS} = +15V$		23			23			23		Ω
		$V_{GS} = +20V$		19			19			19		Ω
		$V_{GS} = +25V$		17						17		Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25\,°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD213			SD214			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage												
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		20	25		20	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			20			20			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			25			25			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			25			25			V
Leakage current												
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$										
		$V_{DS} = +10V$		1	10							nA
		$V_{DS} = +20V$					1	10		1	10	nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$										
		$V_{SD} = +10V$		1	10							nA
		$V_{SD} = +20V$					1	10		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$										
		$V_{GB} = \pm 40V$						0.1				nA
		$V_{GB} = +25V$			10							μA
		$V_{GB} = +30V$									10	μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$										
		$V_{GS} = +5V$		50	70		50	70		50	70	Ω
		$V_{GS} = +10V$		30	45		30	45		30	45	Ω
		$V_{GS} = +15V$		23			23			23		Ω
		$V_{GS} = +20V$		19			19			19		Ω
		$V_{GS} = +25V$					17			17		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25\,°C$ unless otherwise specified.

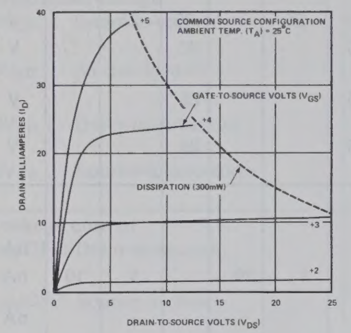
PARAMETER		TEST CONDITIONS	SD210			SD211			SD212			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										
$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25\,°C$ unless otherwise specified.

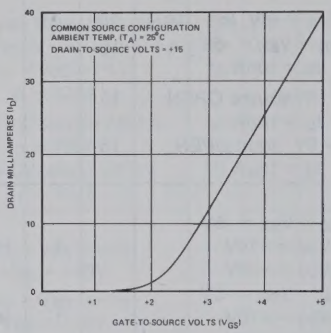
PARAMETER		TEST CONDITIONS	SD213			SD214			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										
$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

TYPICAL PERFORMANCE CHARACTERISTICS

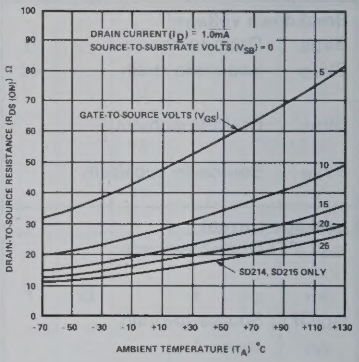
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



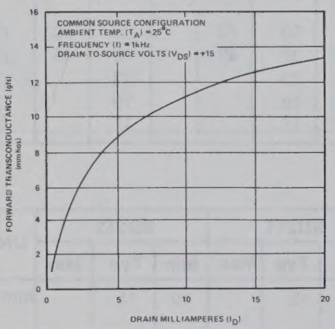
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



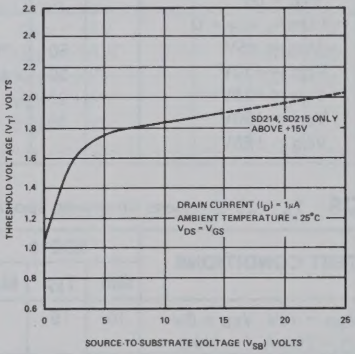
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



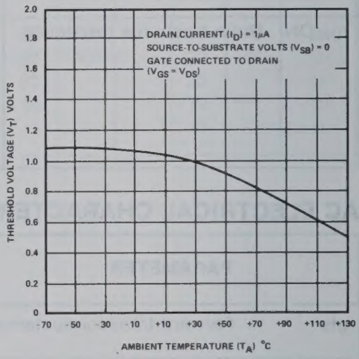
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



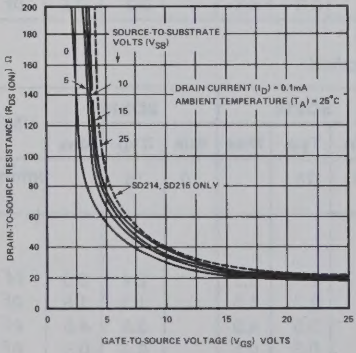
THRESHOLD VOLTAGE vs SOURCE-TO-SUBSTRATE VOLTAGE



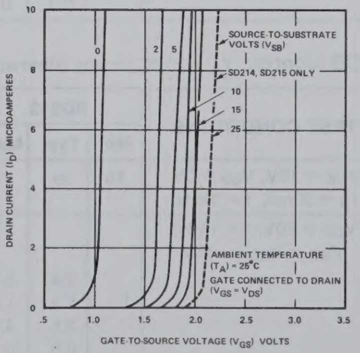
THRESHOLD VOLTAGE vs TEMPERATURE



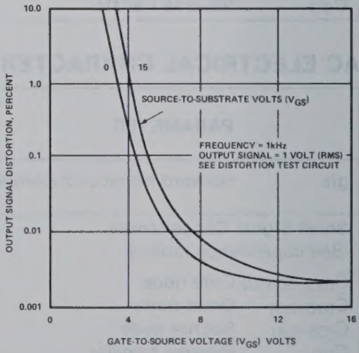
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

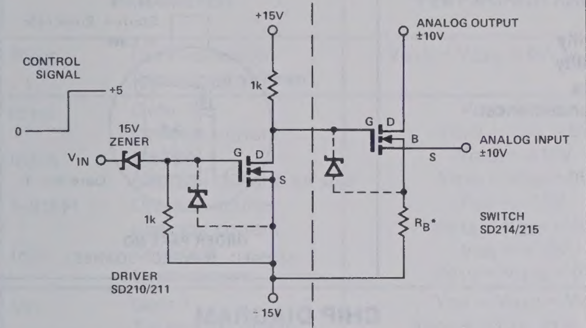


DISTORTION vs GATE-TO-SOURCE VOLTAGE



TYPICAL APPLICATION

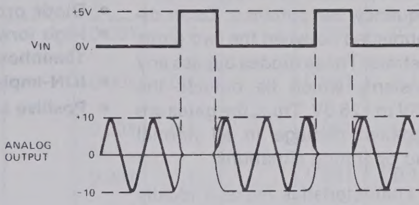
D-MOS DRIVER/SWITCH


+15V
ANALOG OUTPUT
±10V
CONTROL
SIGNAL
+5
0
1k
15V
ZENER
V_{IN}
G
D
S
G
D
B
S
ANALOG INPUT
±10V
1k
R_B*
SWITCH
SD214/215
DRIVER
SD210/211
-15V

R_B*Optional current limiting resistor

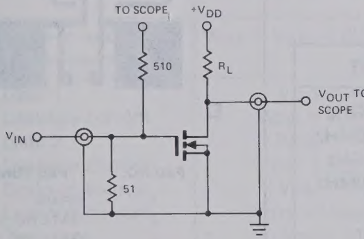
NOTE
*All resistors standard and are measured in ohms.

TYPICAL SWITCHING WAVEFORM



TEST CIRCUITS

SWITCHING

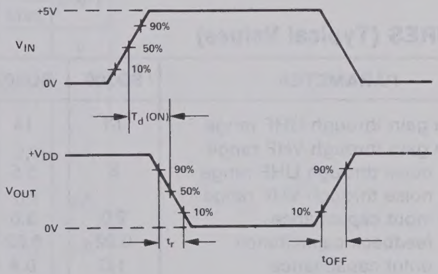

TO SCOPE
$+V_{DD}$
510
R_L
V_{OUT} TO
SCOPE
V_{IN}
51

Input pulse: t_d, t_r < 1ns,
Pulse width = 100ns,
Rep rate = 1MHz

SAMPLING SCOPE

t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

TYPICAL SWITCHING WAVEFORM

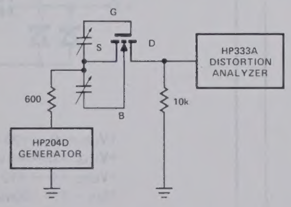


SWITCHING CHARACTERISTICS

		t_d(ON) (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

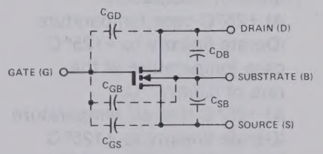
*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

DISTORTION


G
S
D
HP333A
DISTORTION
ANALYZER
600
B
10k
HP204D
GENERATOR

NOTE: All resistors standard and are measured in ohms.

CAPACITANCE MODEL


C_{GD}
DRAIN (D)
C_{DB}
GATE (G)
SUBSTRATE (B)
C_{GB}
C_{SB}
SOURCE (S)
C_{GS}

D-MOS FET DUAL GATE N-CHANNEL ENHANCEMENT — SD300/303/304

SD300/303-EC
SD304-EE

DESCRIPTION

The Signetics D-MOS SD300/303/304 are silicon, dual-insulated-gate, field effect transistor of the N-channel enhancement mode type. It is fabricated by the Signetics double-diffused process which gives superior high frequency performance. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +25.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The device characteristics make it ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (Crss) low. A wide AGC capability plus a significant reduction in cross-modulation distortion is now available because of the inherent linearity of these devices. The SD300/303/304 are hermetically sealed in a modified 4-lead TO-72 package.

GENERAL FEATURES

- **Lower cross-modulation and wider dynamic range than bipolar or single gate FETs**
- **Reverse AGC capability**
- **Linear mixing capability**
- **Diode protected gates**
- **High forward transconductance: 10mmhos**
- **ION-implanted**
- **Positive bias only**

FEATURES (Typical Values)

PARAMETER	SD300	SD303	SD304	UNIT
High gain through UHF range	13	14		dB at 1GHz
High gain through VHF range			16	dB at 500MHz
Low noise through UHF range	8	5.5		dB at 1GHz
Low noise through VHF range			5	dB at 500MHz
Low input capacitance	2.0	3.0	2.5	pF
Low feedback capacitance	0.02	0.02	0.03	pF
Low outut capacitance	1.0	0.6	1.0	pF

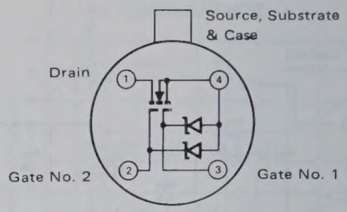
ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source		
	SD300/304	+25	V
	SD303	+20	V
V_{G1B}	DC gate no. 1-to-substrate voltage	-0.3, +10	V
V_{G2B}	DC gate no. 2-to-substrate voltage	-0.3, +15	V
I_D	Drain current	50	mA
T_A	Ambient temperature range		
	Storage	-65 to +175	°C
	Operating	-55 to +125	°C
P_T	Transistor dissipation		
	At +25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
	At +25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

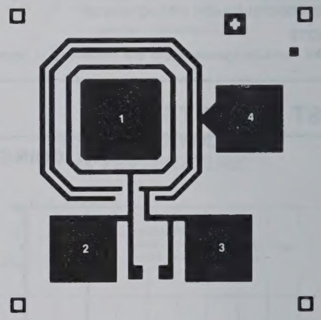
PIN CONFIGURATIONS (Top View)

EC, EE PACKAGE



ORDER PART NO.
SD300EC SD303EC SD304EE

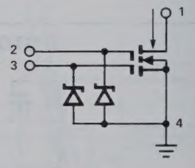
CHIP DIAGRAM



PAD NO.	PAD FUNCTION
1	DRAIN
2	GATE NO. 2
3	GATE NO. 1
4	SOURCE

Die Size 20X20

DUAL GATE CASCODE BIAS SCHEME



$+V_{DS} = 0 \rightarrow +20$ volts
$+V_{G1S} = 0 \rightarrow +4$ volts
$+V_{G2S} = 0 \rightarrow +10$ volts
$+I_{DS} = 0 \rightarrow +20mA$

SD300/303-EC
SD304-EE

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD300			SD303			UNIT
			Min	Typ	Max	Min	Typ	Max	
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	25	30		20	25		V
I_{G1SS}	Gate 1 Leakage current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	µA
I_{G2SS}	Gate 2 Leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	µA
$I_D(OFF)$	Drain-to-source Leakage current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	0.1		0.001	0.1	µA
I_{DSS}	Zero bias Drain current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	0.1		0.001	0.1	µA
V_{T1}	Gate 1 Threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$ $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2}	Gate 2 Threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +4V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
r_{DS} (ON)	Drain-to-source On resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		90	130		65	80	Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD304			UNIT
			Min	Typ	Max	
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	25	30		V
I_{G1SS}	Gate 1 Leakage current	$V_{G1S} = +5V$, $V_{G2S} = V_{DC} = 0V$		0.001	0.1	µA
I_{G2SS}	Gate 2 Leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1	µA
$I_D(OFF)$	Drain-to-source Leakage current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	0.1	µA
I_{DSS}	Zero bias Drain current	$V_{DS} = +15V$ $v_{G1S} = V_{G2S} = 0V$		0.001	0.1	µA
V_{T1}	Gate 1 Threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$ $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	V
V_{T2}	Gate 2 Threshold voltage	$V_{DS} = V_{G2S} = T_{T2}$, $V_{G1S} = +4V$, $I_D = 1\mu A$	0.1	1.0	2.0	V
r_{DS}(ON)	Drain-to-source On resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		90	130	Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD300			SD303			SD304			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Small signal short circuit Capacitances	f = 1MHz, Gate 2 AC grounded										
C_{iss}	Input	$V_{DS} = +15V$, $V_{G1S} \cong 3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$		2.0	2.5					2.5	3.0	pF
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$					3.0	3.5				pF
C_{oss}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		1.0	1.2		0.6			1.0	1.2	pF
C_{rss}	Reverse transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.02			0.02			0.03		pF
gfs	Forward transconductance	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1kHz	8.0	10.0					8.0	10.0		mmhos
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$				13.0	15.0					mmhos
Gps	Power gain	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$										
		f = 1GHz	9.0	13.0*								dB
		f = 500MHz							13.0	16.0		dB
		f = 200MHz	22.0	24.0								dB
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1GHz				10.0	14.0*					dB
NF	Noise figure	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$										
		f = 1GHz		8.0*	9.0							dB
		f = 500MHz								5.0	6.0	dB
		f = 200MHz		3.0	4.0							
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1GHz					5.5*	7.0				dB
E_{int}	Interfering signal level at gate for 1% cross-modulation distortion. Peak voltage referenced to 300Ω system.	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, Desired signal f = 500MHz, Undersired signal f = 501MHz			200					200		mV
		$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, Wanted Signal f = 1GHz, Interfering signal f = 0.995GHz					150					mV
AGC (V_{G2S})	Range of automatic Gain control	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, f = 500MHz		40						40		dB
		$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, f = 500MHz					40					dB

*NOTE

Measured in amplifier test fixture.

SD300/303-EC
SD304-EE

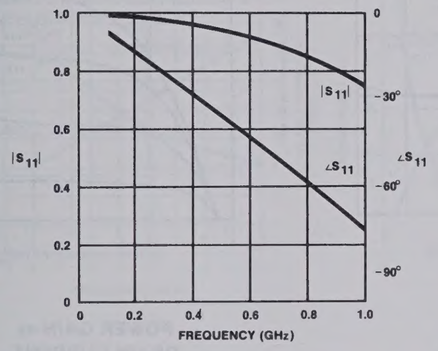
SD300 TYPICAL PERFORMANCE CHARACTERISTICS

SD300 "S" PARAMETERS

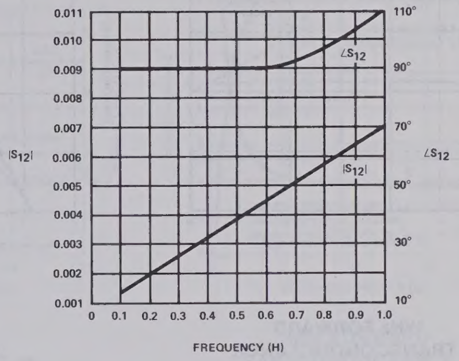
AMBIENT TEMP. (TA) = +25°C
DRAIN MILLIAMPERES (ID) = 18

DRAIN-TO-SOURCE VOLTS (VDS) = +15
GATE NO. 1-TO-SOURCE VOLTS (VG1S) ≃ +3.5
GATE NO. 2-TO-SOURCE VOLTS (VG2S) = +10

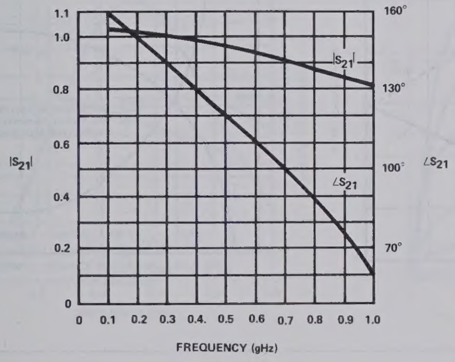
S_{11}



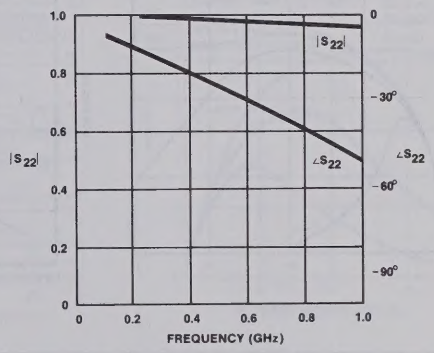
S_{12}



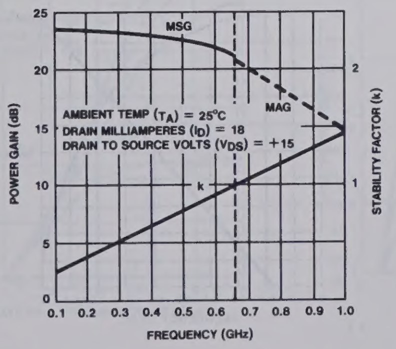
S_{21}



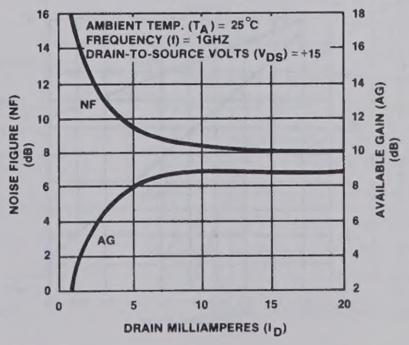
S_{22}



POWER GAIN vs FREQUENCY



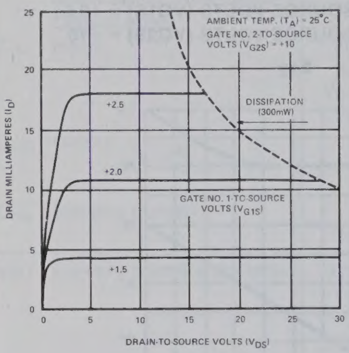
NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



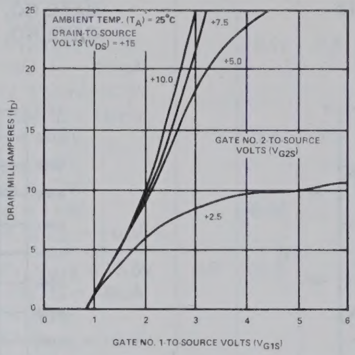
SD300/303-EC
SD304-EE

SD303 TYPICAL PERFORMANCE CHARACTERISTICS

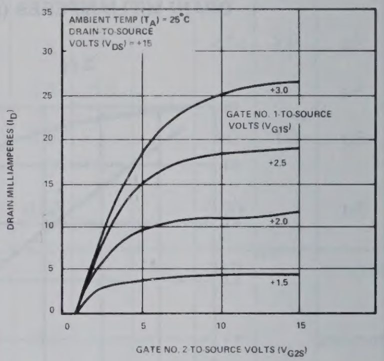
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



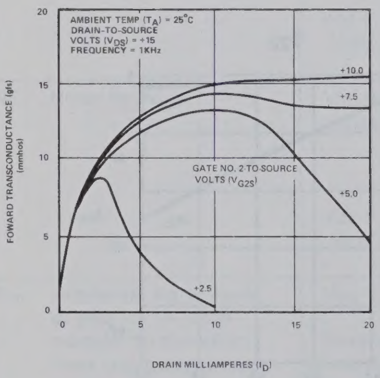
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



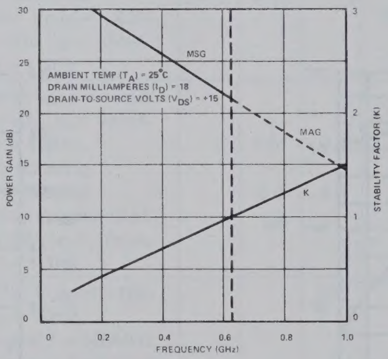
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



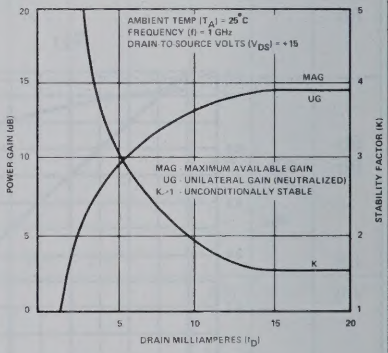
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



POWER GAIN vs FREQUENCY



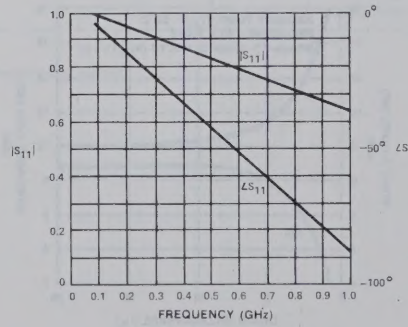
POWER GAIN vs DRAIN CURRENT

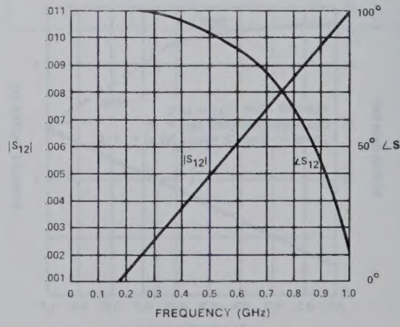


SD303 "S" PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18

DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) ≃ +2.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

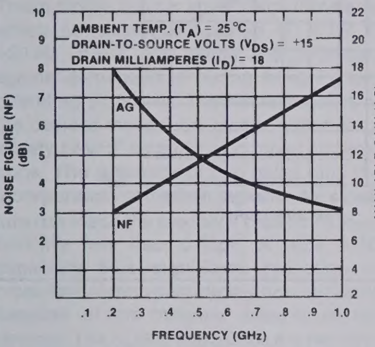




SD300/SE304 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

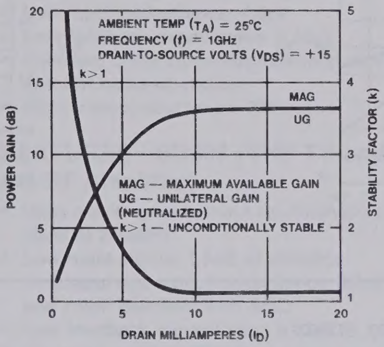
NOISE FIGURE AND AVAILABLE GAIN vs FREQUENCY

SD300



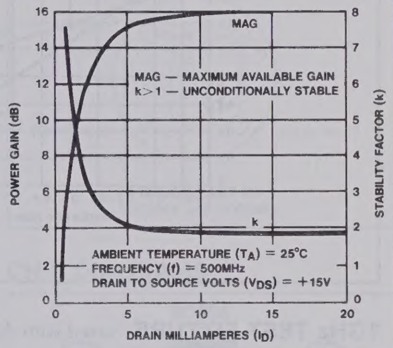
POWER GAIN vs DRAIN CURRENT

SD300



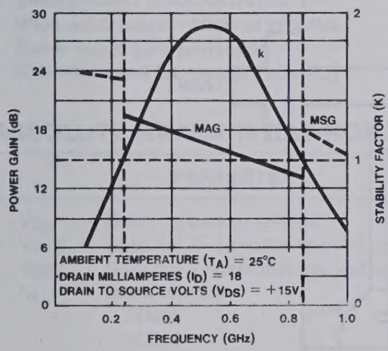
POWER GAIN vs DRAIN CURRENT

SD304



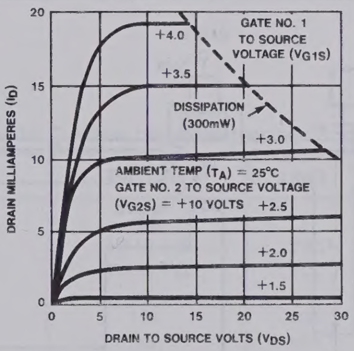
POWER GAIN vs FREQUENCY

SD304



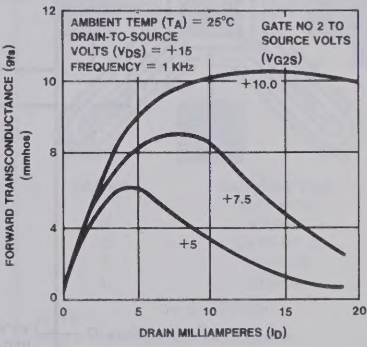
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

SD300/SE304



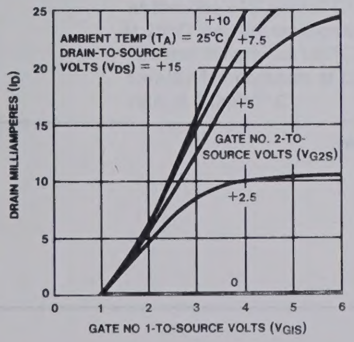
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT

SD300/SD304



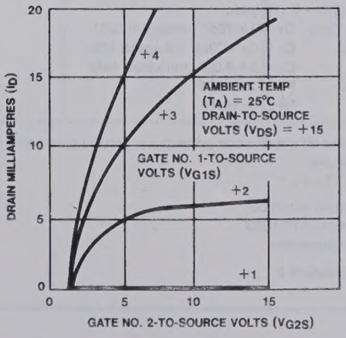
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE

SD300/SD304



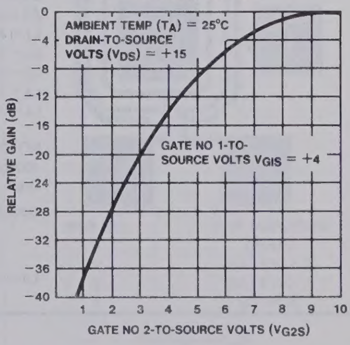
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE

SD300/SD304

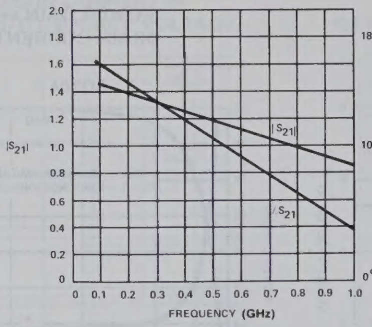


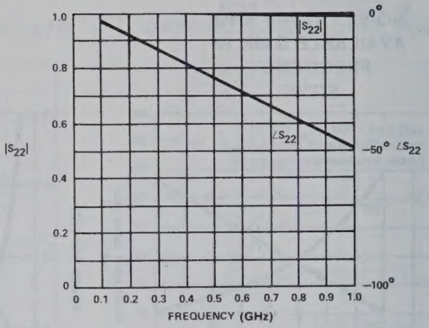
AUTOMATIC GAIN CONTROL RANGE AT 50MHz

SD300/SD304

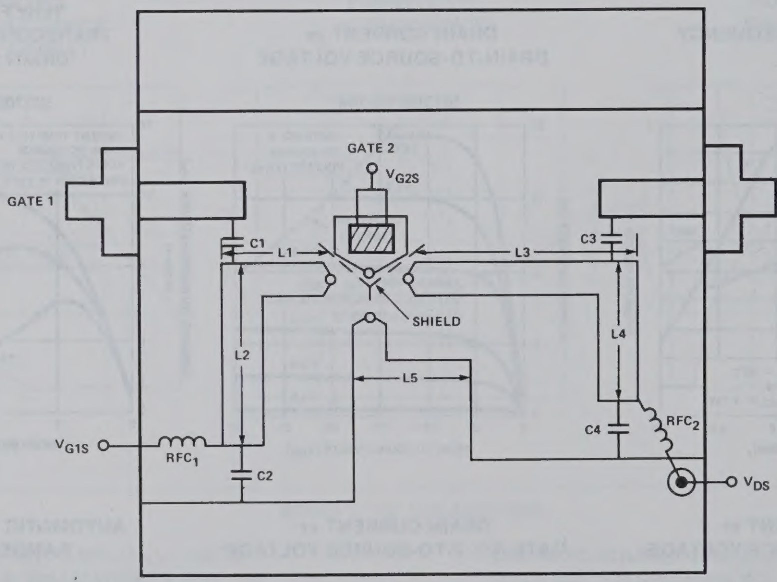


SD303 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)





1GHz TEST FIXTURE (used with SD300, SD303)


GATE 1
GATE 2
V_{G2S}
DRAIN
C1
L1
L3
C3
SHIELD
L2
L4
L5
C4
RFC_2
V_{G1S}
RFC_1
C2
V_{DS}

Dielectric is 1/16" Teflon-Fiberglass (3M-K6098-11).
All microstrip width = 0.175 inch.

L_1 = 0.42 inch	C_1 = 0.8-10pF Johanson 5201
L_2 = 1.68 inches	C_2 = C_4 1.20pF Johanson 5501
L_3 = 0.64 inch	C_3 = 0.4-6.0pF Johanson 4642
L_4 = 1.52 inches	RFC_1 = 0.22μH
L_5 = 0.30 inch	RFC_2 = 18μH

NOTE Shield and all passive components on ground plane side of amplifier.
1000pF bypasses are:

Drain:	Cory FT4-01-2
Gate 2:	American technical Ceramics ATC100B (Chip capacitor)

Launchers are OSM248-2

DESCRIPTION

The Signetics D-MOS SD305 and 306 are silicon, dual-insulated gate, field-effect transistors of the N-channel enhancement mode type. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations. The characteristics of the devices make them ideally suited for a variety of VHF amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (C_{G1D}) typically less than 0.03pF. A wide AGC capability plus significant reduction in cross modulation distortion is now available because of the inherent linearity of the devices. The SD305 and SD306 are hermetically sealed in a 4-lead TO-72 package.

GENERAL FEATURES

- **Positive bias only**
- **Low gate voltages**
- **Enhancement mode operation**
- **Wide AGC range: -50dB at 200MHz**
- **Zener diode gate protection**
- **ION implanted for greater reliability**

FEATURES—SD305 (VHF TV and FM Mixer)

- **High conversion gain: 17dB at 200MHz with $V_{G1S} = V_{G2S}$ for biasing simplicity**
- **Excellent isolation from Gate No. 1 (RF) to Gate No. 2 (LO): -20dB at 200MHz**
- **Low input capacitance: 4.0pF**
- **Low feedback capacitance: 0.03pF**
- **Excellent cross modulation performance and low noise operation**
- **High transconductance: 27mmhos**

FEATURES—SD306 (VHF TV and FM RF Amplifier)

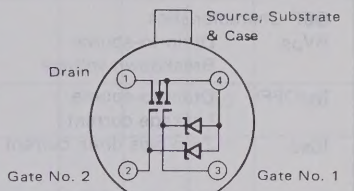
- **High power gain without neutralization: 20dB at 200MHz**
- **Low noise figure: 1.5dB at 200MHz**
- **Low input and output capacitance: 3.3pF and 1.0pF constant with AGC**
- **Low feedback capacitance: 0.03pF**
- **Superior cross modulation performance**
- **High transconductance: 15mmhos**

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

	PARAMETER	RATING	UNIT
V_{DS}	Drain-to-source voltage	+20	V
V_{G1B}	Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
V_{G2B}	Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
I_D	Drain current		
	SD305	150	mA
	SD306	50	mA
T_A	Ambient temperature range		
	Storage	-65 to +175	°C
	Operating	-55 to +125	°C
P_T	Transistor dissipation		
	At 25°C case temperature (Derate linearly to 125°C case temperature at the rate of 8.0mW/°C)	1.2	W
	At 25°C free-air temperature (Derate linearly to 125°C free-air temperature at the rate of 2.0mW/°C)	300	mW

PIN CONFIGURATION

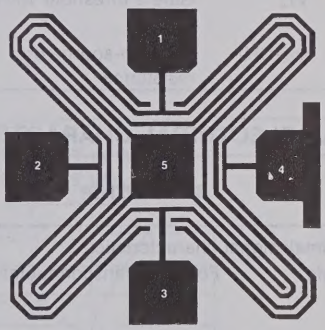
DE PACKAGE
(Top View)



ORDER PART NO.
SD305EE and SD306EE

CHIP DIAGRAMS

SD305

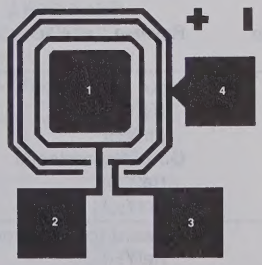


PAD NO.	PAD FUNCTION
1	GATE NO. 1
2	SOURCE
3	GATE NO. 2
4	SOURCE
5	DRAIN

Die Size 24 X 24

NOTE
Pads 2 and 4 must both be utilized for source connection

SD306



PAD NO.	PAD FUNCTION
1	DRAIN
2	GATE NO. 2
3	GATE NO. 1
4	SOURCE

Die Size 20 X 20

DC ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD305			SD306			UNIT
			Min	Typ	Max	Min	Typ	Max	
OFF Characteristics									
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		20	25		V
I_D (OFF)	Drain-to-source Leakage current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{DSS}	Zero bias drain current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{G1SS}	Gate no. 1 leakage current	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
I_{G2SS}	Gate no. 2 leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
ON Characteristics									
V_{T1}	Gate 1 threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2}	Gate 2 threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
r_{DS}(ON)	Drain-to-source on resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		30	60		65	100	Ω

AC ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD305			SD306			UNIT
			Min	Typ	Max	Min	Typ	Max	
Small signal characteristics									
g_{fs}	Forward transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, f = 1kHz							
		$I_D = 50mA$	24	27					mmhos
		$I_D = 18mA$				13	15		mmhos
g_{fs} (CONV)	Conversion transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, f = 1kHz, $E_{LO}(RMS) = 750mV$		10					mmhos
Capacitances		f = 1MHz, gate 2 AC grounded							
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$							
		$I_D = 50mA$		4.0	5.0				pF
		$I_D = 18mA$					3.3	3.6	pF
		$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	5.0				pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		1.3	1.7		1.0	1.3	pF
C_{G1D}	Reverse transfer	$V_{DS} = +15V$ $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.03			0.03		pF
	Input admittance	f = 200MHz, $V_{DS} = +15V$	$V_{G1S} = V_{G2S}$, $I_D = 8mA$			$V_{G2S} = +10V$, $I_D = 18mA$			
	$Re(Y_{11})$			1.05			1.11		mmhos
	$Im(Y_{11})$			6.66			4.76		mmhos
	Output admittance	f = 200MHz, $V_{DS} = +15V$							
	$Re(Y_{22})$			0.73			1.05		mmhos
	$Im(Y_{22})$			2.09			1.54		mmhos
	Forward transmittance	f = 200MHz, $V_{DS} = +15V$							
	$Re(Y_{21})$			4.69			13.23		mmhos
	$Im(Y_{21})$			-3.01			-5.62		mmhos
	Reverse transmittance	f = 200MHz, $V_{DS} = +15V$							
	$Re(Y_{12})$			0.04			0.01		mmhos
	$Im(Y_{12})$			-0.03			-0.04		mmhos
G_{ps}	Power gain[2]	$V_{DS} = +15V$, $V_{G2S} = +10V$ $I_D = 18mA$, f = 200MHz				17	20		dB

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.

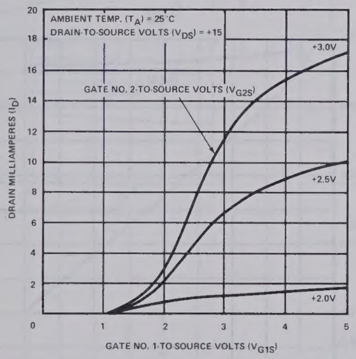
PARAMETER		TEST CONDITIONS	SD305			SD306			UNIT
			Min	Typ	Max	Min	Typ	Max	
G_{ps}(CONV)	Conversion power gain[1]	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f_{rf} = 200MHz$, $f_{LO} = 245MHz$	14	17					dB
NF	Noise figure	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, $f = 200MHz$					1.5	2.5	dB
AGC_{VG2S}	Range of automatic gain control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V \rightarrow 0V$, $f = 200MHz$					50		dB
E_{INT}	Interfering signal level at gate 1 for 1% cross modulation distortion, peak voltage referenced to 50Ω system[3]	$V_{DS} = 15V$, $V_{G2S} = +8V$, $I_D = 15mA$ Wanted signal f = 200MHz interfering signal f = 196MHz					480		mV

NOTES

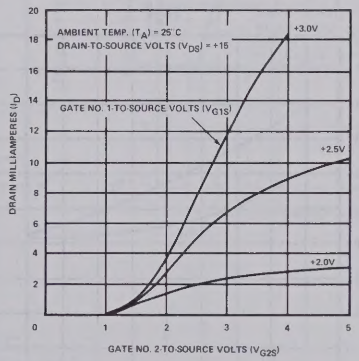
1. Measured in mixer test fixture.
2. Measured in amplifier test fixture.
3. Measured as shown in block diagram.

SD305 TYPICAL PERFORMANCE CHARACTERISTICS

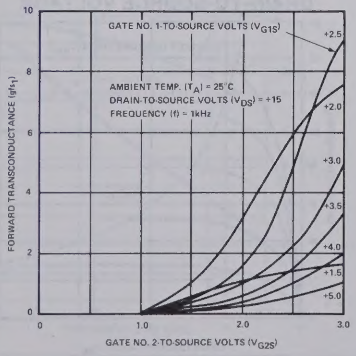
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



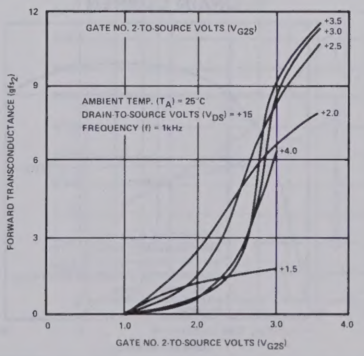
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



GATE NO. 1 FORWARD TRANSCONDUCTANCE vs GATE NO. 2-TO-SOURCE VOLTAGE



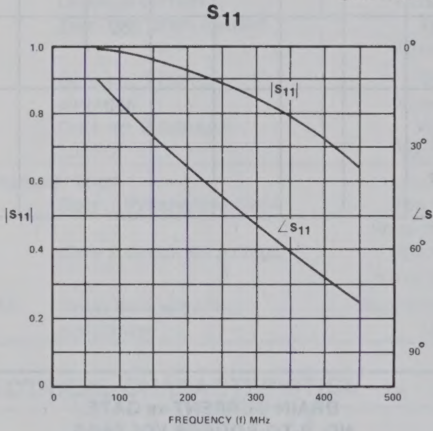
GATE NO. 2 FORWARD TRANSCONDUCTANCE vs GATE NO. 1-TO-SOURCE VOLTAGE

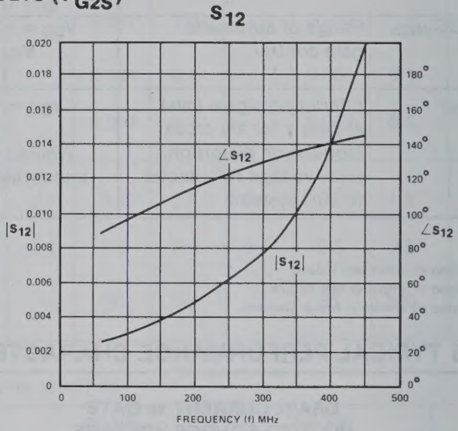


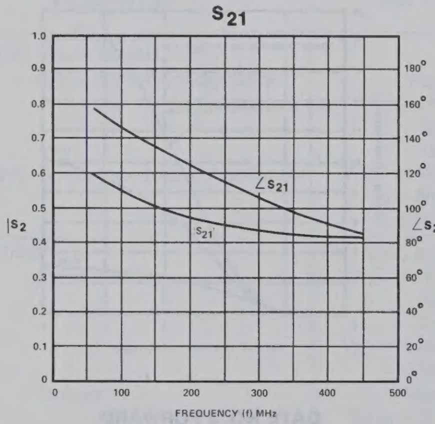
SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

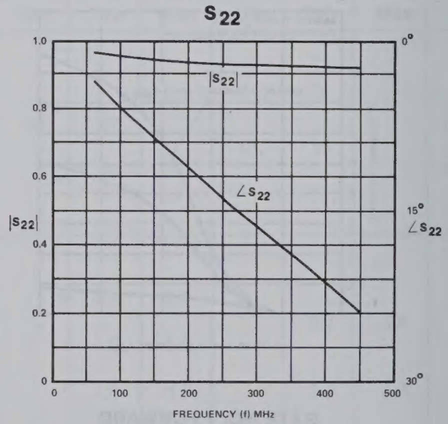
"S" PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
DRAIN MILLIAMPERES (ID) = 8
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) =
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S})

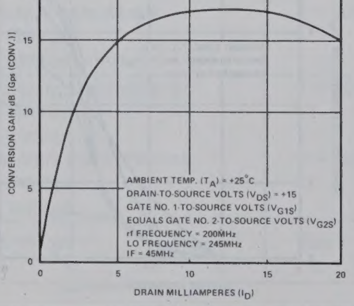






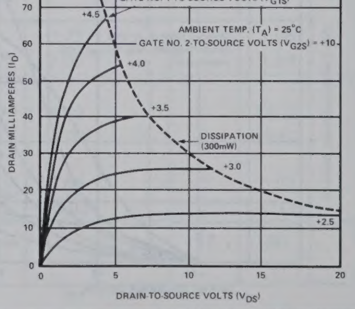


CONVERSION GAIN vs DRAIN CURRENT



AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S})
EQUALS GATE NO. 2-TO-SOURCE VOLTS (V_{G2S})
rf FREQUENCY = 200MHz
LO FREQUENCY = 245MHz
IF = 45MHz

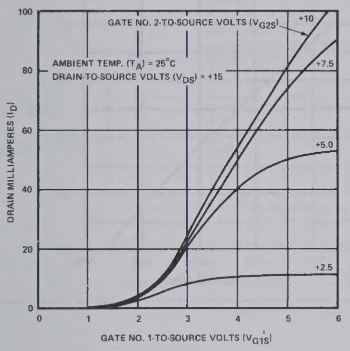
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



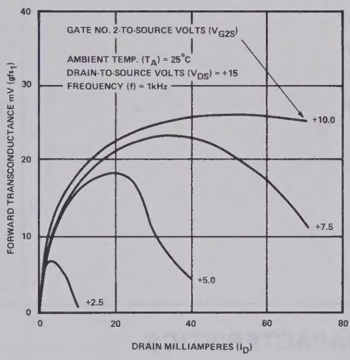
AMBIENT TEMP. (T_A) = 25°C
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

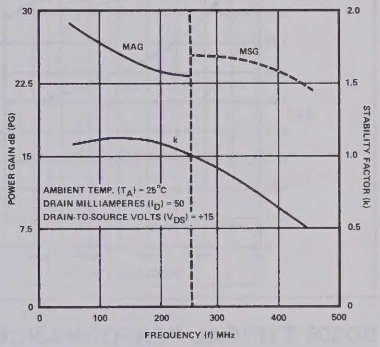
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



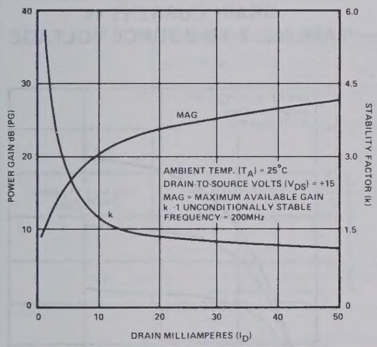
GATE NO. 1 FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



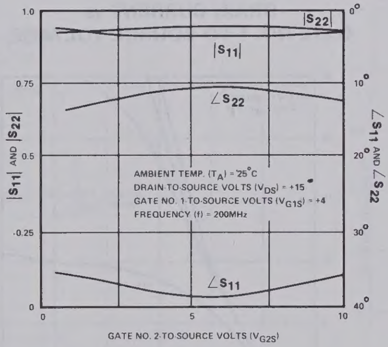
POWER GAIN vs FREQUENCY



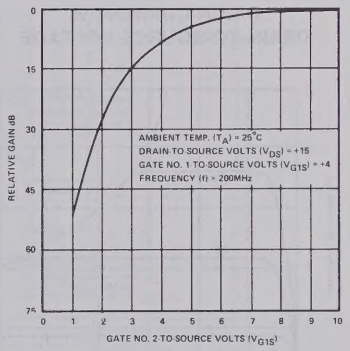
POWER GAIN vs DRAIN CURRENT



AUTOMATIC GAIN CONTROL vs S_{11} AND S_{22}



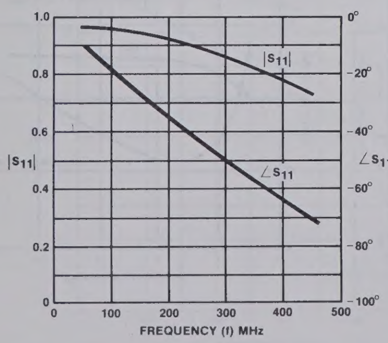
AUTOMATIC GAIN CONTROL RANGE



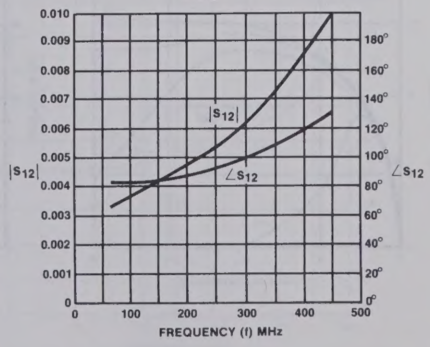
"S" PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
DRAIN MILLIAMPERES (I_D) = 50
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) ≃ +3.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

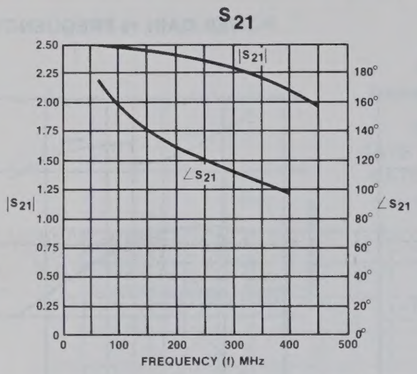
S_{11}

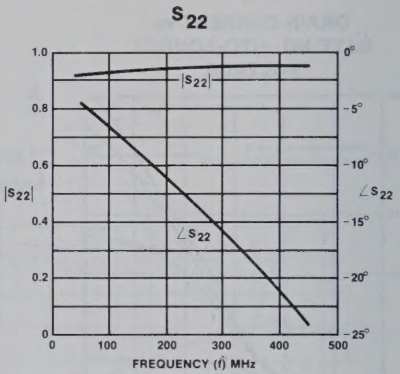


S_{12}



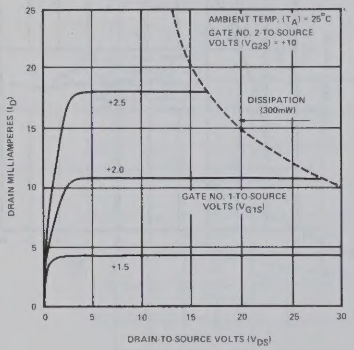
SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



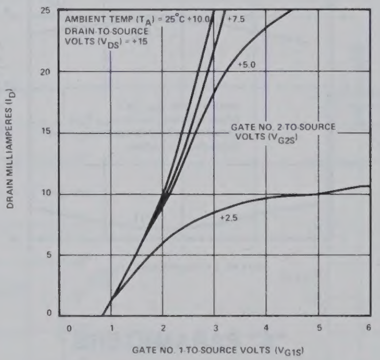


SD306 TYPICAL PERFORMANCE CHARACTERISTICS

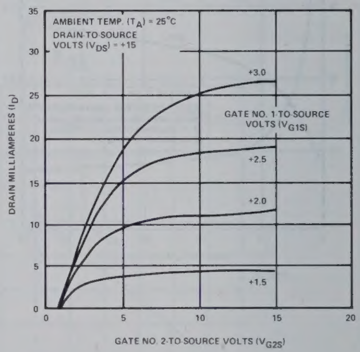
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



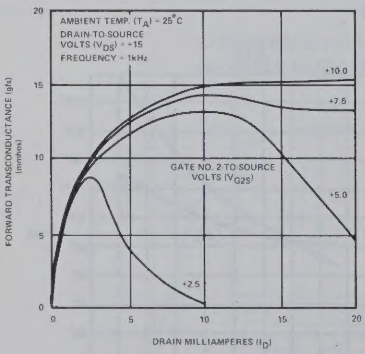
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



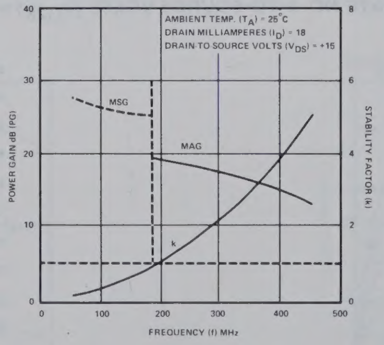
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



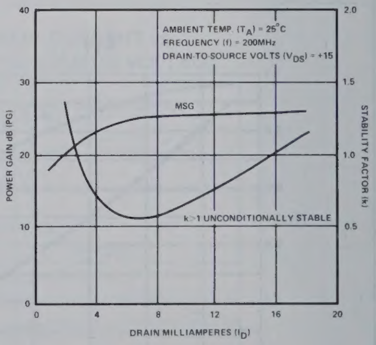
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



POWER GAIN vs FREQUENCY

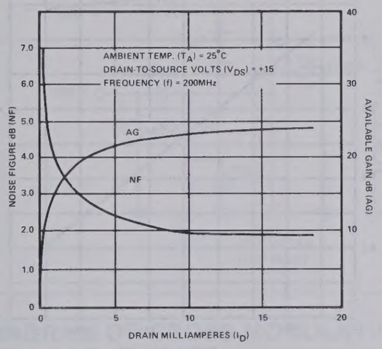


POWER GAIN vs DRAIN CURRENT

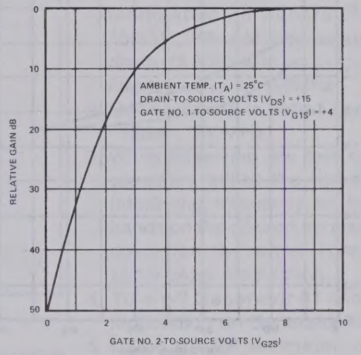


SD306 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

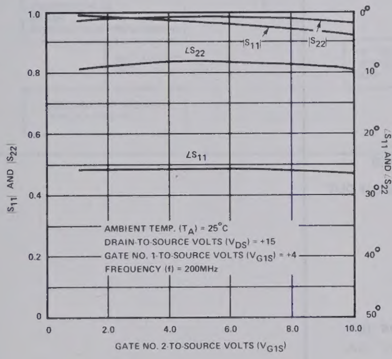
NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



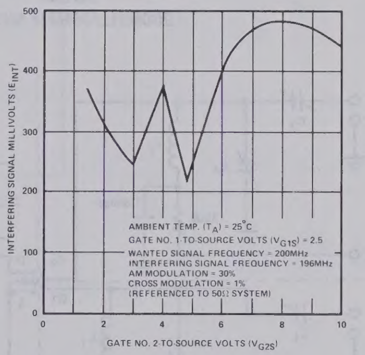
AUTOMATIC GAIN CONTROL RANGE AT 200MHz



S_{11} AND S_{22} vs AUTOMATIC GAIN CONTROL



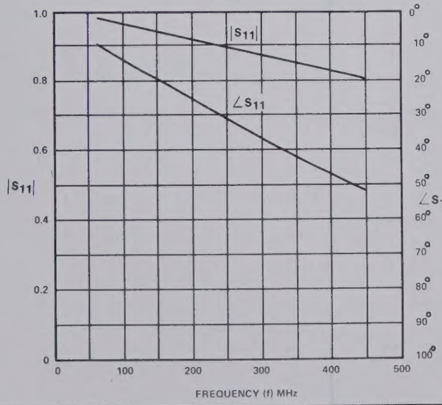
INTERFERING SIGNAL LEVEL vs GATE NO. 2-TO-SOURCE VOLTS



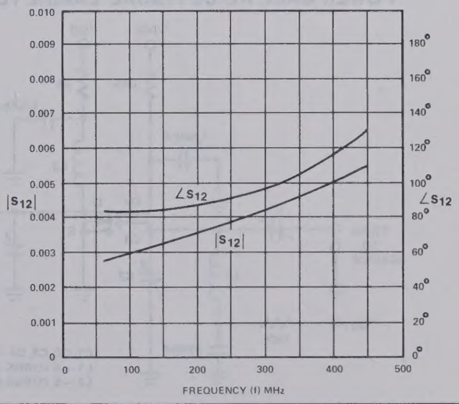
"S" PARAMETERS

AMBIENT TEMP. $(T_A) = +25°C$
DRAIN-TO-SOURCE VOLTS $(V_{DS}) = 15$
DRAIN MILLIAMPERES $(I_D) = 8$
GATE NO. 1-TO-SOURCE VOLTS $(V_{G1S}) \simeq +2.5$
GATE NO. 2-TO-SOURCE VOLTS $(V_{G2S}) = +10$

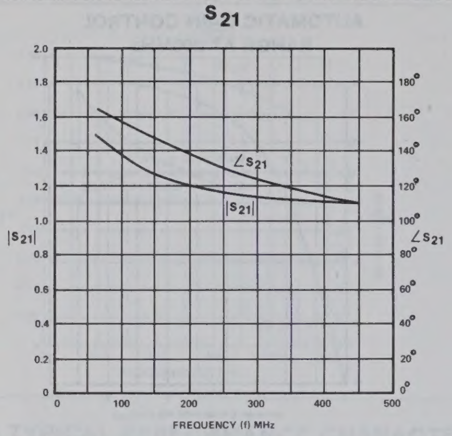
S_{11}

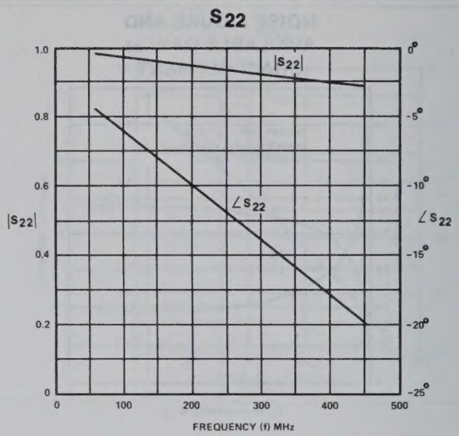


S_{12}



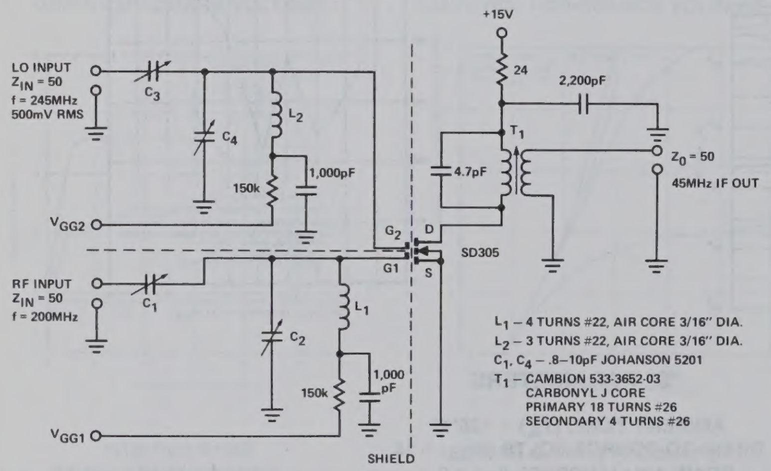
SD306 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)





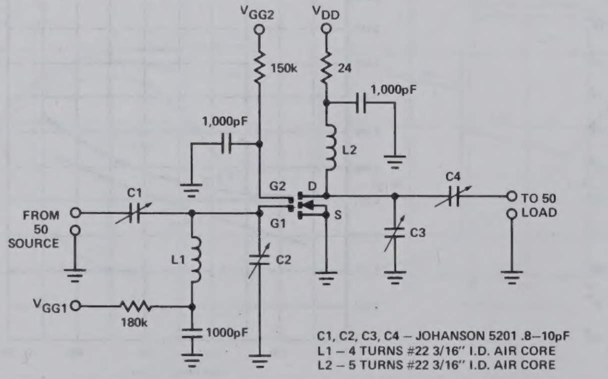
TEST CIRCUITS

SD305
200MHz/45MHz MIXER


+15V
LO INPUT
Z$_{IN}$ = 50
f = 245MHz
500mV RMS
C3
C4
L2
24
2,200pF
T1
4.7pF
Z0 = 50
45MHz IF OUT
150k
1,000pF
VGG2
G2
D
G1
S
SD305
RF INPUT
Z$_{IN}$ = 50
f = 200MHz
C1
L1
C2
150k
1,000 pF
VGG1
SHIELD

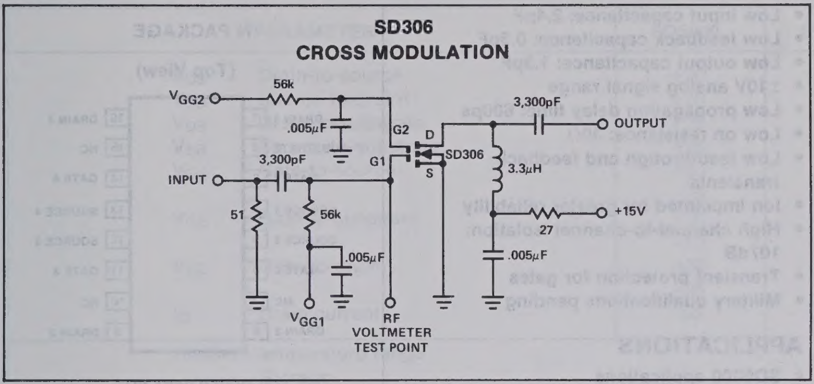
L_1 – 4 TURNS #22, AIR CORE 3/16" DIA.
L_2 – 3 TURNS #22, AIR CORE 3/16" DIA.
C_1, C_4 – .8–10pF JOHANSON 5201
T_1 – CAMBION 533-3652-03
CARBONYL J CORE
PRIMARY 18 TURNS #26
SECONDARY 4 TURNS #26

SD306
POWER GAIN, NOISE FIGURE 200MHz TEST AMPLIFIER;

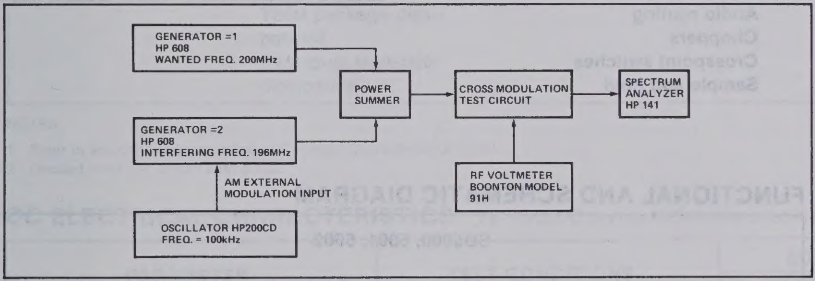

VGG2
VDD
150k
24
1,000pF
1,000pF
L2
C4
G2
D
G1
S
FROM
50
SOURCE
C1
TO 50
LOAD
C3
L1
C2
VGG1
180k
1000pF

C1, C2, C3, C4 – JOHANSON 5201 .8–10pF
L1 – 4 TURNS #22 3/16" I.D. AIR CORE
L2 – 5 TURNS #22 3/16" I.D. AIR CORE

TEST CIRCUITS (Cont'd)


SD306
CROSS MODULATION
V_{GG2}
56k
.005µF
G2
D
3,300pF
OUTPUT
3,300pF
G1
SD306
S
INPUT
3.3µH
51
56k
27
+15V
.005µF
.005µF
V_{GG1}
RF
VOLTMETER
TEST POINT

BLOCK DIAGRAM OF CROSS MODULATION TEST


GENERATOR =1
HP 608
WANTED FREQ. 200MHz
POWER
SUMMER
CROSS MODULATION
TEST CIRCUIT
SPECTRUM
ANALYZER
HP 141
GENERATOR =2
HP 608
INTERFERING FREQ. 196MHz
AM EXTERNAL
MODULATION INPUT
RF VOLTMETER
BOONTON MODEL
91H
OSCILLATOR HP200CD
FREQ. = 100kHz

SD306
TEST PROCEDURE FOR CROSS MODULATION DISTORTION MEASUREMENTS

1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.
2. Generator #2 is set at approximately –15dbm, 200MHz.
3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.
4. Turn off Generator #1 and turn off the modulation on Generator #2.
5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

D-MOS FET QUAD ANALOG SWITCH ARRAYS AND MULTIPLEXERS

SD5000/SD5001/SD5002

SD5000/5001/5002-N

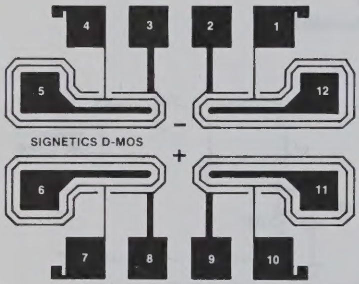
DESCRIPTION

The Signetics D-MOS SD5000 series are monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enhancement mode technology.

This family of devices is designed to handle a wide variety of analog switching and driver applications. They are capable of high speed operation where excellent transient response, and wide voltage range are required. The SD5000 quad switch array quad multiplexer can handle high voltage analog signals (±10V). The SD5002 is designed for ±7.5V analog signals using ±15V power supplies. The SD5001 is designed for lower voltage applications.

CHIP DIAGRAM

SD5000, 5001, 5002
SWITCH ARRAYS


4
3
2
1
5
12
SIGNETICS D-MOS
–
+
6
11
7
8
9
10

PAD NO.	PAD FUNCTION
1	Gate No. 1
2	Source No. 1
3	Source No. 2
4	Gate No. 2
5	Drain No. 2
6	Drain No. 3
7	Gate No. 3
8	Source No. 3
9	Source No. 4
10	Gate No. 4
11	Drain No. 4
12	Drain No. 1

Die Size 40X32

FEATURES

- **Low input capacitance: 2.4pF**
- **Low feedback capacitance: 0.3pF**
- **Low output capacitance: 1.3pF**
- **±10V analog signal range**
- **Low propagation delay time: 600ps**
- **Low on resistance: 30Ω**
- **Low feedthrough and feedback transients**
- **Ion implanted for greater reliability**
- **High channel-to-channel isolation: 107dB**
- **Transient protection for gates**
- **Military qualifications pending**

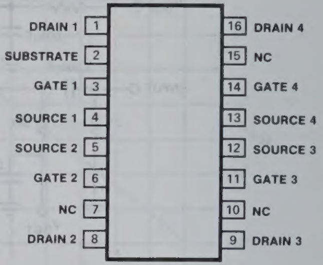
APPLICATIONS

- **SD5000 applications**
  Analog switching (up to very high frequencies)
  Audio routing
  Choppers
  Crosspoint switches
  Sample and hold

PIN CONFIGURATIONS

N PACKAGE

(Top View)

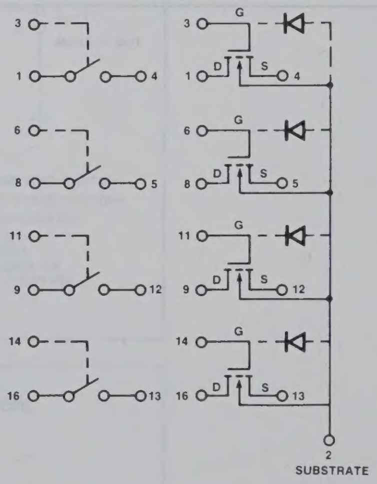

DRAIN 1 1
SUBSTRATE 2
GATE 1 3
SOURCE 1 4
SOURCE 2 5
GATE 2 6
NC 7
DRAIN 2 8
16 DRAIN 4
15 NC
14 GATE 4
13 SOURCE 4
12 SOURCE 3
11 GATE 3
10 NC
9 DRAIN 3

ORDER PART NO.

SD5000N SD5001N SD5002N

FUNCTIONAL AND SCHEMATIC DIAGRAM

SD5000, 5001, 5002


3
1
4
6
8
5
11
9
12
14
16
13
G
D
S
2
SUBSTRATE

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

	PARAMETER	SD5000	SD5001	SD5002	UNIT
V_{DS}	Drain-to-source	+20	+10	+15	Vdc
V_{SD}	Source-to-drain[1]	+20	+10	+15	Vdc
V_{DB}	Drain-to-substrate	+25	+15	+22.5	Vdc
V_{SB}	Source-to-substrate	+25	+15	+22.5	Vdc
V_{GS}	Gate-to-source	+30 -25	+25 -15	+30 -22.5	Vdc
V_{GB}	Gate-to-substrate	+30 -0.3	+25 -0.3	+30 -0.3	Vdc
V_{GD}	Gate-to-drain	+30 -25	+25 -15	+30 -22.5	Vdc
I_D	Drain current	50	50	50	mA
	Ambient temperature range				
	Storage		-55 to +150		°C
	Operating		0 to +85		°C
	Power Dissipation				
	Total package dissipation[2]		640		mW
	Individual transistor dissipation		300		mW

NOTES

1. Refer to test conditions specified in Electrical Characteristics Table.
2. Derated 5mW per degree centigrade.

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD5000			SD5001			UNIT
			Min	Typ	Max	Min	Typ	Max	
BREAKDOWN VOLTAGE									
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	20	25		10	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	20			10			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open $I_D = 10nA$	25			15			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain Open $I_S = 10\mu A$	25			15			V
LEAKAGE CURRENT									
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$							
		$V_{DS} = +20V$		1	10				nA
		$V_{DS} = +10V$					1	10	nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$							
		$V_{SD} = +20V$		1	10				nA
		$V_{SD} = +10V$					1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$							
		$V_{GB} = 30V$			1				μA
		$V_{GB} = 25V$						1	μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source-resistance	$I_D = 1.0mA$, $V_{SB} = 0$							
		$V_{GS} = +5V$		50	70		50	70	Ω
		$V_{GS} = +10V$		30			30		Ω
		$V_{GS} = +15V$		23			23		Ω
		$V_{GS} = +20V$		19			19		Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD5002			UNIT
			Min	Typ	Max	
BREAKDOWN VOLTAGE						
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	15	25		V
		$V_{GS} = V_{BS} = 0V$, $I_S = 1\mu A$				V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	15			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open				
		$I_D = 10nA$	22.5			V
		$I_D = 1\mu A$				V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain Open				
		$I_S = 10\mu A$	22.5			V
LEAKAGE CURRENT						
$I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$				
		$V_{DS} = +15V$		1	10	nA
		$V_{GS} = V_{BS} = 0V$, $V_{DS} = +10V$				nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$				
		$V_{SD} = +15V$		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$				
		$V_{GB} = 30V$			1	μA
		$V_{GB} = 25V$				μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source-resistance	$I_D = 1.0mA$, $V_{SB} = 0$				
		$V_{GS} = +5V$		50	70	Ω
		$V_{GS} = +10V$		30		Ω
		$V_{GS} = +15V$		23		Ω
		$V_{GS} = +20V$		19		Ω

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	SD5000			SD5001			UNIT
			Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, f = 1kHz	10	15		10	15		mmhos
	Small signal capacitances	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$							
$C_{(GS+GD+GB)}$	Gate node	See capacitance model		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node	in Figure 1		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5	pF
C_T	Cross talk	See test circuits no. 1 and 2, f = 3kHz		−107			−107		dB

AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	SD5002			UNIT
			Min	Typ	Max	
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, f = 1kHz	10	15		mmhos
	Small signal capacitances	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$				
$C_{(GS+GD+GB)}$	Gate node	See capacitance model in Figure 1		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5	pF
C_T	Cross talk	See test circuits no. 1 and 2, f = 3kHz		-107		dB

THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of up to ±10 volts for the SD5000 and ±7.5 volts for the SD5002. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T, the FET switch starts to turn ON with V_{GS} in excess of +10 volts, a low resistance path (typically 30Ω) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are **isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation.** The SD5000 series offers superior performance in all these areas (Figure 1).

Isolation. ON resistance is typically 30Ω and OFF resistance is typically 10^{10}Ω, which results in an OFF to ON resistance ratio in excess of 10^9. Isolation from output to input from 3kHz analog signals is typically -107dB.

Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example, for 600Ω source impedance the insertion loss for voice signals (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5000 switches turn ON at sub-nanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB at 1GHz).

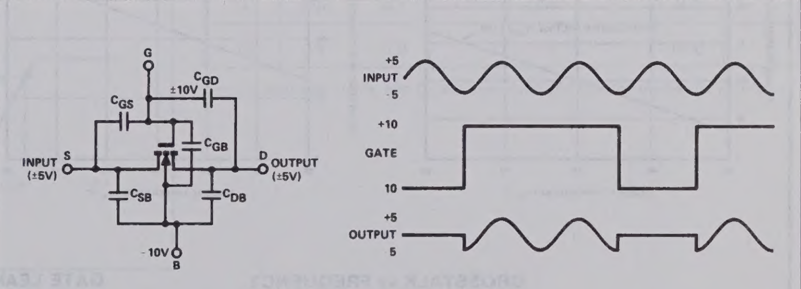
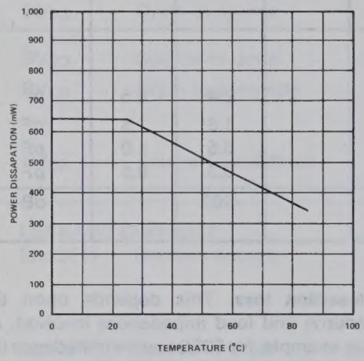


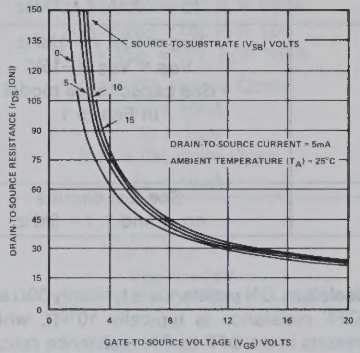
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS

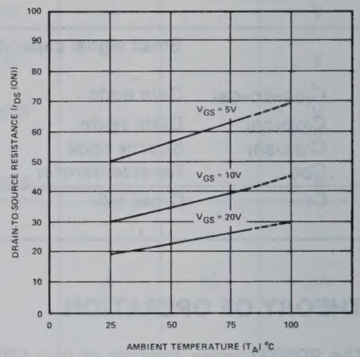
MAXIMUM POWER DISSIPATION vs TEMPERATURE



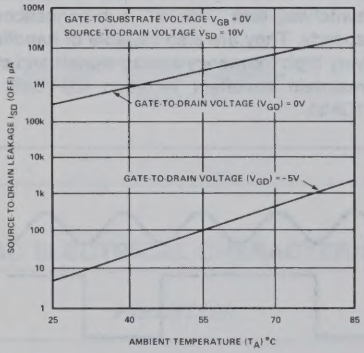
DRAIN-TO-SOURCE RESISTANCE vs SOURCE-TO-SUBSTRATE AND GATE-TO-SOURCE VOLTAGE



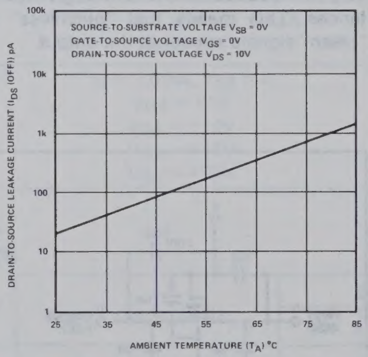
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



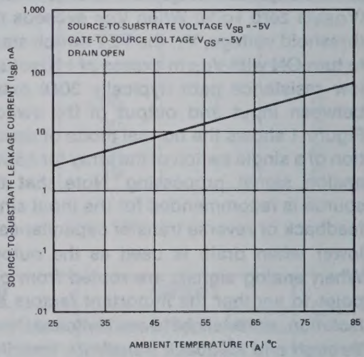
SOURCE-TO-DRAIN LEAKAGE CURRENT vs TEMPERATURE



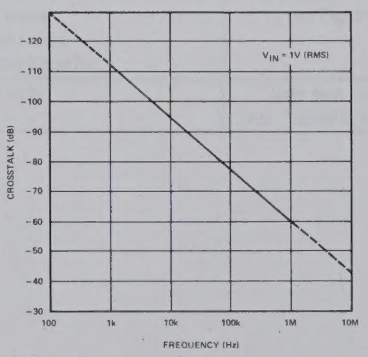
DRAIN-TO-SOURCE LEAKAGE CURRENT vs TEMPERATURE



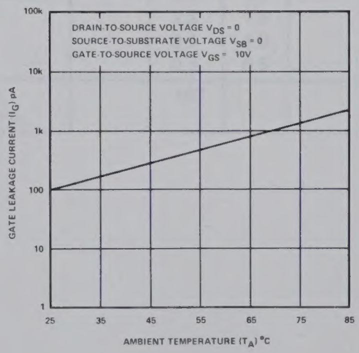
SOURCE-TO-SUBSTRATE LEAKAGE CURRENT vs TEMPERATURE



CROSSTALK vs FREQUENCY



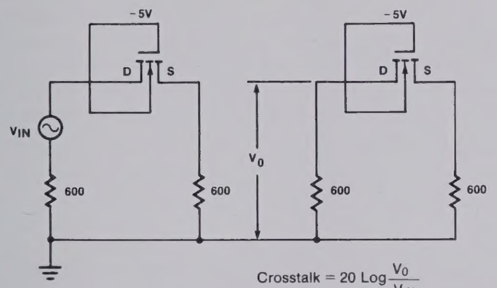
GATE LEAKAGE CURRENT vs TEMPERATURE



TEST CIRCUIT

CROSSTALK MEASUREMENT

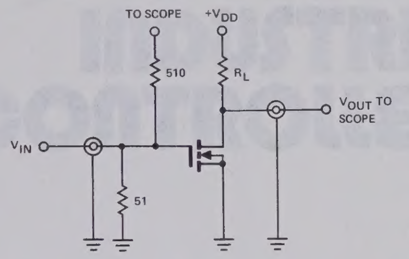
Quad Switch
SD5000/SD5001/SD5002


- 5V
D
S
- 5V
D
S
V_{IN}
600
600
V_0
600
600

$\text{Crosstalk} = 20 \text{ Log} \frac{V_O}{V_{IN}}$

Where V_{IN} = 1V RMS at 3kHz

SWITCHING TEST CIRCUIT


TO SCOPE
$+V_{DD}$
510
R_L
V_{OUT} TO SCOPE
V_{IN}
51

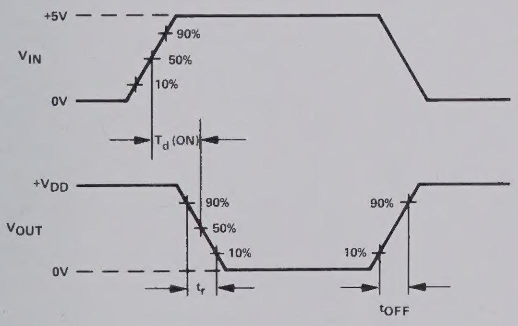
Input Pulse

t_r, t_F < 1ns
Pulse Width = 100ns
Rep Rate = 1MHz

Sampling Scope

t_r < 350ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

SWITCHING WAVEFORMS


+5V
90%
V_{IN}
50%
10%
0V
T_d (ON)
$+V_{DD}$
90%
90%
V_{OUT}
50%
10%
10%
0V
t_r
t_{OFF}

SWITCHING CHARACTERISTICS

		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)*	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

SECTION 16
INDUSTRIAL CONTROLLERS

Section 16—INDUSTRIAL CONTROLLERS

NE5522 Universal Analog Controller 493

DESCRIPTION

The Signetics NE5522 may be used in a wide range of industrial applications where closed loop control of machine speed and acceleration is required. Uses such as conveyer systems, web infeed for plastic film or paper sheet, wire reel take-up and many other process motion control areas, which involve the predetermined ramp up and final speed setting under closed-loop control, can be handled by the Universal Controller.

Inputs to the device are descrete voltage level commands which tell the controller what function is desired such as "Set Memory", 'Memory Erase', 'Positive Ramp', 'Compare to Memory', etc. The closed loop control function is accomplished by an A-C tachometer frequency representative of the speed of the system being fed into the NE5522 where it is compared with an internal reference voltage after being processed by the F/V converter. An error signal is then generated which governs the corrective response of the output. The output function consists of three buffered open collector transistor ports which provide gating and on-off commands to peripheral circuitry. An analog error output is also available for interface with linear control systems.

Basically the NE5522 consists of a frequency to voltage converter, an internal reference oscillator, D to A converter, an I^2L logic encoder-decoder and 256 bit F/V D.C. level data storage.

The nominal supply voltage is +8.2V with a range of 7.4 to 9 volts allowed. Current drain is nominally 20mA for an 8.2V supply.

A typical operation sequence might be to bring a motor up to speed using the program accel mode. This would be accomplished by setting pin 3 (Command Input) to $\simeq .55V_{CC}$. A ramp function determined by R20-C11 (pins 14, 15) then automatically programs the error system to drive up at a fixed rate. Once the desired speed is reached a voltage of $.75V_{CC}$ is momentarily impressed on the command input and the motor speed will then be controlled to stay at that level previously programmed in memory. Note that a voltage level of $1.1V_{CC}$ must be applied momentarily to the command input (pin 3) upon initial turn-on in order to enable the device.

FEATURES

- Adjustable system gain
- Adjustable frequency sensitivity
- Adjustable ramp rate
- Voltage programmable command modes
  1. On
  2. Positive ramp and hold
  3. Compare to set memory
  4. Memory erase
  5. Set memory
  6. Off

APPLICATIONS

- Conveyer Controller
- Web infeed controller
- AC or dc motor speed control
- Actuator control loop
- Engine speed control
- Process control
- Magnetics tape transport control
- Mag/floppy disc controller

TRUTH TABLE

PIN 3 COMMAND INPUT VOLTAGE	MODE	FUNCTION
Greater than 1.1 V_{CC}	ON	ON
.900 V_{CC} to V_{CC}	A	Set memory after command C or D.
.725 V_{CC} to .8 V_{CC}	B	Compare to set memory.
.482 V_{CC} to .599 V_{CC}	C	Positive ramp.
.148 V_{CC} to .272 V_{CC}	D	Memory erase.
Less than .094 V_{CC}	OFF	OFF

TRUTH TABLE

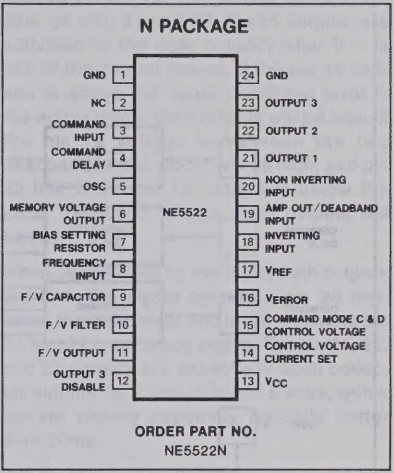
COMMAND MODE INPUT SEQUENCE	OUTPUT 1	OUTPUT 2	OUTPUT 3	V_6 (MEMORY)
OFF	L	L	H	<1V
ON/C	H	H	L	<1V
ON/C/A ($V_S \ll V_M$)	H	H	L	$V_{F/V}$
ON/C/A ($V_S \gg V_M$)	L	L	L	$V_{F/V}$
ON/C/A/D	L	L	H	<1V
ON/C/A/D/A ($V_S \ll V_M$)	H	H	L	$V_{F/V}$
($V_S \gg V_M$)	L	L	L	$V_{F/V}$
ON/D/A/disable	L	L	H	$V_{F/V}$
ON/C/A/DIS/B ($V_S \ll V_M$)	H	H	L	$V_{F/V}$
($V_S \gg V_M$)	L	L	L	$V_{F/V}$

NOTES
V_S = F/V Output
V_M = Memory Voltage
Disable = Pin 12, Output 3
Command Delay Equations: t_d (All except command B) = 45K (C_4), $t_{d(B)}$ = 305K (C_4), $C_4 > .05\mu$

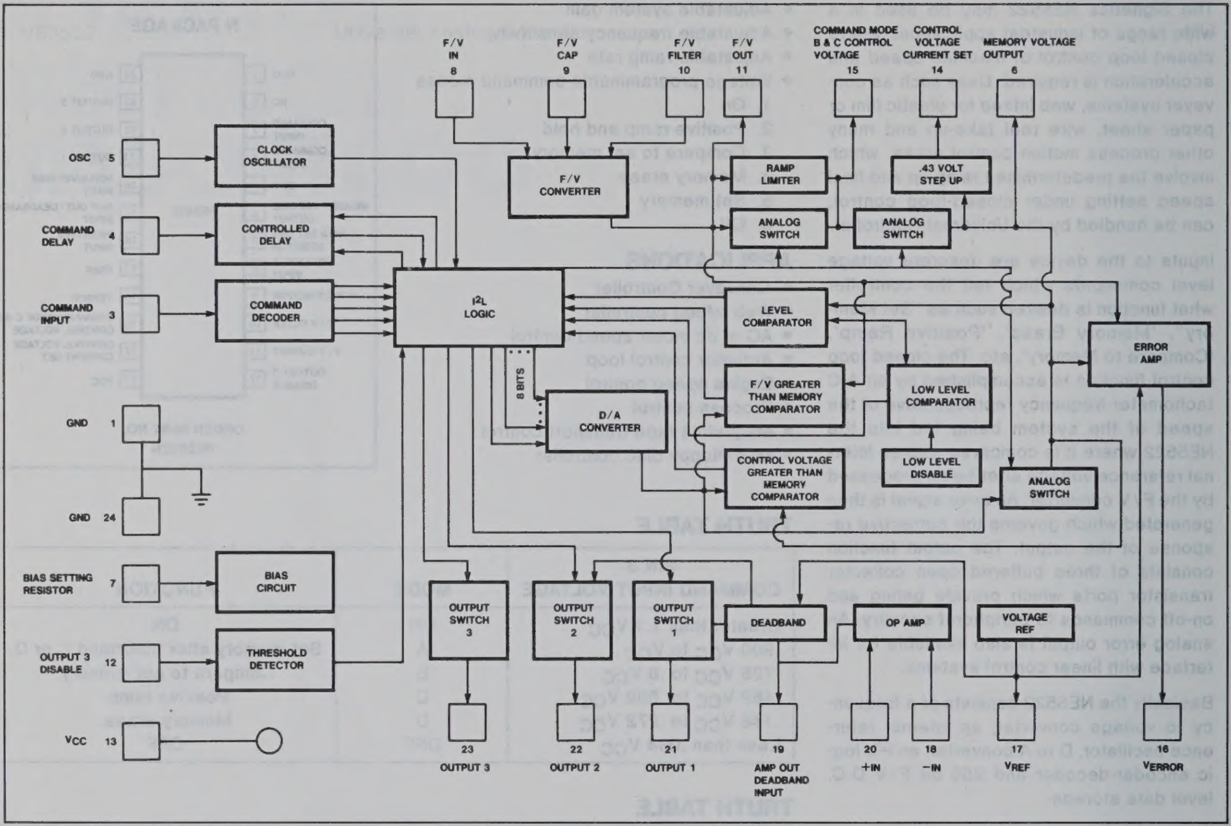
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature	0 to +70	°C
Storage temperature	−65 to +150	°C
Supply voltage	9	V

PIN CONFIGURATION


N PACKAGE
GND 1
NC 2
COMMAND INPUT 3
COMMAND DELAY 4
OSC 5
MEMORY VOLTAGE OUTPUT 6
BIAS SETTING RESISTOR 7
FREQUENCY INPUT 8
F/V CAPACITOR 9
F/V FILTER 10
F/V OUTPUT 11
OUTPUT 3 DISABLE 12
NE5522
24 GND
23 OUTPUT 3
22 OUTPUT 2
21 OUTPUT 1
20 NON INVERTING INPUT
19 AMP OUT/DEADBAND INPUT
18 INVERTING INPUT
17 VREF
16 VERROR
15 COMMAND MODE C & D CONTROL VOLTAGE
14 CONTROL VOLTAGE CURRENT SET
13 VCC
ORDER PART NO.
NE5522N

BLOCK DIAGRAM


F/V IN 8
F/V CAP 9
F/V FILTER 10
F/V OUT 11
COMMAND MODE B & C CONTROL VOLTAGE 15
CONTROL VOLTAGE CURRENT SET 14
MEMORY VOLTAGE OUTPUT 6
OSC 5
CLOCK OSCILLATOR
F/V CONVERTER
RAMP LIMITER
.43 VOLT STEP UP
COMMAND DELAY 4
CONTROLLED DELAY
ANALOG SWITCH
ANALOG SWITCH
COMMAND INPUT 3
COMMAND DECODER
I²L LOGIC
LEVEL COMPARATOR
ERROR AMP
8 BITS
F/V GREATER THAN MEMORY COMPARATOR
LOW LEVEL COMPARATOR
GND 1
D/A CONVERTER
LOW LEVEL DISABLE
CONTROL VOLTAGE GREATER THAN MEMORY COMPARATOR
ANALOG SWITCH
GND 24
BIAS SETTING RESISTOR 7
BIAS CIRCUIT
OUTPUT SWITCH 3
OUTPUT SWITCH 2
OUTPUT SWITCH 1
DEADBAND
OP AMP
VOLTAGE REF
OUTPUT 3 DISABLE 12
THRESHOLD DETECTOR
VCC 13
23 OUTPUT 3
22 OUTPUT 2
21 OUTPUT 1
19 AMP OUT DEADBAND INPUT
20 +IN
18 −IN
17 VREF
16 VERROR

FUNCTIONAL DESCRIPTION

(1) Input Power (V_{CC})—A regulated power source of 8.2 volts ± 10% must be applied between pin 13 and ground. Pins 1 and 24 are the IC ground pins. Pin 2 should be connected to ground also. Standby current drain is typically 20mA. A resistor of 43kΩ ± 5% must be connected between pin 7 and ground to establish the internal current sources.

(2) Frequency-to-Voltage Converter—The F/V input signal for this device is applied to pin 8. It may be in the form of any periodic wave with approximately 50% duty cycle at the zero crossings. Peak amplitudes greater than ±2 volts should be current limited by a resistor in series with pin 8. Maximum currents should not exceed 1mA. This input is internally amplified and limited at the zero crossings (refer to typical test circuit).

A capacitor, C_6, must be applied from pin 9 to ground. A capacitor, C_7, and resistor, R_{18}, must be applied in parallel between pin 10 and ground. A voltage will then appear on pin 11 with a d-c level, V_s, proportional to the input frequency, and a sawtooth ripple frequency equal to twice the input frequency, f_s. V_s and the peak-to-peak ripple amplitude, V_r, are given approximately by the following equations:

$$V_s = (4\text{ volts})\,(R_{18})\,(C_6)\,(f_s)$$

$$V_r = (2\text{ volts})\left(\frac{C_6}{C_7}\right) 1 - \left[(80k\Omega)\,C_6\,f_s\right]$$

The maximum linear value of V_s is typically (V_{CC} − 1.0 volt). The maximum input frequency for linear output is given by:

$$f_s\ max = \frac{1}{(80k\Omega)C_6},$$

assuming symmetrical zero crossings in the input wave. A resistor of no less than 10kΩ from pin 11 to ground is allowable to maintain bias on the NPN emitter follower output stage.

The pin 11 voltage is applied internally to the positive input of the servo error amp.

(3) Input Command Signal (V_c)—The analog voltage applied to pin 3, V_c, determines the operating mode. This input signal should be current limited and well filtered to avoid noise pulses triggering spurious operating conditions.

a) Turn-on:—When power is first applied the part normally comes up in the Off state. If V_C is raised above V_{CC} so that the input current exceeds 100μa (in the current limited mode), the internal logic circuitry will go into the standby mode and be ready to receive other input commands.

b) Standby—To maintain the part in the standby or control mode, V_C should be maintained in the voltage range for mode A as indicated in the table.

c) Positive Ramp, Set—The voltage that appears on pin 6, V_m, is the internally generated servo drive voltage. This voltage is internally connected to the negative input of the servo error amp.

When V_C is in mode C as indicated in the table, the voltage V_m will increase at a rate given by (0.43 volts)/R_8C_1, where R_8 is the resistor between pins 14 and 15, and C_1 is the capacitor between pin 15 and ground. The capacitor must have a leakage at 8 volts of much less than 0.43v/R_8 under all conditions to minimize the variability of this rate. Rates as low as 50mv/sec are practical.

When V_C is restored from mode C to mode A, the value of the pin 11 voltage, V_s, is stored in the internal memory, and this voltage then appears on pin 6 as the servo drive voltage, V_m.

The mechanism by which the value of V_s is stored is as follows. A digital counter whose output is applied to a DAC is turned on. When the DAC output reaches the level of V_s, the counter is stopped, and the DAC output appears on pin 6. The frequency that the counter counts is generated by an internal oscillator connected to a capacitor on pin 5. The oscillator frequency is inversely proportional to capacitor size, and .001μf produces about 75 kHz. This frequency determines the time that it takes for the DAC output to reach the V_s level and set. Since the maximum count is 256, a frequency of 75kHz (period = 13.3μs) provides a maximum set time of 3.4ms. Frequencies higher than 100kHz are not recommended.

d) Disable, Return to Memory—For normal servo and logic operation the voltage on the Disable input, pin 12, must be less than $V_{CC}/2$. If this voltage is raised above $V_{CC}/2$, the device reverts to the standby mode, except that the internal memory voltage, V_m, remains set at its current level. If the input command voltage, V_C, is then reduced momentarily to mode B, as given in the table, the servo drive voltage, V_m, on pin 6 will start at the current value of V_s and increase at the positive ramp rate described earlier until it reaches the level stored in memory. It will then remain at this value. A Disable-Return sequence when V_s is greater than the memory level will restore V_m to the memory level.

e) Memory Erase, Set—If the value of V_C is reduced to mode D given in the table, the part will revert to the standby mode and memory is erased. If V_C then returns to mode A, the memory and the servo drive voltage, V_m, will be set at the current value of V_s in the same manner as described earlier for the Positive Ramp, Set function.

f) Off—If the value of V_C is reduced to the Off level as given in the table, the device reverts to the inactive state until turned on again as described earlier.

g) Low Level Lockout—The device will revert to the standby condition whenever the value of the F/V output voltage, V_s, drops below the LLLO voltage, which is approximately 1.5 volts. However, the internal memory voltage is maintained. A Disable-Return sequence after V_s again rises above the LLLO voltage, will return the voltage V_m to the memory level in the manner described earlier.

h) Command-Delay—When the command voltage, V_C, changes from the standby level as described above, the logic will not see the change for a period of time given in all but one case by the following equation:

$$t_d = \frac{V_{CC}\,C_3}{(182\mu a)},$$

where C_3 is a capacitor that must be inserted between pin 4 and ground. C_3 = .68μf produces a delay of t_d = 30ms with nominal V_{CC}. The exception to this formula is the delay for the Return to Memory function. This delay is given by:

$$t_{dr} = \frac{V_{CC}\,C_3}{27\ \mu a},$$

so that a typical delay with C_3 = .68μf is 200ms. These delays are designed to eliminate switch bounce problems, as well as other noise that might appear on the input command signal. In a relatively noise free environment, C_3 may be small, reducing the delay times.

(4) Error Amplifier—This amplifier has a gain of aproximately unity. The differential inputs are connected as described above, so that the output, which appears on pin 16, is approximately $V_s - V_m$. The current drawn from pin 16 should be less than ±50μa. The maximum linear voltage swing is about ±0.5 volts. The output is referenced to a level roughly equal $V_{CC}/2$, which is typically equal to the reference level on pin 17. Output currents from pin 17 should also be limited to ±50μa maximum.

(5) Operational Amplifier—The non-inverting input of this amplifier is pin 20, the inverting input is pin 18, and the output is pin 19. The output is internally connected to the input of the deadband circuit. The output impedance at pin 19 is high, typically 600K, so that for loads on pin 19 of 100K or less, this becomes a transconductance amplifier. The amplifier input impedance is greater than one megohm, and the input bias current is typically less than 1μa. Low frequency open circuit output gain is typically 150, with a bandwidth of about 10kHz.

(6) Deadband Circuit—The input of this circuit comes from the Op Amp output, as described above. It is a differential amplifier with the second input internally connected to a voltage approximately equal to $V_{CC}/2$. The input on pin 19 can be forced to any desired level between zero and V_{CC} by external circuitry, if desired, without damaging the part. The maximum drive current required to do this is typcially ±100μa. The circuit deadband is typically ±0.6 volts relative to $V_{CC}/2$. The circuit outputs appear on pins 21 and 22. These outputs are activated by the logic circuitry when it is in one of the control modes. If the pin 19 voltage is above the upper deadband level in the active mode, both outputs will be high. If the pin 19 voltage is between the two deadband levels, pin 21 will be high, and pin 22 low. If the pin 19 voltage is below the lower deadband voltage, both outputs will be low.

When deactivated by the logic, both outputs are low. The signal output on pin 23 indicates the logic state and is low when the pin 21 and 22 outputs are active. The pin 21, 22, and 23 outputs are essentially open collector outputs for voltages below 5 volts, with a current sinking capability typically better than 20ma.

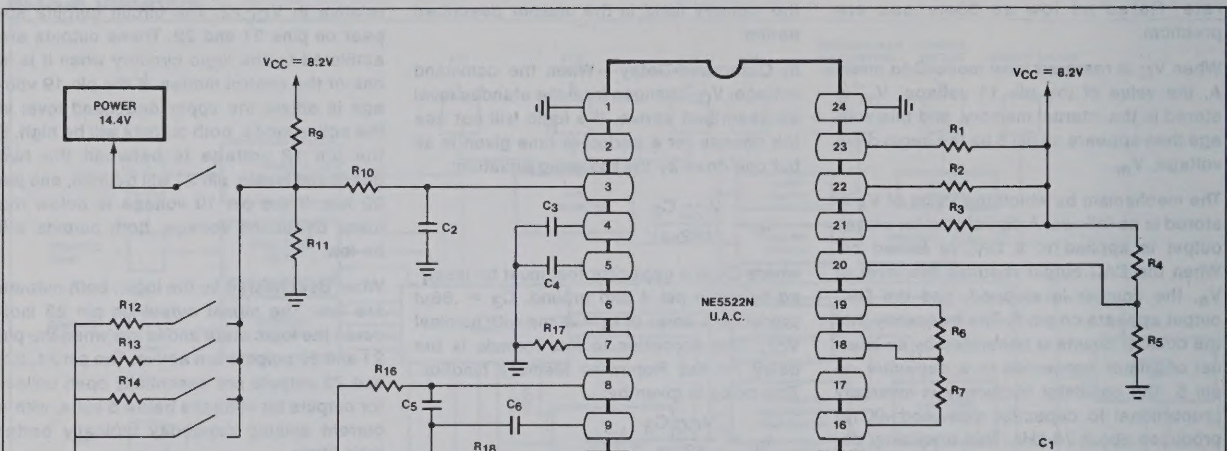
(7) Motor Speed Control—In a typical speed control application an a-c tach signal is fed to the F/V input, pin 8, producing a d-c tach signal on pin 11 (V_s). This is compared to the servo drive voltage, V_m, on pin 6 in the error amplifier. The servo loop gain is established using the op amp with the negative input, pin 18, connected thru a suitable resistor (typically greater than 10kΩ) to the error amp output, pin 16. A feedback resistor between pins 19 and 18 sets the op amp gain. An acceleration feedback signal from the servo is also applied thru a suitable impedance to the negative input, pin 18. The sawtooth ripple from the F/V is amplified by the op amp sufficiently so that it sweeps thru one or both of the deadband circuit thresholds, producing pulse width modulated outputs on pin 21 and 22, the pulse widths increasing as the d-c level at pin 19 increases. The frequency of the pulse width modulation is, of course, the frequency of the ripple, which is twice the input tach frequency.

The pin 21 and 22 outputs are typically applied to some type of "bang-bang" type servo control in such a way that acceleration occurs when both outputs are high and deceleration occurs when both outputs are low.

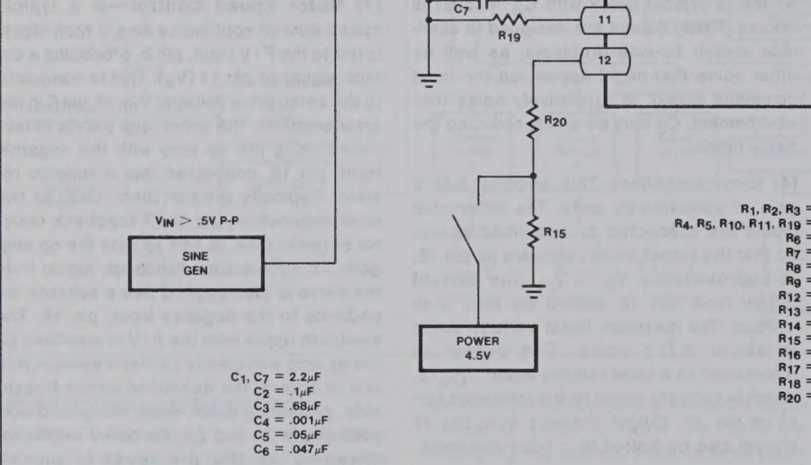
DC MOTOR SPEED CONTROL APPLICATION

This circuit was developed to independently control the speed of two or more model trains running on the same pair of tracks. Each train is equipped with a receiver tuned to a different carrier frequency. The carrier frequency is modulated at the transmitter by a variable audio frequency which carries the speed and direction information. The train which is tuned to the carrier frequency being

TYPICAL TEST CIRCUIT


VCC = 8.2V
POWER 14.4V
R9
R10
C2
R11
R12
R13
R14
R16
C5
VIN > .5V P-P
SINE GEN
C3
C4
R17
C6
R18
C7
R19
R20
R15
POWER 4.5V
NE5522N U.A.C.
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VCC = 8.2V
R1
R2
R3
R4
R6
R5
R7
C1
R8
VCC = 8.2V
R1, R2, R3 = 1.2K
R4, R5, R10, R11, R19 = 10K
R6 = 1.5M
R7 = 15K
R8 = 24M
R9 = 560Ω
R12 = 2.2K
R13 = 680Ω
R14 = 120Ω
R15 = 1K
R16 = 8.2K
R17 = 43K
R18 = 150K
R20 = 51K
C1, C7 = 2.2μF
C2 = .1μF
C3 = .68μF
C4 = .001μF
C5 = .05μF
C6 = .047μF

TYPICAL PERFORMANCE CHARACTERISTICS



transmitted will receive this signal and provide an enable command to the receiver circuit. The modulating audio frequency signal is demodulated and decoded. Train speed (motor voltage) adjusts to the decoded information. When the carrier frequency is removed the receiver stores the last decoded signal and the train (motor) maintains the set speed until it is again addressed using its carrier frequency and the speed can be adjusted.

THEORY OF OPERATION

(A) Transmitter—The transmitter's carrier frequency was selected to be in the 100 to 500kHz range and the modulating frequency in the 1 to 4kHz range. A simple oscillator/modulator was built using an NE556N dual timer.

The two required frequencies are generated by connecting each timer in the astable mode. These circuits generated square waves whose frequency is adjusted by changing the variable resistors (figure 2) R_A and R_B respectively. The oscillation frequency is approximately equal to 0.72 divided by the RC product of the charging and discharging path. For the low frequency oscillator: fm = .72/(5K + R_A)(.02μ) and for the high frequency oscillator: fc = .72/(3K + R_B)(500p). This gives a carrier frequency which can be adjusted between 110 and 480kHz. Each carrier frequency is adjusted to its receiver frequency which is set by a fixed resistor. This was done to eliminate any adjustments at the receiver. The low frequency is variable between 1 and 3kHz. Modulation of the high frequency by the low is accomplished by connecting the low frequency output to the control voltage input of the high frequency oscillator thru a resistor whose value sets the amount of modulation.

The modulated signal is connected to the train track thru an isolation transformer. A variable resistor Rc is connected in series with the output to adjust the output signal.

(B) Receiver—The receiver is broken down into 5 sections for easier analysis (see figure 1);
(1) Receiver/Demodulator
(2) Frequency Converter/Memory
(3) Decoder
(4) Motor Driver
(5) Power Circuits

(1) Receiver/Demodulator (R/D)—An NE567N Phase Locked Loop is used to perform this function. The lock frequency is set by the resistor R whose value is 1.1 X 10^9 divided by the desired carrier frequency. Two signals from the R/D circuit are used to drive the next circuit block; a logic low level on pin 8 when the tuned carrier frequency is detected and the demodulated low frequency appearing on pin 1.

(2) Frequency Converter/Memory—An NE5522N Universal Analog Controller (UAC) is used for this function. The low frequency signal from the R/D circuit is amplified and applied to the f to V converter of the UAC. A d.c. voltage proportional to the input frequency is generated. The conversion factor is set by the capacitor on pin 9 and the resistor on pin 10; its value is: $V_{dc}/f = 4 R_{10}C_9$. Thus for the circuit values shown, V_{dc}/f = 1.72mV/Hz; at 1kHz, 1.72V, at 2kHz 3.44V and 3kHz 5.16V.

When the enable signal is removed (carrier frequency turned off) the converted D.C. voltage is stored and is continuously available on pin 6 of the UAC.

(3) Decoder—An NE324N quad op amp is used to decode the d.c. level from the UAC. One amplifier is connected to give an output which is proportional to the d.c. level. Its output goes to zero at about 3.65V. Another amplifier is connected so that its output is inversely proportional to the d.c. level below 3.25 volts. A deadband is set so that both amplifier outputs are at zero between 3.25 and 3.65V. A transfer characteristic of these two amplifiers is shown in figure 3.

The remaining two amplifiers are used as comparators, each going high when the amplifier driving it goes positive. Thus when the UAC pin 6 voltage is greater than 3.65V, amplifier (4) and comparator (2) have positive output voltages and when this voltage is less than 3.25V amplifier (3) and comparator (1) have positive output voltages.

(4) Motor Driver—The motor driver consists of four NPN transistors connected in an H bridge configuration. The bases of the upper transistors are driven by the decoder amplifier output voltages which are proportional to the UAC voltage as previously described. The bases of the lower transistors are driven by the decoder comparators and are either on or off depending on the UAC voltage above the deadband, inversely proportional to the UAC voltage below the deadband, and zero in the deadband. A system transfer function is shown in figure 4.

(5) Power Circuits—The power supply for the IC's and the transistor drivers is supplied from a bridge rectifier. The transistor bridge and motor are supplied with rectified unfiltered 60Hz. A filtered, regulated 8 volt d.c. supply is used for the IC's.

CARRIER CURRENT
MULTICHANNEL PROGRAMABLE
D.C. MOTOR SPEED AND DIRECTION CONTROL

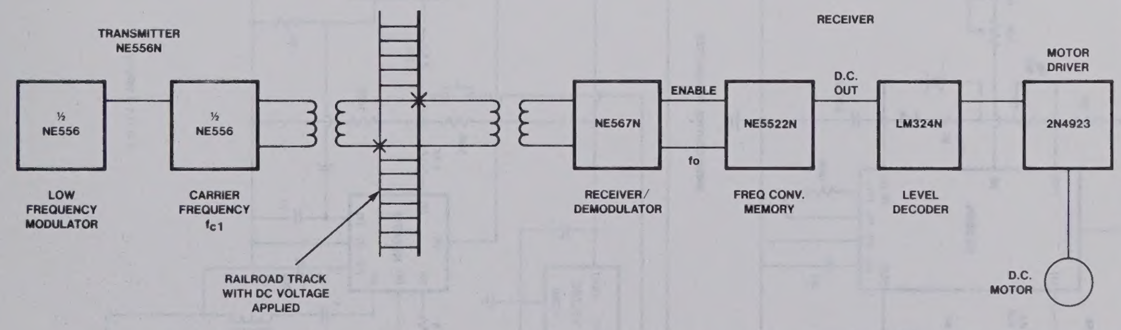
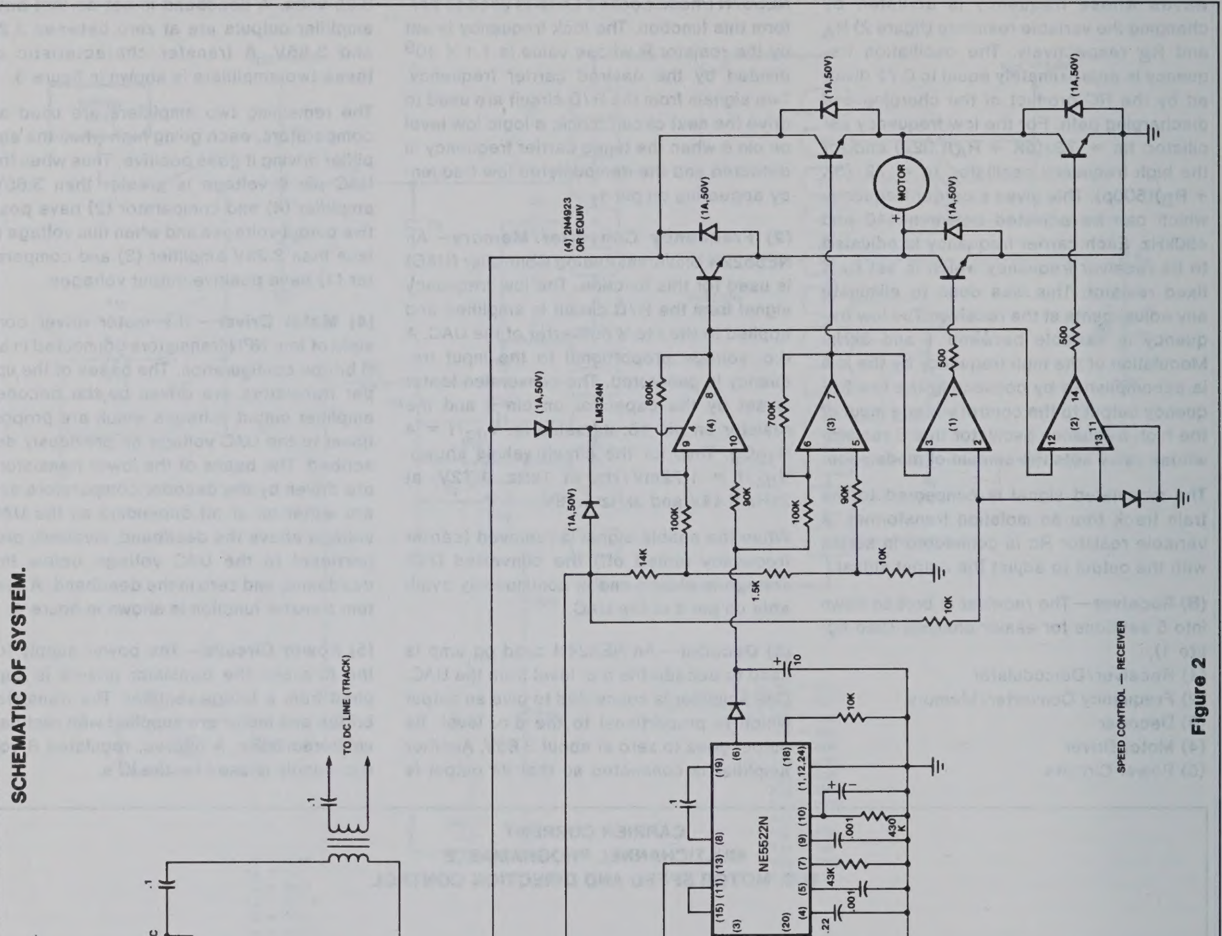


Figure 1

APPLICATION—REMOTE DC MOTOR SPEED CONTROL—MODEL TRAIN


8V D.C.
5K
RB 10K
10K
RC
.1
5K
500 pF
(4,10,14)
(13)
(9)
(8,12)
(11)
(5)
(7)
(3)
(2,6)
(1)
NE556N
150K
.01
5K
RA 20K
5K
.02
10
TO DC LINE (TRACK)
.1
SPEED CONTROL TRANSMITTER
(IN)
(OUT)
78L08S
(COM)
500
.1
(1A,50V)
(1A,50V)
(1A,50V)
(1A,50V)
(1A,50V)
TO LOW VOLTAGE 60 #Z
1:1
.1
R
.001
(5)
(6)
(3)
(2)
(7)
(1)
(8)
(4)
NE567N
.005
.01
.1
5.6K
6.8K
100K
10K
10K
(20)
(4)
(5)
(7)
(9)
(10)
(3)
(15)
(11)
(13)
(8)
(19)
(6)
(18)
(1,12,24)
NE5522N
.22
.001
43K
.001
430K
.1
10
1.5K
4K
100K
(1A,50V)
100K
600K
(4) 2N4923 OR EQUIV
LM324N
9
(4)
8
10
100K
90K
100K
6
(3)
7
5
90K
10K
500
(1)
1
2
10K
500
(2)
14
12
13
11
MOTOR
(1A,50V)
(1A,50V)
(1A,50V)
SPEED CONTROL RECEIVER
R = (1.1 X 10⁹)/fc

SCHEMATIC OF SYSTEM

Figure 2

NE5522-N

DECODER AMPLIFIER CHARACTERISTIC

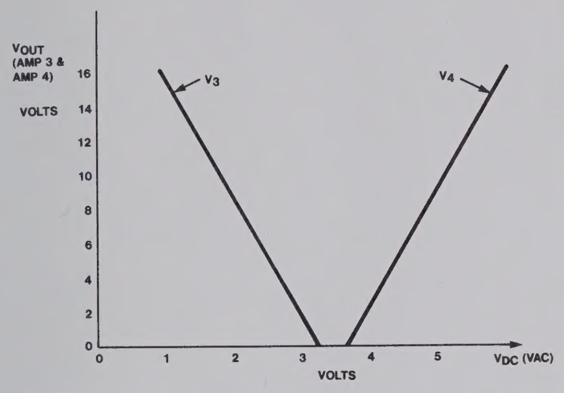


Figure 3

SYSTEM TRANSFER FUNCTION

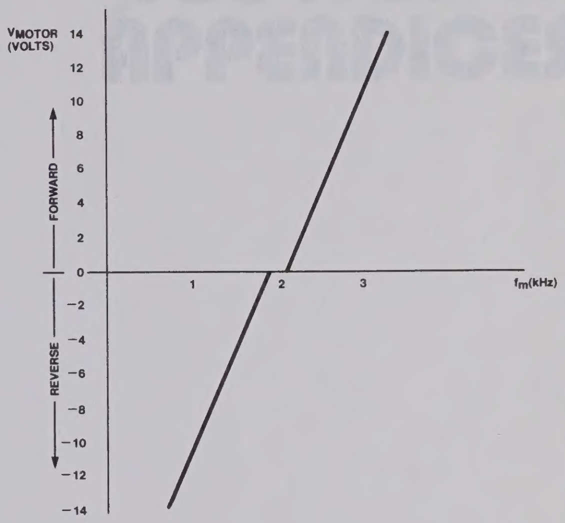


Figure 4

SECTION 17
APPENDICES

MILITARY

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES						
	CAN		DUAL-IN-LINE				
	8-PIN	10-PIN	8-PIN	14-PIN	16-PIN	18-PIN	24-PIN
PB	—	—	FE	—	—	—	—
CB	—	—	—	F	—	—	—
EB	—	—	—	—	F	—	—
JB	—	—	—	—	—	—	F
DB	—	—	—	W	—	—	—
FB	—	—	—	—	W	—	—
ZC	—	—	—	—	—	—	Q
GC	H	—	—	—	—	—	—
IC	—	H	—	—	—	—	—
VB	—	—	—	—	—	I	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	X	X	X
8T	—	X	X
93XX	X	X	X
96XX	—	X	X
Analog	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity or running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond.B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*
Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling* *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)	1010, Cond. C; (10 cycles, −65°C to +150°C)	100%	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30kg in Y1 Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10^{-8}CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ −55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard	10%	10% 3% Funct"l	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per pkg. group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constand acceleration.	Every 3 months per µcircuit type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

LINEAR DEVICES

DEVICE	DESCRIPTION	PACKAGE*	
		DIP	CAN
	OPERATIONAL AMPLIFIERS		
LF155	JFET Op Amp		H
LF156	JFET Op Amp		H
LH2101A	Dual Op Amp	F	
LM101/A	Hi Perf Op Amp	F	H
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		H
MC1556	Hi Perf Op Amp	F	H
MC1558	Dual Op Amp	F	H
SE530	Hi Slew Op Amp	F	H
SE532	Dual Op Amp		H
SE5512	Dual Op Amp	FE	H
SE5532	Dual Op Amp	F,FE	H
SE5532A	Dual Op Amp	FE	
SE5534	Lo Noise Op Amp	F,FE	H
SE5534A	Lo Noise Op Amp	FE	H
SE5537	Sample and Hold Amp	FE	H
SE5539	High Freq Op Amp	F	—
μA747	Dual Op Amp	F	H
	COMPARATORS		
SE521	Dual Differential Comparator	F	
SE522	Dual Differential Comparator	F	
SE527	Voltage Comparator	F	H
SE529	Voltage Comparator	F	H
LH2111	Dual Voltage Comparator	F	
LM111	Voltage Comparator	F	H
LM139/A	Quad Voltage Comparator	F	
LM193/A	Dual Voltage Comparator		H
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
μA733	Video Amplifier	F	H
	PHASE LOCKED LOOPS		
SE567	Tone Decoder PLL	F	H
SE564	Phase Locked Loop	F	H
	TIMERS		
SE555	Timer	F,FE	H
SE556-1	Dual Timer	F	
SE558	Quad Timer	F	

DEVICE	DESCRIPTION	PACKAGE*	
		DIP/ CAN	CAN
	VOLTAGE REGULATORS		
SE5553	Dual Track Reg	F	H
SE5554	Dual Track Reg	F	H
μA723	Adj Volt Reg	F	H

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	D to A CONVERTERS		
DAC-08	8-Bit Mult DAC	F,Q	H
MC1508-8	8-Bit Mult DAC	F	—
SE5008	8-Bit Mult DAC	F	—
SE5009	8-Bit Mult DAC	F	—
SE5018	8-Bit μP-Comp DAC	F	—
SE5019	8-Bit μP-Comp DAC	F	—
SE5118	8-Bit μP-Comp DAC	F	—
SE5119	8-Bit μP-Comp DAC	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	DUAL LINE RECEIVERS		
DS7820/A	Dual Line Receiver	F	—
DS7830/A	Dual Diff Line Driver	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	MOS FET SWITCH		
SD210	Switch N-Channel Enhance	EE	—
SD211	Switch N-Channel Enhance	EE	—
SD5002	Quad Analog Switch	I	

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
	SMPS CONTROL CIRCUITS		
SE5560	SMPS Controller	F	—
SG1524	Reg Pulse Width Mod	F	—

JAN M – 38510			
DEVICE	SLASH SHEET	PKG	QUAL STATUS
SE555	10903BCB	F	QPL 1
SE555	10903BPB	FE	QPL 1
SE555	10901BGC	H	QPL 1
SE556-1	10902BCB	F	QPL 1
LH2101A	10105BEB	F	QPL 1
LM101A	10103BCB	F	QPL 1
LM101A	10103BPB	FE	QPL 1
LM101AH	10103BGC	H	QPL 1
μA741	10101BGC	H	QPL 1
μA747	10101BGC	H	QPL 1
LM124	11005BCB	F	1980
DAC-08	11301BCB	F	1980
DAC-08A	11302BCB	F	1980
SE5537			1980
SG1524			1980

NOTES
F = Cerdip
H = TO-5

LINEAR INDUSTRY CROSS REFERENCE

FAIRCHILD	SIGNETICS
μA111	LM111
μA139	LM139
μA733	μA733
μAF155/156	LF155/156
μA101	LM101
μA101A	LM101A
MC1556	MC1556
μA1558	MC1558
μA747	μA747
MC1555	SE555
μA556	SE556
μA109	LM109
μA79XX	79XX(7)
μA723	μA723

MOTOROLA	SIGNETICS
MLM111	LM111
MC1733	μA733
LF155/56	LF155/156
MLM101	LM101
MLM101A	LM101A
MC1558	MC1558
MC1747	μA747
MC3556	SE556
MLM109	LM109
MC78XX	78XX(7)
MC79XX	79XX(7)
MC1723	μA723
MC1508	MC1508-8

NATIONAL	SIGNETICS
LM161	SE527
LH2111	LH2111
LM111	LM111
LM119	LM119
LM139	LM139
LM193	LM193/193A
LM733	μA733
LF155/56	LF155/156
LH2101A	LH2101A
LH2108A	LH2108A
LM101A	LM101
LM101	LM101A
LM124	LM124
LM158	LM158
LM1558	MC1558
LM1581	SE532
LM747	μA747
LM567	SE567
DM7820	DM7820
DM7830	DM7830
LM555	SE555
LM109	LM109
LM723	μA723

PMI	SIGNETICS
SSS1508	MC1508-8
DAC-08	SE5008

RAYTHEON	SIGNETICS
LM111	LM111
LM139	LM139
RM733	μA733
LF155/56/57	LF155/156
LM101	LM101
LM101A	LM101A
LM124	LM124
RM1556	MC1556
RM1558	MC1558
RM747	μA747
RM555	SE555
LM109	LM109
RM723	μA723

T.I.	SIGNETICS
LM111	LM111
SN52733	μA733
LF155/56	LF155/156
SN52101A	LM101A
SN55182	DM7820
SN55183	DM7830
SN52555	SE555
SE556	SE556
LM109	LM109
μA79XX	μA79XX(7)
SN52723	μA723

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminature packages.
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

Hermetic Only

10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb .010 inches.
16. Maximum glass climb or lid skew is .010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION[1]
Standard Dual-In-Line			
8	NE	162/65	
14	NH	150/65	TO-116/MO-001
16	NJ	137/53	MO-001
18	NK	135/53	
20	NL	135/53	
22	NM	120/53	
24	NN	116/53	MO-015
24	NNE NNF	120/60	Slim Line
28	NQ	116/53	MO-015
40	NW	110/50	MO-015
Power Dual-In-Line			
14	NHA[2]	95/33	Butterfly
16	NJA[2]	95/33	Butterfly
18	NKA[2]	90/26	Butterfly
20	NLA[2]	90/26	Butterfly
24	NNA[2]	60/23	Heatsink
28	NQA[2]	56/21	Heatsink
SO Packages			
8	DE	110	SO-8
14	DH	100	SO-14
16	DJ	100	SO-16

NOTES
1. Dual-in-Line packages unless otherwise described.
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads.

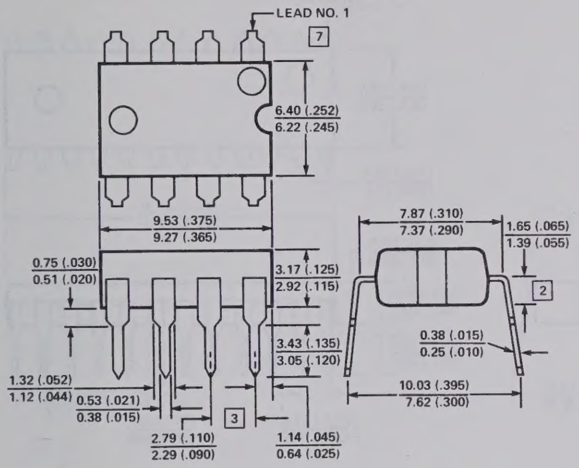
HERMETIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc}(°C/W)	DESCRIPTION[1]
Metal Headers			
3	HBA	100/20	TO-5 Header
4	EC	100/20	TO-46 Header
4	EE	150/25	TO-72 Header
8	HEA/HEB	150/25	TO-5 Header
10	HFB/HFA	150/25	TO-5/TO-100 Header, Short Can
10	HFD/HFC	150/25	TO-5/TO-100 Header, Tall Can
Flat Packs			
10	QF	230/55	Flat Ceramic
10	WF	240/50	Flat Ceramic
14	QHA	185/45	Flat Ceramic Laminate
14	WH	205/50	Flat Ceramic
16	QJA	170/45	Flat Ceramic Laminate
16	RJA	133/30	Flat Ceramic, BeO
16	WJ	200/50	Flat Ceramic
18	RKA	107/22	Flat Ceramic, BeO
24	QNA	155/44	Flat Ceramic Laminate
24	RNA	107/22	Flat Ceramic, BeO
24	WN	155/40	Flat Ceramic
28	RQA	107/22	Flat Ceramic, BeO
40	RWA	95/20	Flat Ceramic, BeO
Cerdip Family			
8	FE	110/30	Dual-in-Line Ceramic
14	FH	110/30	Dual-in-Line Ceramic
16	FJ	100/30	Dual-in-Line Ceramic
18	FK	93/27	Dual-in-Line Ceramic
20	FL	90/25	Dual-in-Line Ceramic
22	FM	75/27	Dual-in-Line Ceramic
24	FN	60/26	Dual-in-Line Ceramic
28	FQ	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
8	IEA	100/30	Dip Laminate
14	IHA	95/25	Dip Laminate
16	IJA	90/25	Dip Laminate
18	IKA/IKB	88/25	Dip Laminate
22	IMA	80/25	Dip Laminate
24	INC/INH	65/25	Dip Laminate
28	IQA	60/25	Dip Laminate
28	GQ*	90/35	Chip Carrier
40	IWA	55/25	Dip Laminate
44	GX*	75/30	Chip Carrier
48	JY*	55/25	Dual-in-Line Ceramic
50	IZA	42/20	Dip Laminate

*Contact factory for Package drawings.

PLASTIC: Standard and Power Dual-In-Line

NE Package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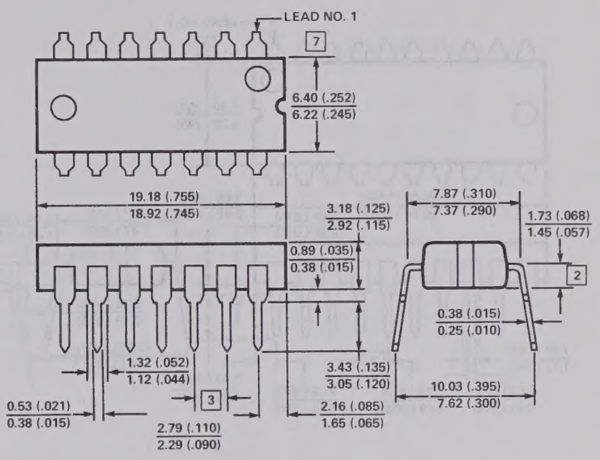
7
6.40 (.252)
6.22 (.245)
9.53 (.375)
9.27 (.365)
7.87 (.310)
7.37 (.290)
1.65 (.065)
1.39 (.055)
0.75 (.030)
0.51 (.020)
3.17 (.125)
2.92 (.115)
2
3.43 (.135)
3.05 (.120)
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
10.03 (.395)
7.62 (.300)
3
2.79 (.110)
2.29 (.090)
1.14 (.045)
0.64 (.025)

NH Package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7
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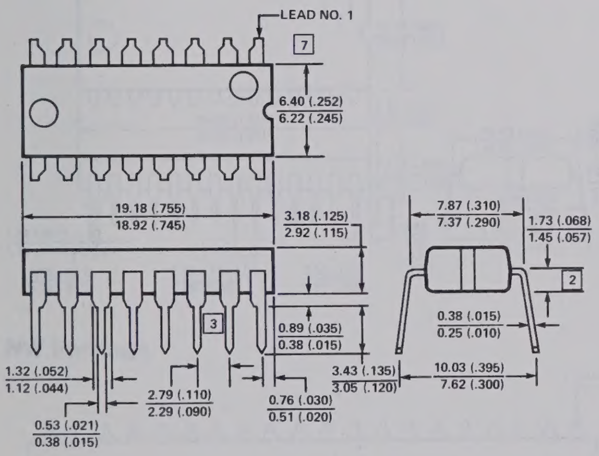
6.22 (.245)
19.18 (.755)
18.92 (.745)
3.18 (.125)
2.92 (.115)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
0.89 (.035)
0.38 (.015)
2
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
3.43 (.135)
3.05 (.120)
10.03 (.395)
7.62 (.300)
0.53 (.021)
0.38 (.015)
3
2.16 (.085)
1.65 (.065)
2.79 (.110)
2.29 (.090)

NJ Package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7
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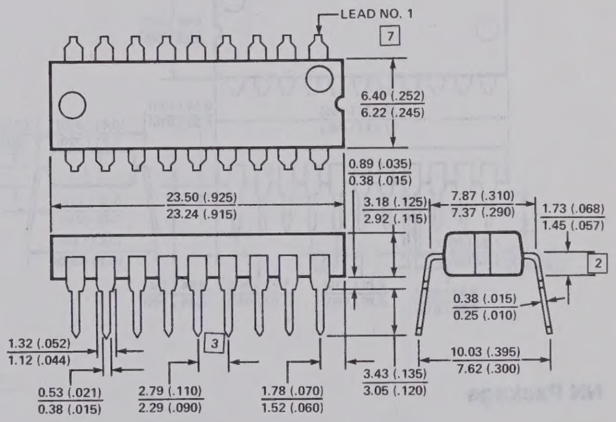
6.22 (.245)
19.18 (.755)
18.92 (.745)
3.18 (.125)
2.92 (.115)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
2
3
0.89 (.035)
0.38 (.015)
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
2.79 (.110)
2.29 (.090)
3.43 (.135)
3.05 (.120)
10.03 (.395)
7.62 (.300)
0.76 (.030)
0.51 (.020)
0.53 (.021)
0.38 (.015)

NK Package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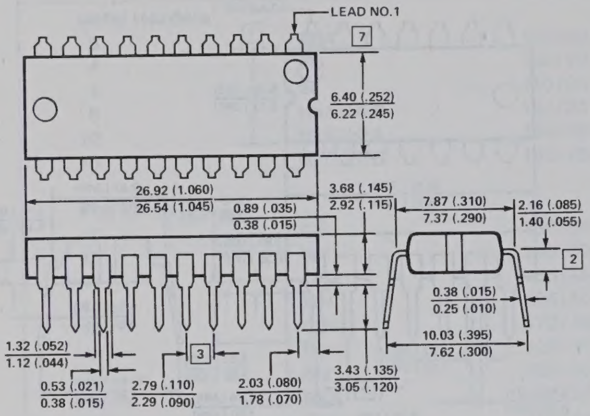
7
6.40 (.252)
6.22 (.245)
0.89 (.035)
0.38 (.015)
23.50 (.925)
23.24 (.915)
3.18 (.125)
2.92 (.115)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
2
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
3
10.03 (.395)
7.62 (.300)
3.43 (.135)
3.05 (.120)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.78 (.070)
1.52 (.060)

PLASTIC: Standard and Power Dual-In-Line (cont'd.)

NL Package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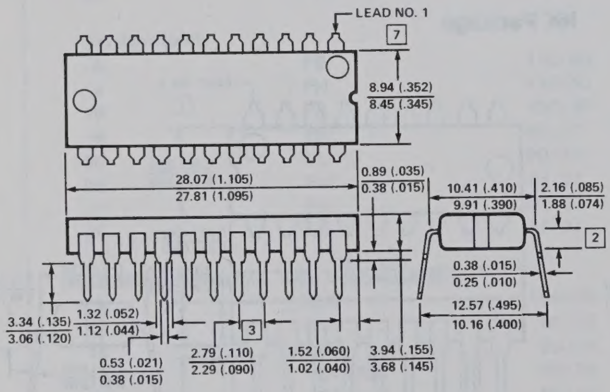
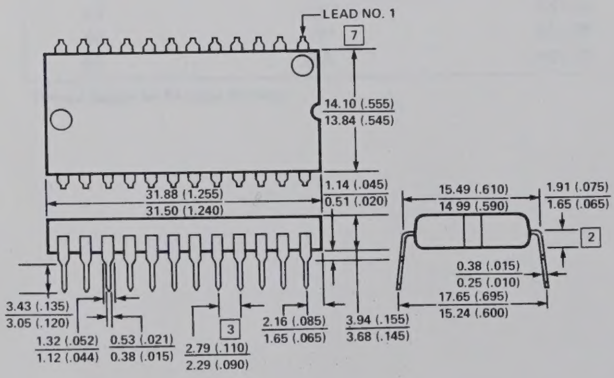
7
6.40 (.252)
6.22 (.245)
26.92 (1.060)
26.54 (1.045)
0.89 (.035)
0.38 (.015)
3.68 (.145)
2.92 (.115)
7.87 (.310)
7.37 (.290)
2.16 (.085)
1.40 (.055)
2
0.38 (.015)
0.25 (.010)
10.03 (.395)
7.62 (.300)
1.32 (.052)
1.12 (.044)
3
3.43 (.135)
3.05 (.120)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.03 (.080)
1.78 (.070)

NM Package

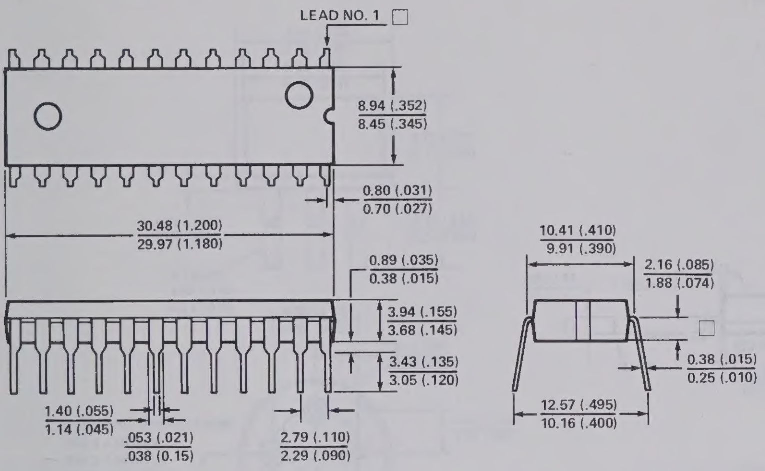

LEAD NO. 1
7
8.94 (.352)
8.45 (.345)
0.89 (.035)
0.38 (.015)
28.07 (1.105)
27.81 (1.095)
10.41 (.410)
9.91 (.390)
2.16 (.085)
1.88 (.074)
2
0.38 (.015)
0.25 (.010)
12.57 (.495)
10.16 (.400)
3.34 (.135)
3.06 (.120)
1.32 (.052)
1.12 (.044)
3
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.52 (.060)
1.02 (.040)
3.94 (.155)
3.68 (.145)

NN Package

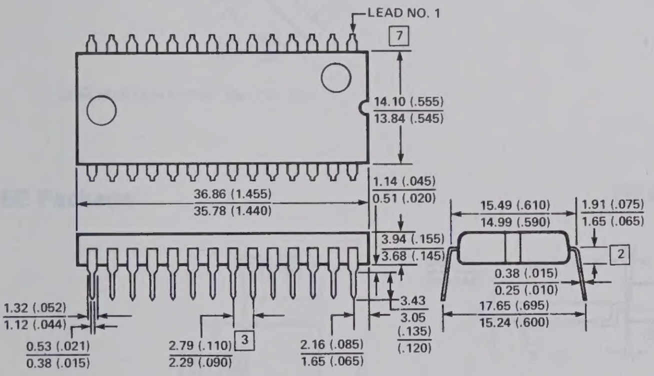

LEAD NO. 1
7
14.10 (.555)
13.84 (.545)
1.14 (.045)
0.51 (.020)
31.88 (1.255)
31.50 (1.240)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
2
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
3.43 (.135)
3.05 (.120)
3
2.16 (.085)
1.65 (.065)
3.94 (.155)
3.68 (.145)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)

PLASTIC: Standard and Power Dual-In-Line (cont'd.)

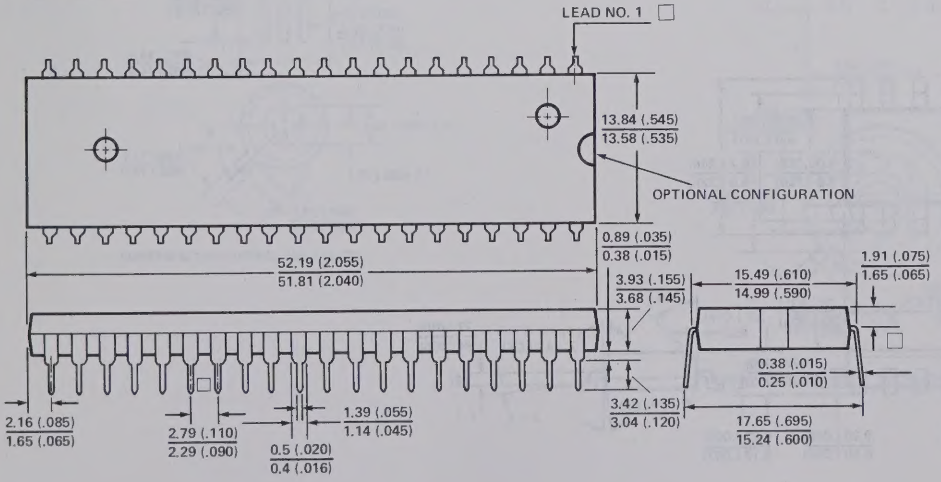
NNE/NNF Package


LEAD NO. 1 ☐
8.94 (.352)
8.45 (.345)
0.80 (.031)
0.70 (.027)
30.48 (1.200)
29.97 (1.180)
0.89 (.035)
0.38 (.015)
3.94 (.155)
3.68 (.145)
3.43 (.135)
3.05 (.120)
1.40 (.055)
1.14 (.045)
.053 (.021)
.038 (0.15)
2.79 (.110)
2.29 (.090)
10.41 (.410)
9.91 (.390)
2.16 (.085)
1.88 (.074)
☐
0.38 (.015)
0.25 (.010)
12.57 (.495)
10.16 (.400)

NQ Package

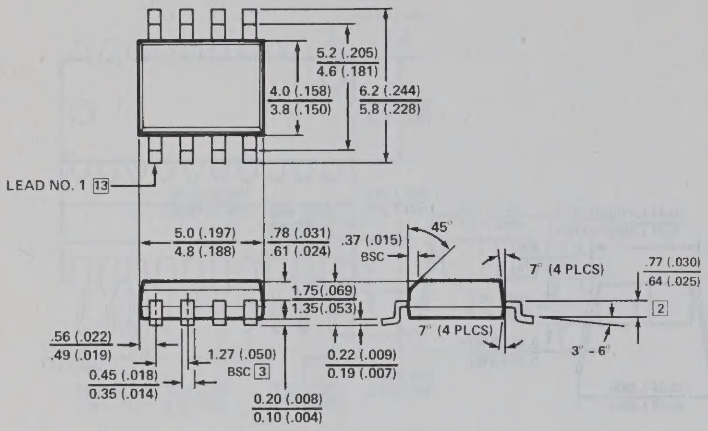

LEAD NO. 1
7
14.10 (.555)
13.84 (.545)
1.14 (.045)
0.51 (.020)
36.86 (1.455)
35.78 (1.440)
3.94 (.155)
3.68 (.145)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
2
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
3.43
3.05
(.135)
(.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
3
2.16 (.085)
1.65 (.065)

NW Package

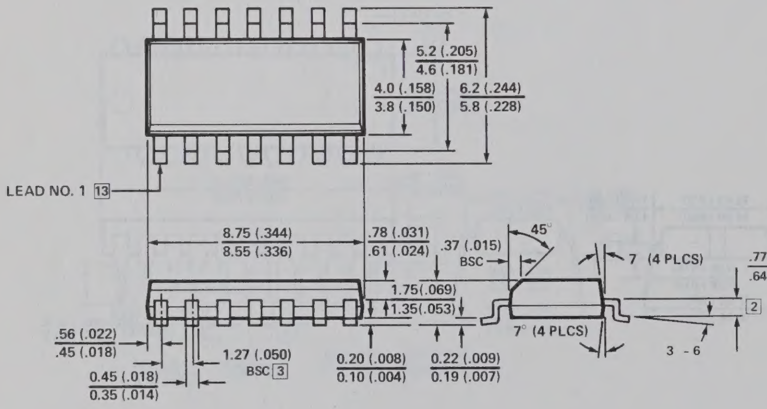

LEAD NO. 1 ☐
13.84 (.545)
13.58 (.535)
OPTIONAL CONFIGURATION
0.89 (.035)
0.38 (.015)
52.19 (2.055)
51.81 (2.040)
3.93 (.155)
3.68 (.145)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
☐
0.38 (.015)
0.25 (.010)
3.42 (.135)
3.04 (.120)
17.65 (.695)
15.24 (.600)
☐
2.16 (.085)
1.65 (.065)
2.79 (.110)
2.29 (.090)
1.39 (.055)
1.14 (.045)
0.5 (.020)
0.4 (.016)

PLASTIC: SO Packages

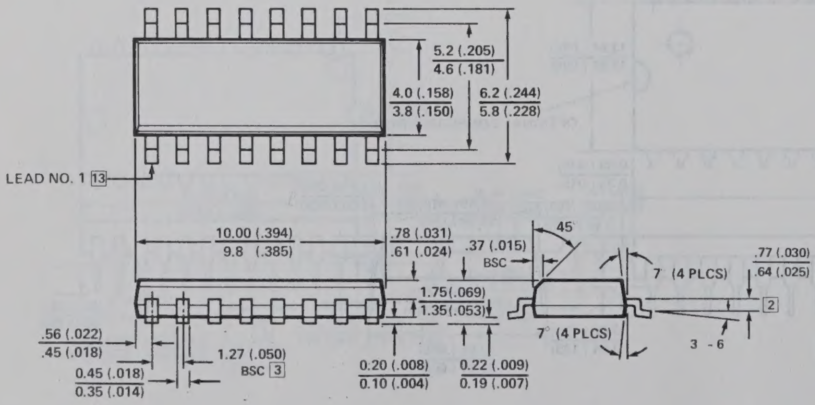
DE Package


5.2 (.205)
4.6 (.181)
4.0 (.158)
3.8 (.150)
6.2 (.244)
5.8 (.228)
LEAD NO. 1 13
5.0 (.197)
4.8 (.188)
.78 (.031)
.61 (.024)
.37 (.015)
BSC
45°
7° (4 PLCS)
.77 (.030)
.64 (.025)
2
1.75(.069)
1.35(.053)
7° (4 PLCS)
3° - 6°
.56 (.022)
.49 (.019)
1.27 (.050)
BSC 3
0.22 (.009)
0.19 (.007)
0.45 (.018)
0.35 (.014)
0.20 (.008)
0.10 (.004)

DH Package

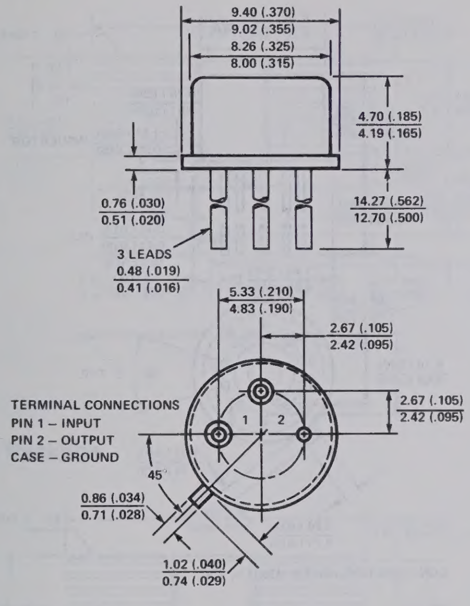

5.2 (.205)
4.6 (.181)
4.0 (.158)
3.8 (.150)
6.2 (.244)
5.8 (.228)
LEAD NO. 1 13
8.75 (.344)
8.55 (.336)
.78 (.031)
.61 (.024)
.37 (.015)
BSC
45°
7 (4 PLCS)
.77 (.030)
.64 (.025)
1.75(.069)
1.35(.053)
2
7° (4 PLCS)
3 - 6
.56 (.022)
.45 (.018)
1.27 (.050)
BSC 3
0.45 (.018)
0.35 (.014)
0.20 (.008)
0.10 (.004)
0.22 (.009)
0.19 (.007)

DJ Package


5.2 (.205)
4.6 (.181)
4.0 (.158)
3.8 (.150)
6.2 (.244)
5.8 (.228)
LEAD NO. 1 13
10.00 (.394)
9.8 (.385)
.78 (.031)
.61 (.024)
.37 (.015)
BSC
45°
7 (4 PLCS)
.77 (.030)
.64 (.025)
1.75(.069)
1.35(.053)
2
7° (4 PLCS)
3 - 6
.56 (.022)
.45 (.018)
1.27 (.050)
BSC 3
0.45 (.018)
0.35 (.014)
0.20 (.008)
0.10 (.004)
0.22 (.009)
0.19 (.007)

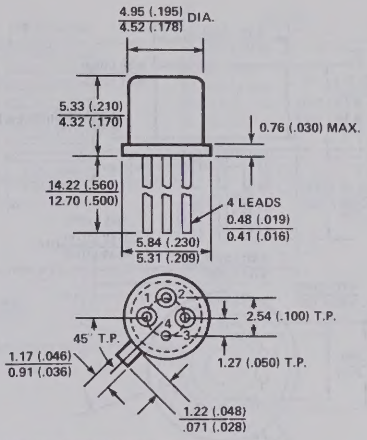
HERMETIC: Metal Headers

HBA Package


9.40 (.370)
9.02 (.355)
8.26 (.325)
8.00 (.315)
4.70 (.185)
4.19 (.165)
0.76 (.030)
0.51 (.020)
14.27 (.562)
12.70 (.500)
3 LEADS
0.48 (.019)
0.41 (.016)
5.33 (.210)
4.83 (.190)
2.67 (.105)
2.42 (.095)
TERMINAL CONNECTIONS
PIN 1 – INPUT
PIN 2 – OUTPUT
CASE – GROUND
2.67 (.105)
2.42 (.095)
1
2
45°
0.86 (.034)
0.71 (.028)
1.02 (.040)
0.74 (.029)

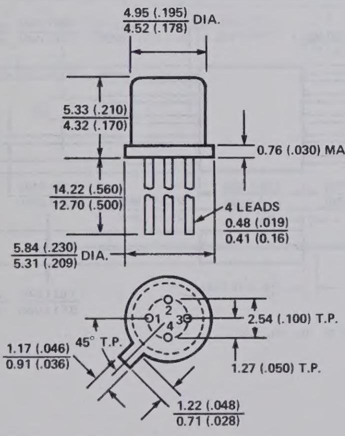
CONSTRUCTION NOTES: 10a, 11a, 12a

EC Package


4.95 (.195)
4.52 (.178)
DIA.
5.33 (.210)
4.32 (.170)
0.76 (.030) MAX.
14.22 (.560)
12.70 (.500)
4 LEADS
0.48 (.019)
0.41 (.016)
5.84 (.230)
5.31 (.209)
1
2
4
3
2.54 (.100) T.P.
45° T.P.
1.17 (.046)
0.91 (.036)
1.27 (.050) T.P.
1.22 (.048)
.071 (.028)

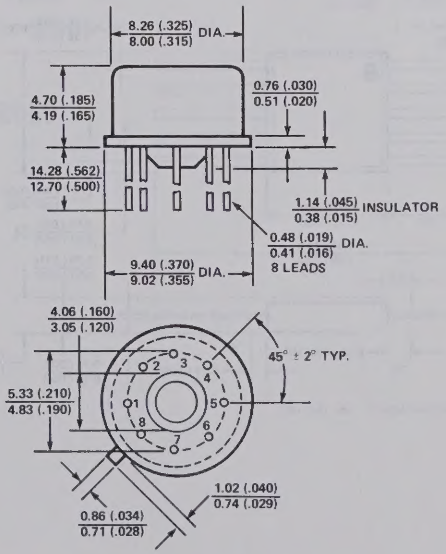
CONSTRUCTION NOTES: 10a, 11a, 12a

EE Package


4.95 (.195)
4.52 (.178)
DIA.
5.33 (.210)
4.32 (.170)
0.76 (.030) MAX.
14.22 (.560)
12.70 (.500)
4 LEADS
0.48 (.019)
0.41 (0.16)
5.84 (.230)
5.31 (.209)
DIA.
1
2
3
4
2.54 (.100) T.P.
45° T.P.
1.17 (.046)
0.91 (.036)
1.27 (.050) T.P.
1.22 (.048)
0.71 (.028)

CONSTRUCTION NOTES: 10a, 11a, 12a

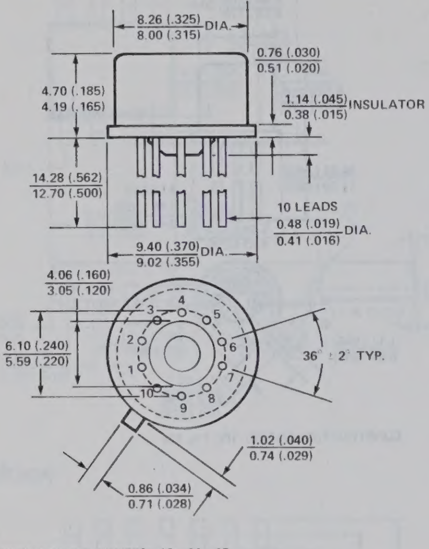
HEA/HEB Package


8.26 (.325)
8.00 (.315)
DIA.
4.70 (.185)
4.19 (.165)
0.76 (.030)
0.51 (.020)
14.28 (.562)
12.70 (.500)
1.14 (.045)
0.38 (.015)
INSULATOR
0.48 (.019)
0.41 (.016)
DIA.
8 LEADS
9.40 (.370)
9.02 (.355)
DIA.
4.06 (.160)
3.05 (.120)
45° ± 2° TYP.
1
2
3
4
5
6
7
8
5.33 (.210)
4.83 (.190)
1.02 (.040)
0.74 (.029)
0.86 (.034)
0.71 (.028)

CONSTRUCTION NOTES: 10a, 11a, 12a

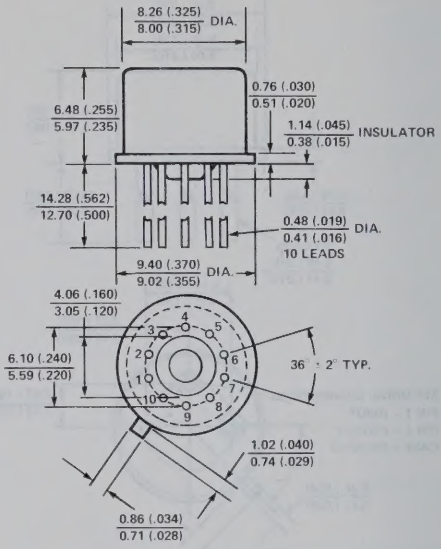
HERMETIC: Metal Headers (cont'd.)

HFB/HFA Package


8.26 (.325) / 8.00 (.315) DIA.
0.76 (.030) / 0.51 (.020)
4.70 (.185) / 4.19 (.165)
1.14 (.045) / 0.38 (.015) INSULATOR
14.28 (.562) / 12.70 (.500)
10 LEADS
0.48 (.019) / 0.41 (.016) DIA.
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
6.10 (.240) / 5.59 (.220)
1
2
3
4
5
6
7
8
9
10
36° ± 2° TYP.
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

CONSTRUCTION NOTES: 10a, 11a, 12a

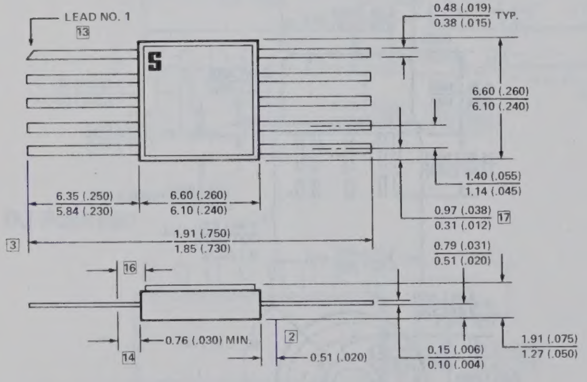
HFD/HFC Package


8.26 (.325) / 8.00 (.315) DIA.
0.76 (.030) / 0.51 (.020)
6.48 (.255) / 5.97 (.235)
1.14 (.045) / 0.38 (.015) INSULATOR
14.28 (.562) / 12.70 (.500)
0.48 (.019) / 0.41 (.016) DIA.
10 LEADS
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
6.10 (.240) / 5.59 (.220)
1
2
3
4
5
6
7
8
9
10
36° ± 2° TYP.
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

CONSTRUCTION NOTES: 10a, 11a, 12a

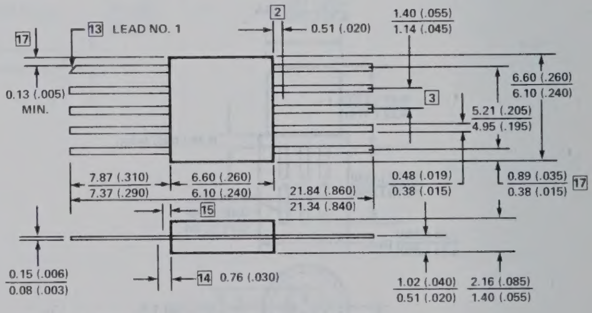
HERMETIC: Flat Packs

QF Package


LEAD NO. 1
13
S
0.48 (.019) / 0.38 (.015) TYP.
6.60 (.260) / 6.10 (.240)
1.40 (.055) / 1.14 (.045)
6.35 (.250) / 5.84 (.230)
6.60 (.260) / 6.10 (.240)
0.97 (.038) / 0.31 (.012)
17
3
1.91 (.750) / 1.85 (.730)
0.79 (.031) / 0.51 (.020)
16
0.76 (.030) MIN.
14
2
0.51 (.020)
0.15 (.006) / 0.10 (.004)
1.91 (.075) / 1.27 (.050)

CONSTRUCTION NOTES: 10c, 11d, 12b

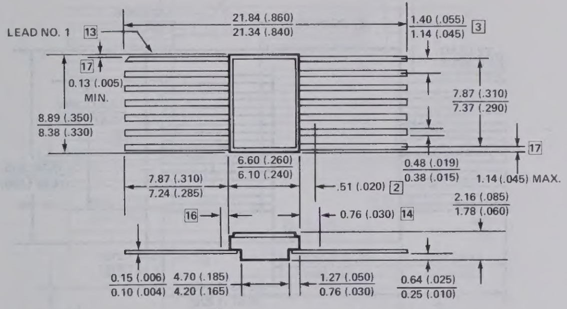
WF Package


2
1.40 (.055) / 1.14 (.045)
17
13 LEAD NO. 1
0.51 (.020)
6.60 (.260) / 6.10 (.240)
0.13 (.005) MIN.
3
5.21 (.205) / 4.95 (.195)
7.87 (.310) / 7.37 (.290)
6.60 (.260) / 6.10 (.240)
0.48 (.019) / 0.38 (.015)
0.89 (.035) / 0.38 (.015)
17
21.84 (.860) / 21.34 (.840)
15
0.15 (.006) / 0.08 (.003)
14 0.76 (.030)
1.02 (.040) / 0.51 (.020)
2.16 (.085) / 1.40 (.055)

CONSTRUCTION NOTES: 10b, 11b, 12b

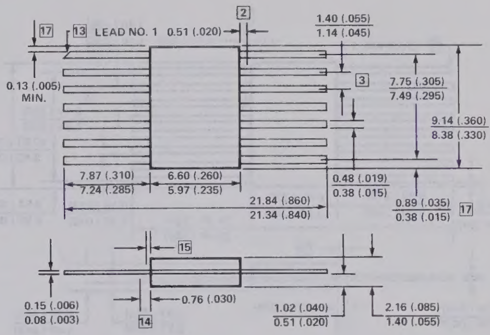
HERMETIC: Flat Packs (cont'd.)

QHA Package


LEAD NO. 1
13
21.84 (.860)
21.34 (.840)
1.40 (.055)
1.14 (.045)
3
17
0.13 (.005)
MIN.
8.89 (.350)
8.38 (.330)
7.87 (.310)
7.37 (.290)
17
6.60 (.260)
6.10 (.240)
0.48 (.019)
0.38 (.015)
1.14 (.045) MAX.
7.87 (.310)
7.24 (.285)
.51 (.020)
2
2.16 (.085)
1.78 (.060)
16
0.76 (.030)
14
0.15 (.006)
0.10 (.004)
4.70 (.185)
4.20 (.165)
1.27 (.050)
0.76 (.030)
0.64 (.025)
0.25 (.010)

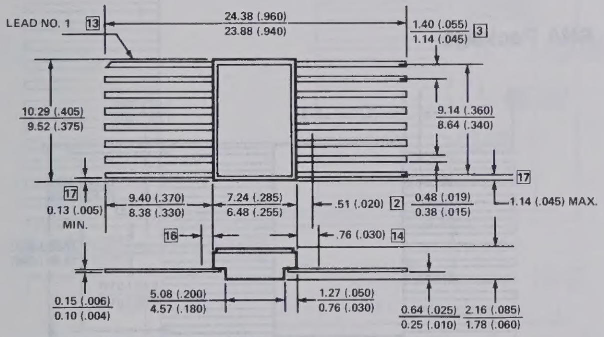
CONSTRUCTION NOTES: 10c, 11d, 12b

WH Package


2
17
13
LEAD NO. 1
0.51 (.020)
1.40 (.055)
1.14 (.045)
3
7.75 (.305)
7.49 (.295)
0.13 (.005)
MIN.
9.14 (.360)
8.38 (.330)
7.87 (.310)
7.24 (.285)
6.60 (.260)
5.97 (.235)
0.48 (.019)
0.38 (.015)
21.84 (.860)
21.34 (.840)
0.89 (.035)
0.38 (.015)
17
15
0.15 (.006)
0.08 (.003)
0.76 (.030)
14
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.40 (.055)

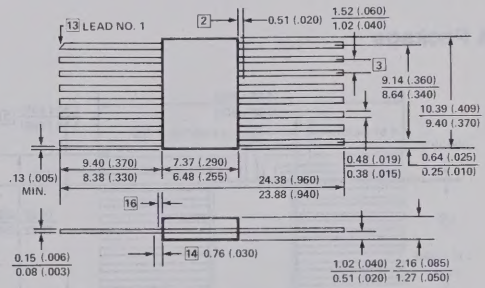
CONSTRUCTION NOTES: 10b, 11b, 12b

QJA Package


LEAD NO. 1
13
24.38 (.960)
23.88 (.940)
1.40 (.055)
1.14 (.045)
3
10.29 (.405)
9.52 (.375)
9.14 (.360)
8.64 (.340)
17
17
0.13 (.005)
MIN.
9.40 (.370)
8.38 (.330)
7.24 (.285)
6.48 (.255)
.51 (.020)
2
0.48 (.019)
0.38 (.015)
1.14 (.045) MAX.
16
.76 (.030)
14
0.15 (.006)
0.10 (.004)
5.08 (.200)
4.57 (.180)
1.27 (.050)
0.76 (.030)
0.64 (.025)
0.25 (.010)
2.16 (.085)
1.78 (.060)

CONSTRUCTION NOTES: 10c, 11d, 12b

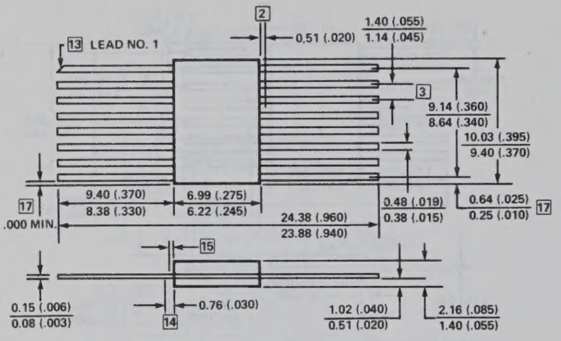
RJA Package


13
LEAD NO. 1
2
0.51 (.020)
1.52 (.060)
1.02 (.040)
3
9.14 (.360)
8.64 (.340)
10.39 (.409)
9.40 (.370)
.13 (.005)
MIN.
9.40 (.370)
8.38 (.330)
7.37 (.290)
6.48 (.255)
24.38 (.960)
23.88 (.940)
0.48 (.019)
0.38 (.015)
0.64 (.025)
0.25 (.010)
16
0.15 (.006)
0.08 (.003)
14
0.76 (.030)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.27 (.050)

RJA CONSTRUCTION NOTES: 10b, 11c, 12b

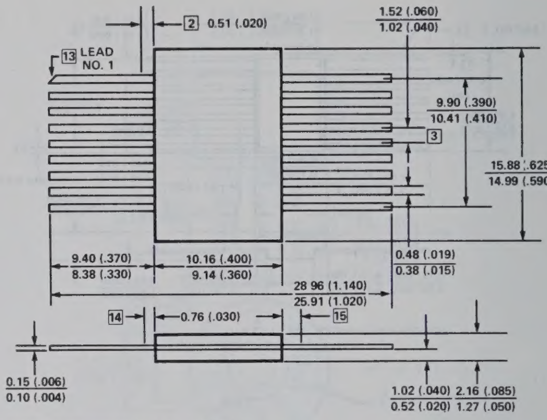
HERMETIC: Flat Packs (cont'd.)

WJ Package


2
13 LEAD NO. 1
0.51 (.020)
1.40 (.055)
1.14 (.045)
3
9.14 (.360)
8.64 (.340)
10.03 (.395)
9.40 (.370)
17
.000 MIN.
9.40 (.370)
8.38 (.330)
6.99 (.275)
6.22 (.245)
24.38 (.960)
23.88 (.940)
0.48 (.019)
0.38 (.015)
0.64 (.025)
0.25 (.010)
17
15
0.15 (.006)
0.08 (.003)
0.76 (.030)
14
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.40 (.055)

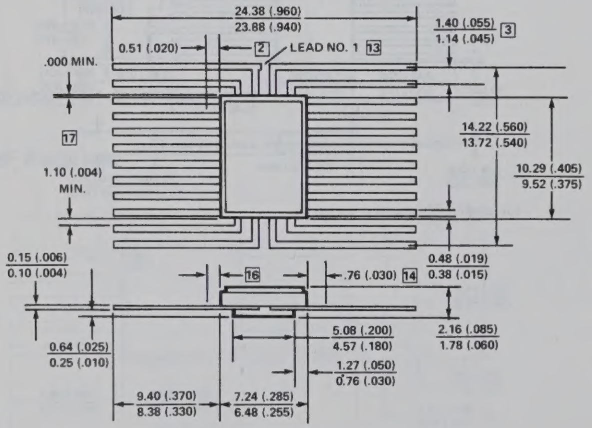
CONSTRUCTION NOTES: 10b, 11b, 12b

RKA Package


2 0.51 (.020)
1.52 (.060)
1.02 (.040)
13 LEAD NO. 1
9.90 (.390)
10.41 (.410)
3
15.88 (.625)
14.99 (.590)
0.48 (.019)
0.38 (.015)
9.40 (.370)
8.38 (.330)
10.16 (.400)
9.14 (.360)
28 96 (1.140)
25.91 (1.020)
14
0.76 (.030)
15
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.52 (.020)
2.16 (.085)
1.27 (.050)

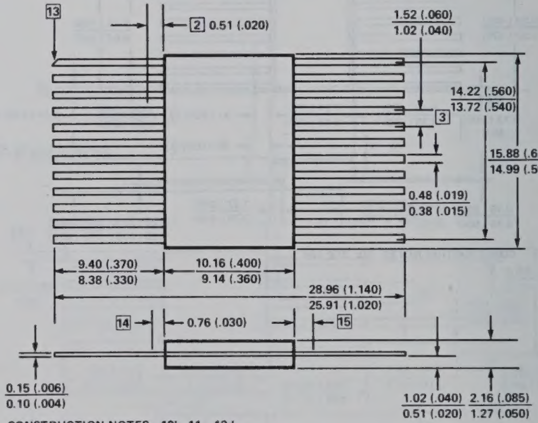
CONSTRUCTION NOTES: 10b, 11c, 12d

QNA Package


24.38 (.960)
23.88 (.940)
1.40 (.055)
1.14 (.045)
3
0.51 (.020)
2
LEAD NO. 1
13
.000 MIN.
17
14.22 (.560)
13.72 (.540)
10.29 (.405)
9.52 (.375)
1.10 (.004) MIN.
0.15 (.006)
0.10 (.004)
16
.76 (.030)
14
0.48 (.019)
0.38 (.015)
0.64 (.025)
0.25 (.010)
5.08 (.200)
4.57 (.180)
2.16 (.085)
1.78 (.060)
1.27 (.050)
0.76 (.030)
9.40 (.370)
8.38 (.330)
7.24 (.285)
6.48 (.255)

CONSTRUCTION NOTES: 10c, 11d, 12b

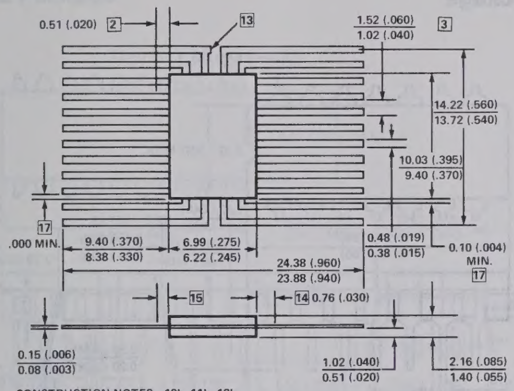
RNA Package


13
2 0.51 (.020)
1.52 (.060)
1.02 (.040)
14.22 (.560)
13.72 (.540)
3
15.88 (.625)
14.99 (.590)
0.48 (.019)
0.38 (.015)
9.40 (.370)
8.38 (.330)
10.16 (.400)
9.14 (.360)
28.96 (1.140)
25.91 (1.020)
14
0.76 (.030)
15
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.27 (.050)

CONSTRUCTION NOTES: 10b, 11c, 12d

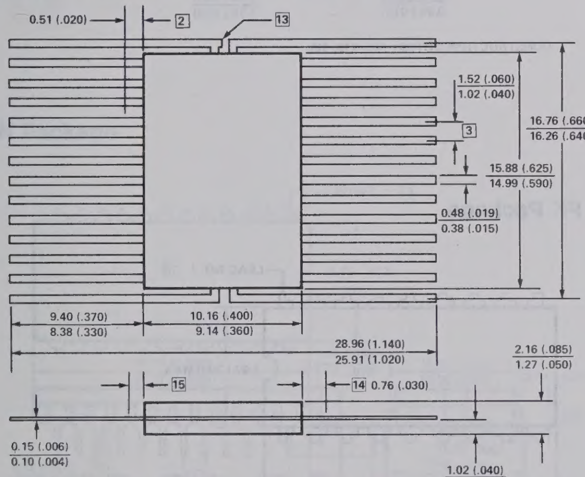
HERMETIC: Flat Packs (cont'd.)

WN Package


0.51 (.020)
2
13
1.52 (.060)
1.02 (.040)
3
14.22 (.560)
13.72 (.540)
10.03 (.395)
9.40 (.370)
17
.000 MIN.
9.40 (.370)
8.38 (.330)
6.99 (.275)
6.22 (.245)
0.48 (.019)
0.38 (.015)
0.10 (.004)
MIN.
17
24.38 (.960)
23.88 (.940)
15
14
0.76 (.030)
0.15 (.006)
0.08 (.003)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.40 (.055)

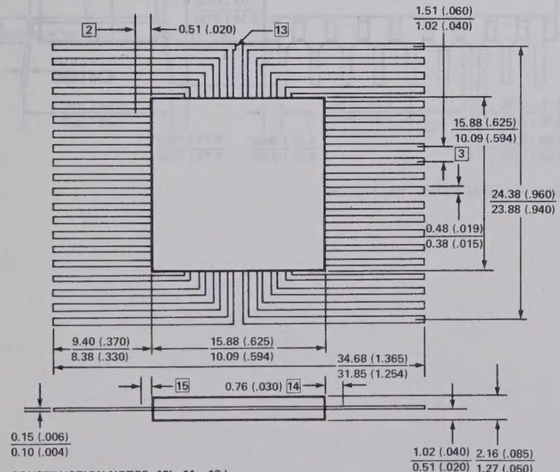
CONSTRUCTION NOTES: 10b, 11b, 12b

RQA Package


0.51 (.020)
2
13
1.52 (.060)
1.02 (.040)
3
16.76 (.660)
16.26 (.640)
15.88 (.625)
14.99 (.590)
0.48 (.019)
0.38 (.015)
9.40 (.370)
8.38 (.330)
10.16 (.400)
9.14 (.360)
28.96 (1.140)
25.91 (1.020)
2.16 (.085)
1.27 (.050)
15
14
0.76 (.030)
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.51 (.020)

CONSTRUCTION NOTES: 10b, 11c, 12d

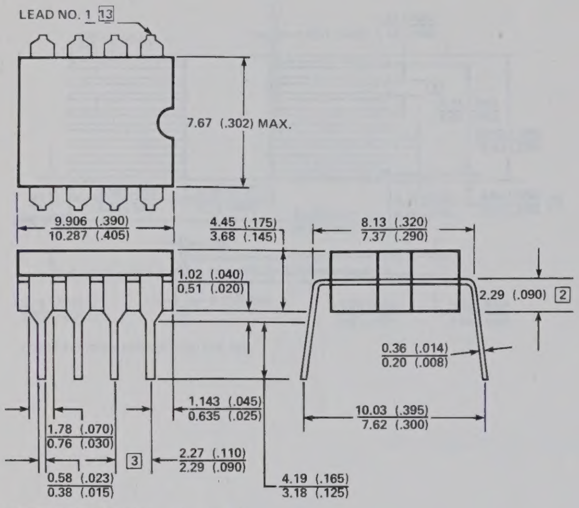
RWA Package


1.51 (.060)
1.02 (.040)
2
0.51 (.020)
13
15.88 (.625)
10.09 (.594)
3
24.38 (.960)
23.88 (.940)
0.48 (.019)
0.38 (.015)
9.40 (.370)
8.38 (.330)
15.88 (.625)
10.09 (.594)
34.68 (1.365)
31.85 (1.254)
15
0.76 (.030)
14
0.15 (.006)
0.10 (.004)
1.02 (.040)
0.51 (.020)
2.16 (.085)
1.27 (.050)

CONSTRUCTION NOTES: 10b, 11c, 12d

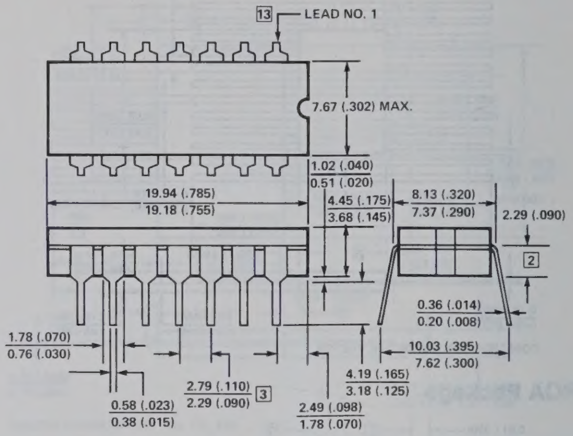
HERMETIC: Cerdip Family

FE Package


LEAD NO. 1 13
7.67 (.302) MAX.
9.906 (.390)
10.287 (.405)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
1.02 (.040)
0.51 (.020)
2.29 (.090) 2
0.36 (.014)
0.20 (.008)
1.143 (.045)
0.635 (.025)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
3
2.27 (.110)
2.29 (.090)
0.58 (.023)
0.38 (.015)
4.19 (.165)
3.18 (.125)

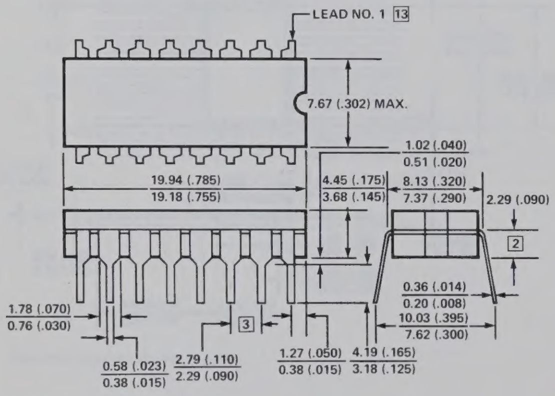
CONSTRUCTION NOTES: 10b, 11b, 12b

FH Package


13 LEAD NO. 1
7.67 (.302) MAX.
1.02 (.040)
0.51 (.020)
19.94 (.785)
19.18 (.755)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
2
0.36 (.014)
0.20 (.008)
1.78 (.070)
0.76 (.030)
10.03 (.395)
7.62 (.300)
4.19 (.165)
3.18 (.125)
2.79 (.110)
2.29 (.090)
3
0.58 (.023)
0.38 (.015)
2.49 (.098)
1.78 (.070)

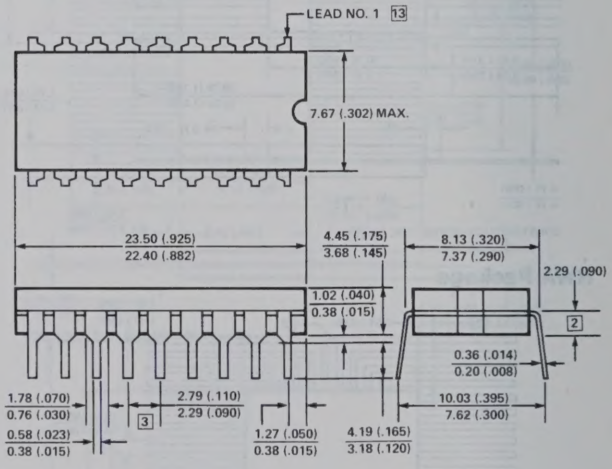
CONSTRUCTION NOTES: 10b, 11b, 12b

FJ Package


LEAD NO. 1 13
7.67 (.302) MAX.
1.02 (.040)
0.51 (.020)
19.94 (.785)
19.18 (.755)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
2
0.36 (.014)
0.20 (.008)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
3
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.27 (.050)
0.38 (.015)
4.19 (.165)
3.18 (.125)

CONSTRUCTION NOTES: 10b, 11b, 12b

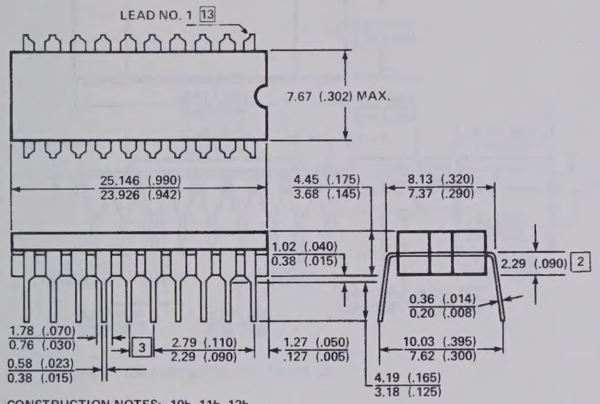
FK Package


LEAD NO. 1 13
7.67 (.302) MAX.
23.50 (.925)
22.40 (.882)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
1.02 (.040)
0.38 (.015)
2
0.36 (.014)
0.20 (.008)
1.78 (.070)
0.76 (.030)
2.79 (.110)
2.29 (.090)
3
10.03 (.395)
7.62 (.300)
0.58 (.023)
0.38 (.015)
1.27 (.050)
0.38 (.015)
4.19 (.165)
3.18 (.120)

CONSTRUCTION NOTES: 10b, 11b, 12b

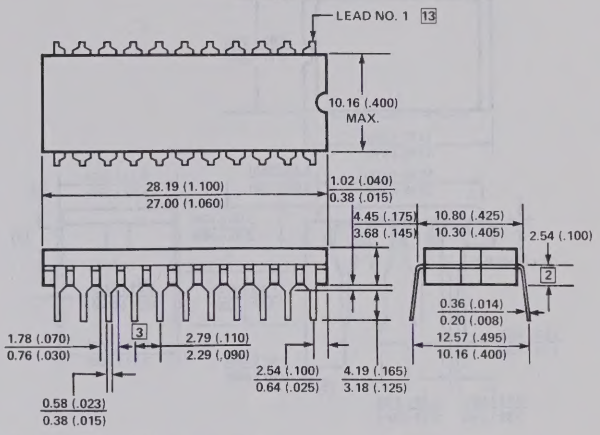
HERMETIC: Cerdip Family (cont'd.)

FL Package


LEAD NO. 1 13
7.67 (.302) MAX.
25.146 (.990)
23.926 (.942)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
1.02 (.040)
0.38 (.015)
2.29 (.090) 2
0.36 (.014)
0.20 (.008)
1.78 (.070)
0.76 (.030)
3
2.79 (.110)
2.29 (.090)
1.27 (.050)
.127 (.005)
10.03 (.395)
7.62 (.300)
0.58 (.023)
0.38 (.015)
4.19 (.165)
3.18 (.125)

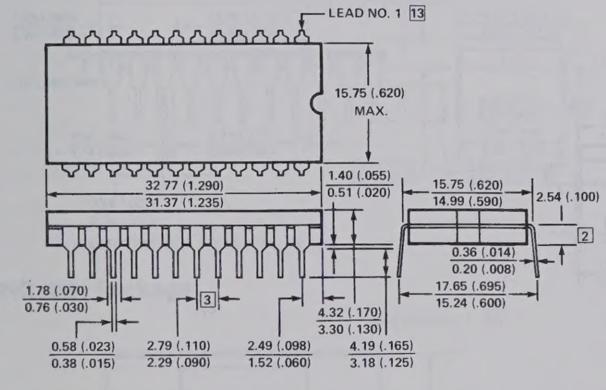
CONSTRUCTION NOTES: 10b, 11b, 12b

FM Package


LEAD NO. 1 13
10.16 (.400)
MAX.
28.19 (1.100)
27.00 (1.060)
1.02 (.040)
0.38 (.015)
4.45 (.175)
3.68 (.145)
10.80 (.425)
10.30 (.405)
2.54 (.100)
2
0.36 (.014)
0.20 (.008)
12.57 (.495)
10.16 (.400)
1.78 (.070)
0.76 (.030)
3
2.79 (.110)
2.29 (.090)
2.54 (.100)
0.64 (.025)
4.19 (.165)
3.18 (.125)
0.58 (.023)
0.38 (.015)

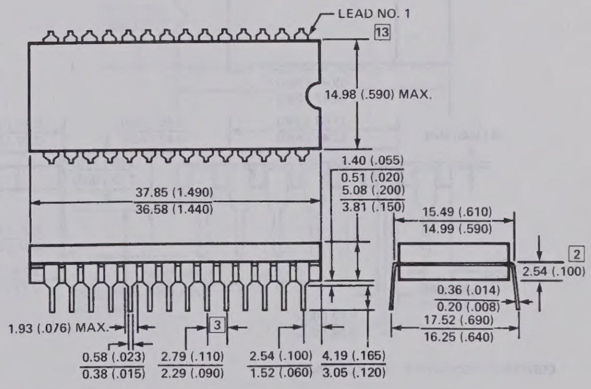
CONSTRUCTION NOTES: 10b, 11b, 12b

FN Package


LEAD NO. 1 13
15.75 (.620)
MAX.
1.40 (.055)
0.51 (.020)
32 77 (1.290)
31.37 (1.235)
15.75 (.620)
14.99 (.590)
2.54 (.100)
2
0.36 (.014)
0.20 (.008)
17.65 (.695)
15.24 (.600)
1.78 (.070)
0.76 (.030)
3
4.32 (.170)
3.30 (.130)
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.49 (.098)
1.52 (.060)
4.19 (.165)
3.18 (.125)

CONSTRUCTION NOTES: 10b, 11b, 12b

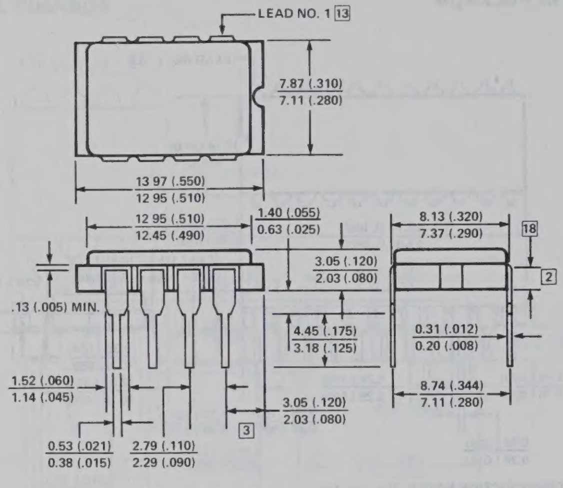
FQ Package


LEAD NO. 1
13
14.98 (.590) MAX.
1.40 (.055)
0.51 (.020)
5.08 (.200)
3.81 (.150)
37.85 (1.490)
36.58 (1.440)
15.49 (.610)
14.99 (.590)
2
2.54 (.100)
0.36 (.014)
0.20 (.008)
17.52 (.690)
16.25 (.640)
1.93 (.076) MAX.
3
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.54 (.100)
1.52 (.060)
4.19 (.165)
3.05 (.120)

CONSTRUCTION NOTES: 10b, 11b, 12b

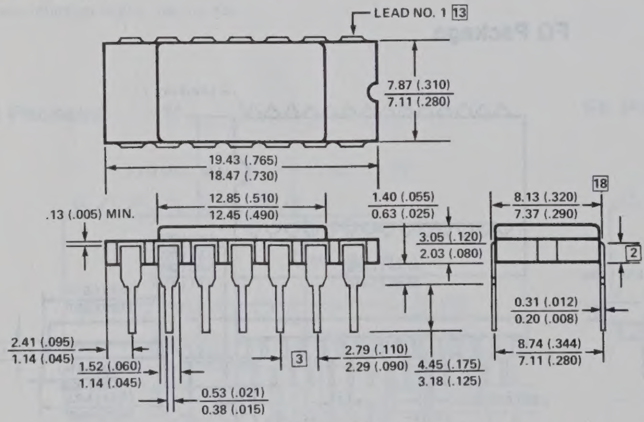
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package


LEAD NO. 1 13
7.87 (.310)
7.11 (.280)
13 97 (.550)
12 95 (.510)
12 95 (.510)
12.45 (.490)
1.40 (.055)
0.63 (.025)
8.13 (.320)
7.37 (.290)
18
3.05 (.120)
2.03 (.080)
2
.13 (.005) MIN.
4.45 (.175)
3.18 (.125)
0.31 (.012)
0.20 (.008)
1.52 (.060)
1.14 (.045)
8.74 (.344)
7.11 (.280)
3.05 (.120)
2.03 (.080)
3
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)

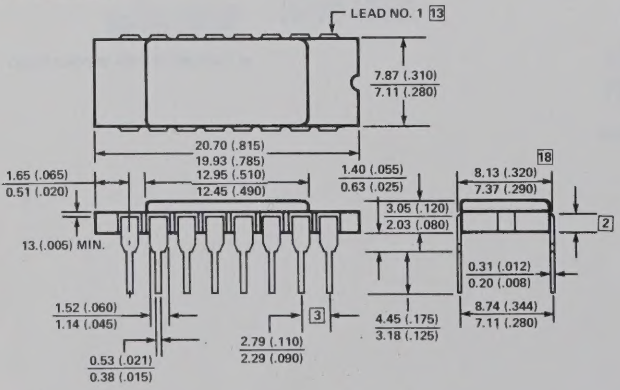
CONSTRUCTION NOTES: 10b, 11d, 12b

IHA Package


LEAD NO. 1 13
7.87 (.310)
7.11 (.280)
19.43 (.765)
18.47 (.730)
18
.13 (.005) MIN.
12.85 (.510)
12.45 (.490)
1.40 (.055)
0.63 (.025)
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
2
0.31 (.012)
0.20 (.008)
2.41 (.095)
1.14 (.045)
1.52 (.060)
1.14 (.045)
3
2.79 (.110)
2.29 (.090)
4.45 (.175)
3.18 (.125)
8.74 (.344)
7.11 (.280)
0.53 (.021)
0.38 (.015)

CONSTRUCTION NOTES: 10b, 11d, 12b

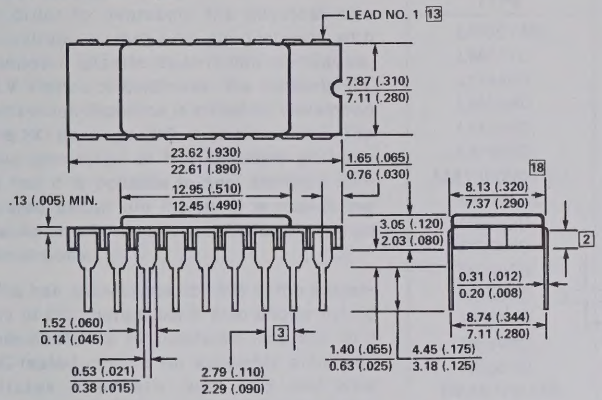
IJA Package


LEAD NO. 1 13
7.87 (.310)
7.11 (.280)
20.70 (.815)
19.93 (.785)
18
1.65 (.065)
0.51 (.020)
12.95 (.510)
12.45 (.490)
1.40 (.055)
0.63 (.025)
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
2
13.(.005) MIN.
0.31 (.012)
0.20 (.008)
1.52 (.060)
1.14 (.045)
3
4.45 (.175)
3.18 (.125)
8.74 (.344)
7.11 (.280)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)

CONSTRUCTION NOTES: 10b, 11d, 12b

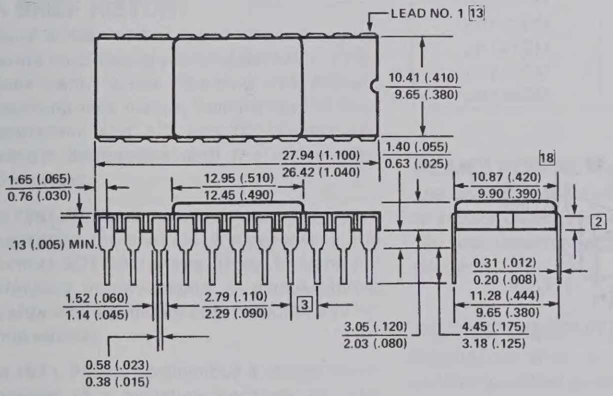
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IKA/IKB Package


LEAD NO. 1 13
7.87 (.310)
7.11 (.280)
23.62 (.930)
22.61 (.890)
1.65 (.065)
0.76 (.030)
18
.13 (.005) MIN.
12.95 (.510)
12.45 (.490)
8.13 (.320)
7.37 (.290)
3.05 (.120)
2.03 (.080)
2
0.31 (.012)
0.20 (.008)
1.52 (.060)
0.14 (.045)
3
8.74 (.344)
7.11 (.280)
1.40 (.055)
0.63 (.025)
4.45 (.175)
3.18 (.125)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)

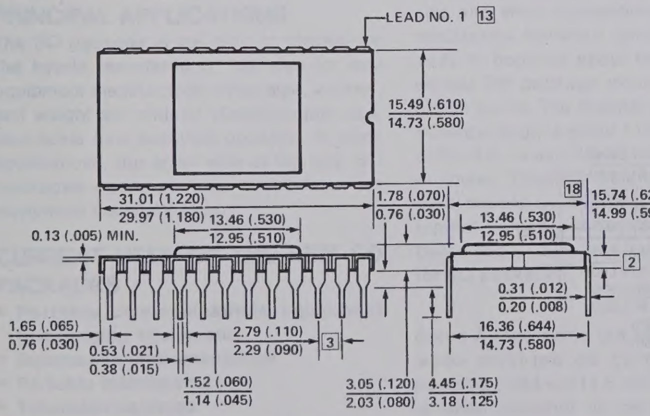
CONSTRUCTION NOTES: 10b, 11d, 12b OR 12c

IMA Package


LEAD NO. 1 13
10.41 (.410)
9.65 (.380)
1.40 (.055)
0.63 (.025)
27.94 (1.100)
26.42 (1.040)
18
1.65 (.065)
0.76 (.030)
12.95 (.510)
12.45 (.490)
10.87 (.420)
9.90 (.390)
2
.13 (.005) MIN.
0.31 (.012)
0.20 (.008)
1.52 (.060)
1.14 (.045)
2.79 (.110)
2.29 (.090)
3
11.28 (.444)
9.65 (.380)
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)
0.58 (.023)
0.38 (.015)

CONSTRUCTION NOTES: 10b, 11d, 12b

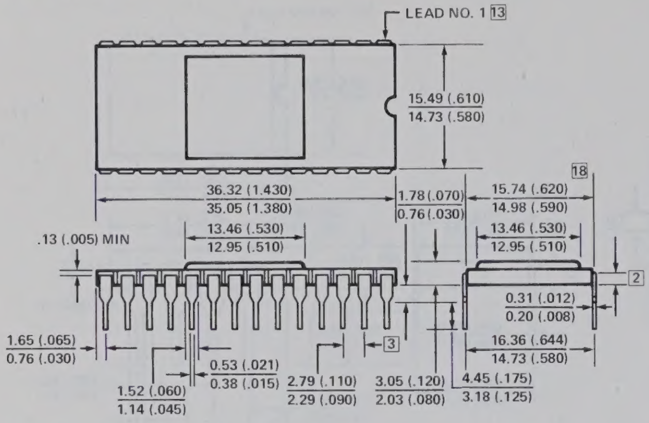
INC/INH Package


LEAD NO. 1 13
15.49 (.610)
14.73 (.580)
31.01 (1.220)
29.97 (1.180)
1.78 (.070)
0.76 (.030)
18
15.74 (.620)
14.99 (.590)
13.46 (.530)
12.95 (.510)
13.46 (.530)
12.95 (.510)
0.13 (.005) MIN.
2
0.31 (.012)
0.20 (.008)
1.65 (.065)
0.76 (.030)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
3
16.36 (.644)
14.73 (.580)
1.52 (.060)
1.14 (.045)
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)

CONSTRUCTION NOTES: 10b, 11b, 12b

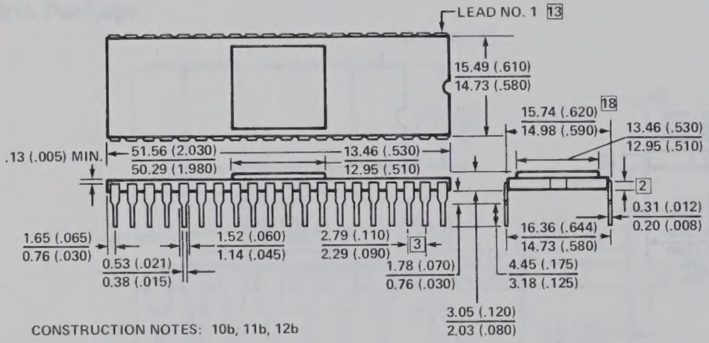
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package


LEAD NO. 1 13
15.49 (.610)
14.73 (.580)
18
36.32 (1.430)
35.05 (1.380)
1.78 (.070)
0.76 (.030)
15.74 (.620)
14.98 (.590)
13.46 (.530)
12.95 (.510)
.13 (.005) MIN
13.46 (.530)
12.95 (.510)
2
0.31 (.012)
0.20 (.008)
1.65 (.065)
0.76 (.030)
3
16.36 (.644)
14.73 (.580)
0.53 (.021)
0.38 (.015)
1.52 (.060)
1.14 (.045)
2.79 (.110)
2.29 (.090)
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)

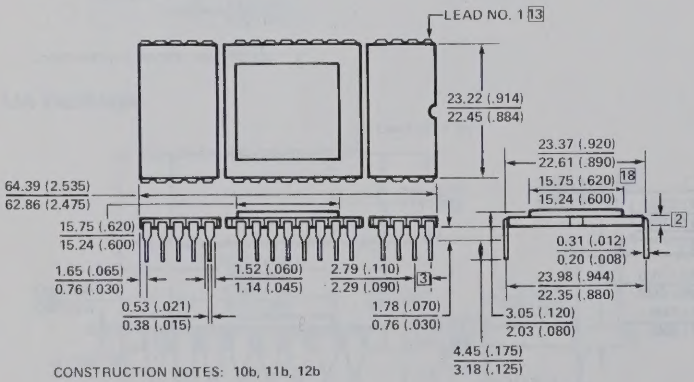
CONSTRUCTION NOTES: 10b, 11b, 12b

IWA Package


LEAD NO. 1 13
15.49 (.610)
14.73 (.580)
15.74 (.620)
14.98 (.590)
18
13.46 (.530)
12.95 (.510)
.13 (.005) MIN.
51.56 (2.030)
50.29 (1.980)
13.46 (.530)
12.95 (.510)
2
0.31 (.012)
0.20 (.008)
16.36 (.644)
14.73 (.580)
1.65 (.065)
0.76 (.030)
1.52 (.060)
1.14 (.045)
2.79 (.110)
2.29 (.090)
3
0.53 (.021)
0.38 (.015)
1.78 (.070)
0.76 (.030)
4.45 (.175)
3.18 (.125)
3.05 (.120)
2.03 (.080)

CONSTRUCTION NOTES: 10b, 11b, 12b

IZA Package


LEAD NO. 1 13
23.22 (.914)
22.45 (.884)
23.37 (.920)
22.61 (.890)
15.75 (.620)
15.24 (.600)
18
64.39 (2.535)
62.86 (2.475)
15.75 (.620)
15.24 (.600)
2
0.31 (.012)
0.20 (.008)
1.65 (.065)
0.76 (.030)
1.52 (.060)
1.14 (.045)
2.79 (.110)
2.29 (.090)
3
23.98 (.944)
22.35 (.880)
0.53 (.021)
0.38 (.015)
1.78 (.070)
0.76 (.030)
3.05 (.120)
2.03 (.080)
4.45 (.175)
3.18 (.125)

CONSTRUCTION NOTES: 10b, 11b, 12b

WHAT IS A MINIATURE IC PACKAGE?

In order to overcome the physical size constraint sometimes encountered with standard plastic dual-in-line packages, N.V. Philips of Eindhoven, the Netherlands, with which Signetics is affiliated, developed the SO package (SO = small outline). The true advantage of this miniature package is that it is possible to seal standard integrated circuit die inside of a dual-in-line package with significantly reduced outside dimensions.

This has advantages not only in the assembly of PC boards, but it also allows hybrid manufacturers to purchase fully DC- and AC-tested circuits for assembly onto substrates. Presently, with chip and wire assembly techniques, it is only possible to purchase DC-tested, unpackaged integrated circuits.

A BRIEF HISTORY

Early in the 1960's, hybrid circuit manufacturers began using unpackaged chips. Problems swiftly arose. Handling was difficult, mounting was messy, bonding was a hand operation, and AC- and DC-testing was almost impossible until the circuit was completed.

In 1967, Philips introduced the first miniature packages for discrete components in the form of SOT-23 devices. These brought outstanding improvements in manufacturing yields with significant cost reductions to hybrid circuits.

In 1971, Philips commenced a similar development of a miniature package for integrated circuits for use in the Swiss watch industry.

PRINCIPAL APPLICATIONS

The SO package is not only of interest for the hybrid manufacturer, but also for any equipment manufacturer when size, volume, and weight are critical. Miniaturization on a new scale now becomes possible. In many applications, the small size of the new SO packages opens up new possibilities for equipment manufacturers.

CURRENT USES OF THE NEW SO PACKAGES

- **Portable communications equipment (e.g. paging equipment)**
- **Automobile instrumentation**
- **Portable instruments**
- **Television cameras**
- **Photographic cameras**
- **Telephone transmission equipment**
- **Model control**

TYPES OF CIRCUITS CURRENTLY AVAILABLE

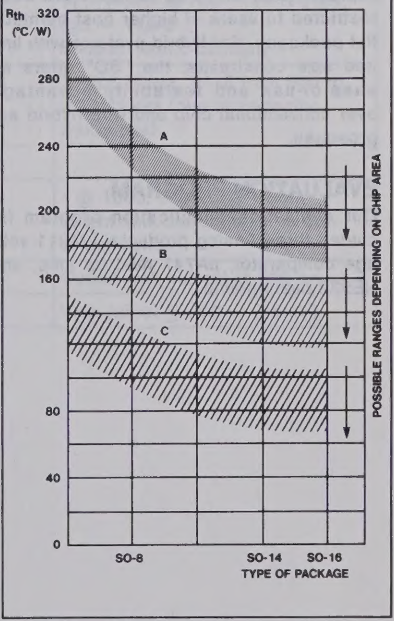
TYPE	PACKAGE	FUNCTION
LM301AD	SO-8	High performance op amp
LM311D	SO-8	Single general purpose comparator
LM319D	SO-14	Dual voltage comparator
LM324D	SO-14	Quad op amp
LM339D	SO-14	Quad voltage comparator
LM358D	SO-8	Dual op amp
LM13600D/AD	SO-8	Dual operational transconductance amplifier
MC1458D	SO-8	Dual op amp
NE532D	SO-8	Dual op amp
NE544D	SO-14	Servo amplifier
NE555D	SO-8	Timer
NE556D	SO-14	Dual timer
NE564D	SO-16	Phase locked loop
NE592D	SO-14	Video amplifier
NE5512	SO-8	Dual high performance op amp
NE5517D/AD	SO-16	Dual operational transconductance amplifier
NE5534D	SO-8	Low noise op amp
NE5539D	SO-14	Ultra high frequency op amp
NE5044D	SO-16	Seven channel R.C. encoder
NE5045D	SO-16	Seven channel R.C. decoder
μA723CD	SO-14	Precision voltage regulator
μA741CD	SO-8	General purpose op amp
μA747CD	SO-14	Dual general purpose op amp
μA748CD	SO-8	General purpose op amp

PLANS FOR NEW TYPES

Our analog product range will be extended to include devices in the new SO packaging. We are considering the full line of analog products.

POWER DISSIPATION

Considering their size, the SO packages exhibit excellent properties of power dissipation. When mounted on a ceramic substrate, the heat dissipated can be readily conducted away from the source. The thin size and short connections give a thermal resistance between junction and solder pads or heatsink about the same as for a normal DIP package mounted on a printed circuit board. The thermal resistance of the SO-8 package is about 110°C/W, while that of the SO-14 and SO-16 is about 100°C/W, or lower. Thermal resistance does, however, depend on chip size. The graph shows typical values of thermal resistance between the junction and heatsink or ambient for SO packages.



Curve A represents the thermal resistance when mounted on ceramic against a heatsink (.984 x .511 x .023 inches); curve B is when mounted on ceramic in free air; curve C is when mounted on a printed circuit board in free air.

RELIABILITY ENGINEERING QUALIFICATION REPORT ON THE "SO" PACKAGE

A Miniature Molded Epoxy Package

K. M. Self & P. J. Naumchik
Signetics Reliability Engineering

ABSTRACT

This report summarizes the Reliability Engineering activities undertaken to evaluate and qualify a miniature molded epoxy package configuration identified as the "SO." The evaluation demonstrated that the stress performance of the "SO" Package is equivalent to the larger standard molded epoxy dual-in-line package in all aspects, and mounted, the package thermal resistance characteristics are exceptional considering the reduced size and mass of the package.

BACKGROUND/ADVANTAGES

The "SO" Package was developed by N.V. Philips in 1967 for applications in hybrid structures and later for watch modules.

The reduced size of this package (refer to Figure 1) offers significant packing density improvements which up to now have been restricted to users of higher cost hermetic flat packages. For hybrid systems with limited size constraints, the "SO" offers an ease-of-use and testability advantage over conventional chip and wire hybrid approaches.

EVALUATION PROGRAM

Our evaluation/qualification program included three Analog products; LM311 voltage comparator, μA747 dual op amp, and NE532 dual op amp. These devices encompass three wafer fabrication processes and both 8-Pin and 14-Pin package configurations.

All products were assembled on Alloy 42 lead frames, die attached utilizing conventional gold-silicon eutectic and molded in our standard Morton 410B epoxy Novalac compound. The devices were subjected to a series of accelerated stresses and tested to conventional data sheet parameters. Variables data was taken and drift analysis was performed.

The stress conditions employed were as follows:

- High Temperature Bias Life
  $T_A = 125°C$ $V_{CC} = \pm 15V$
- High Temperature Storage Life
  $T_A = 150°C$
- Temperature/Humidity Bias Life
  $T_A = 85°C$ RH = 85% $V_{CC} = \pm 15V$
- Temperature/Humidity/Pressure (Pressure Cooker) $T_A = 121°C$
  15 PSIG 100% Sat. Steam
- Thermal Shock (Liquid to Liquid)
  −65°C to 150°C

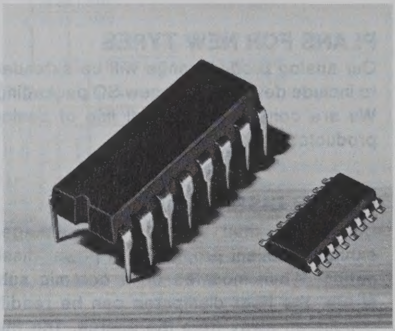


Figure 1

PROGRAM RESULTS

The details of all the stress results are included in Table I. The size of the "SO" Package tends to suggest that the structure may be less rugged than its molded dual-in-line counter part. The test results demonstrate how misleading a factor size can be. In all stresses the "SO" devices performed as well as standard dual-in-line product. Requirements for qualification were met or exceeded on all three products evaluated.

THERMAL RESISTANCE

Thermal resistance measurements were made with devices mounted on a 2CM x 1CM (13/16" x 3/8") ceramic substrate. The results were as follows:

8-Pin "SO" $\theta_{JA} = 110°C/W$
14-Pin "SO" $\theta_{JA} = 100°C/W$
16-Pin "SO" $\theta_{JA} = 100°C/W$

CONCLUSIONS

The "SO" Package constructed with Alloy-42 lead frame, Au-Si eutectic die attach, and molded in 410B epoxy Novalac provides an integrated circuit with a reliable barrier to hostile external environmental conditions and stresses. It is qualified for use with any Signetics Bipolar Analog or Bipolar Logic device which can tolerate the physical limitations of die attach pad size and can operate reliably within the thermal resistance limitations of the package.

RELIABILITY EVALUATION RESULTS

RELIABILITY ENGINEERING PROJECT ID	SIGNETICS PRODUCT TYPE	STRESS	STRESS CONDITIONS	STRESS DURATION	CUMULATIVE RESULT	ANALYSIS
790707	LM311 (14 Lead "SO")	HTOL	125°C	2,000 Hours	1/49	1 @ 168 Hours: Ball bond to trace short.
		HTSL	150°C	2,000 Hours	0/50	
		Bias/Temperature/Humidity	85°C @ 85% RH V_{CC} = 5.5V	2,000 Hours	2/50	2 @ 2000 Hours: Internal metal corrosion.
		Pressure Pot	121°C 15PSIG	432 Hours	2/51	1 @ 192 Hours: Output leakage = 68nA 1 @ 432 Hours: Output Leakage = 100nA Both internal metal corrosion.
		Thermal Shock	−65°C TO +150°C	1,000 ~	0/45	
790708	μA747 (14 Lead "SO")	HTOL	125°C ± 15V	2,000 Hours	2/50	1 @ 168 Hours: V_{OS} = 10mV. V_{OS} = 7.4mV @ 2K Hours 1 @ 1500 Hours V_{OS} = −80mV, I_B = 8μA Suspect static damage.
		HTSL	150°C	2,000 Hours	0/50	
		Bias/Temperature/Humidity	85°C @ 85% RH V_{CC} = 5.5V	2,000 Hours	1/50	V_{OS} reject @ 500 Hours (−80mV) suspect static damage
		Pressure Pot	121°C 15PSIG	312 Hours	3/50	Three V_{OS} rejects @ 312 Hours (~ 8mV)
		Thermal Shock	−65°C TO +150°C	1,000 ~	1/48	V_{OS} reject @ 700 ~ (−170 mV, I_{B-} = 14μA) Suspect static damage
795003	NE532 (8 Lead "SO")	HTOL	150°C	2,000 Hours	0/45	To 500 Hours, 0/18 from 500 to 2000 Hours (due to capacity limitations).
		HTSL	150°C	2,000 Hours	0/46	
		Bias/Temperature/Humidity	85°C @ 85% RH	2,000 Hours	2/49	1 @ 1500, 1 @ 2000—Both output sink current failures due to corrosion.
		Pressure Pot	121°C 15PSIG	456 Hours	1/43	Output sink current @ 288 hours.
		Thermal Shock	−65°C TO +150°C	1,000 ~	1/45	V_{OS} reject @ 200 ~ (15mV)

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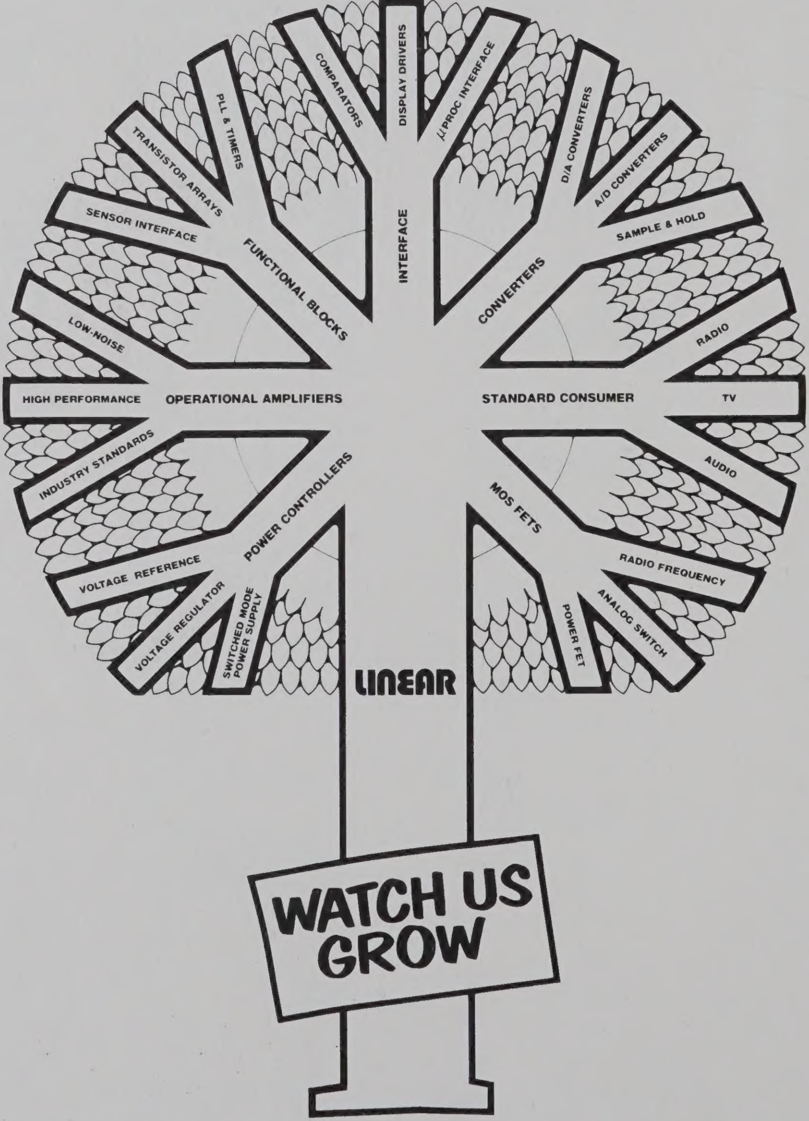
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